System-Level Design Space Exploration for SoCs Integrating Optical Networks on Chip

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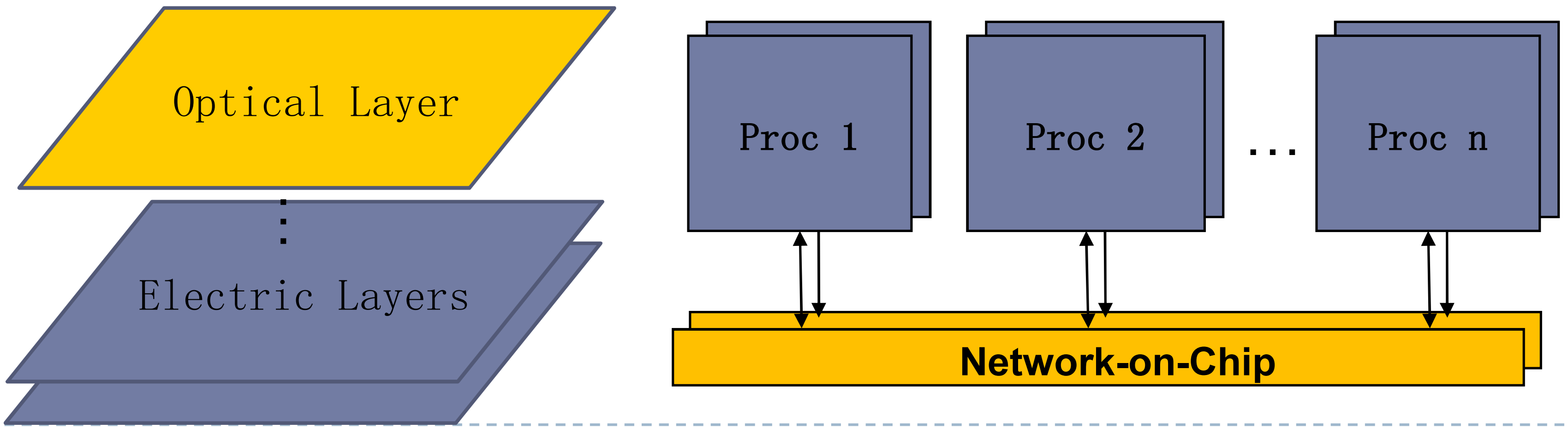
Multi-Processor Systems-on-Chip (MPSoC) Design Trends

- SoC Design – two contradictory trends
  - Rising platform development cost
    - Embedded software – over 50% of the total cost
      - Complexity increasing with 140% per year
  - Reducing the product market window
- Directions to tackle these challenges
  - Exploit domain-specific MPSoC reusable platforms
    - Several interconnected processors
    - Networks-on-Chip
- Classical Network-on-Chip Issues
  - High power consumption
  - Limited bandwidth
  - Long latency
  - Poor scalability

> Studies have shown that global metallic interconnects will consume kilowatts of power to achieve the communication bandwidth that will be required by MPSoCs by 2020 using the 14 nm process

Multi-Processor Systems-on-Chip (MPSoC) Design Trends

- Integration of Heterogeneous Technologies
  - Promising paradigm
    - Multiple technologies
    - Functions will use the best technology available
      - Ex. computing → electronics / communication → optics



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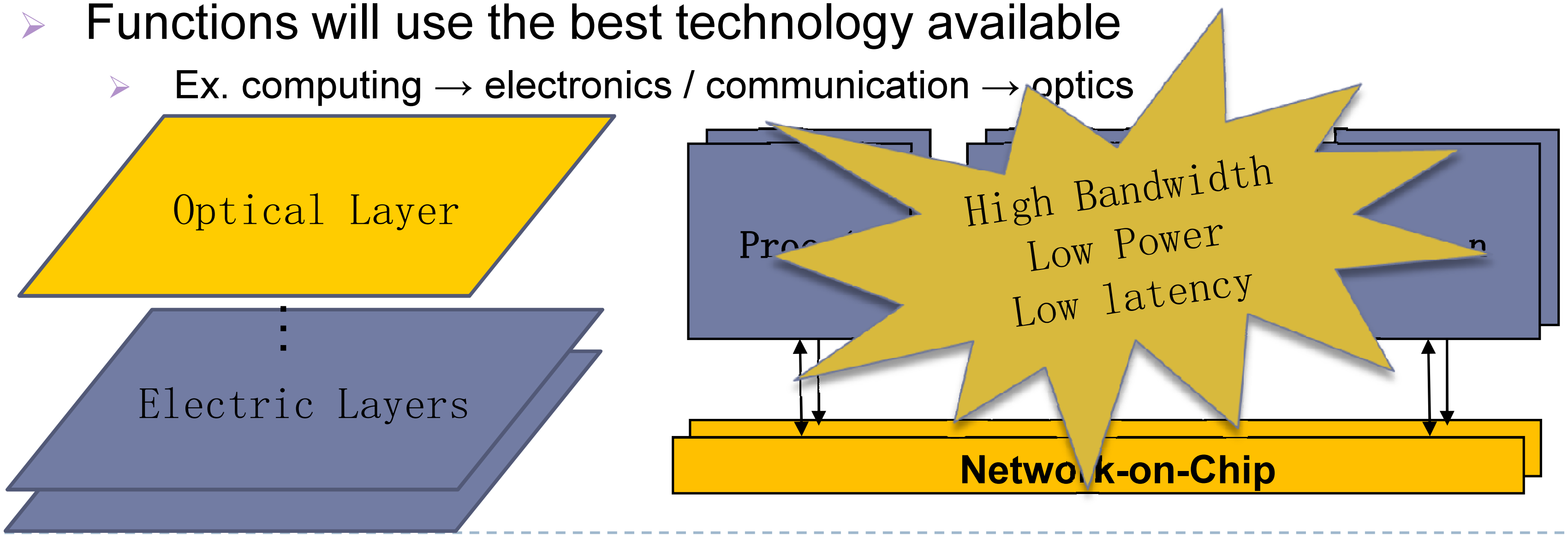
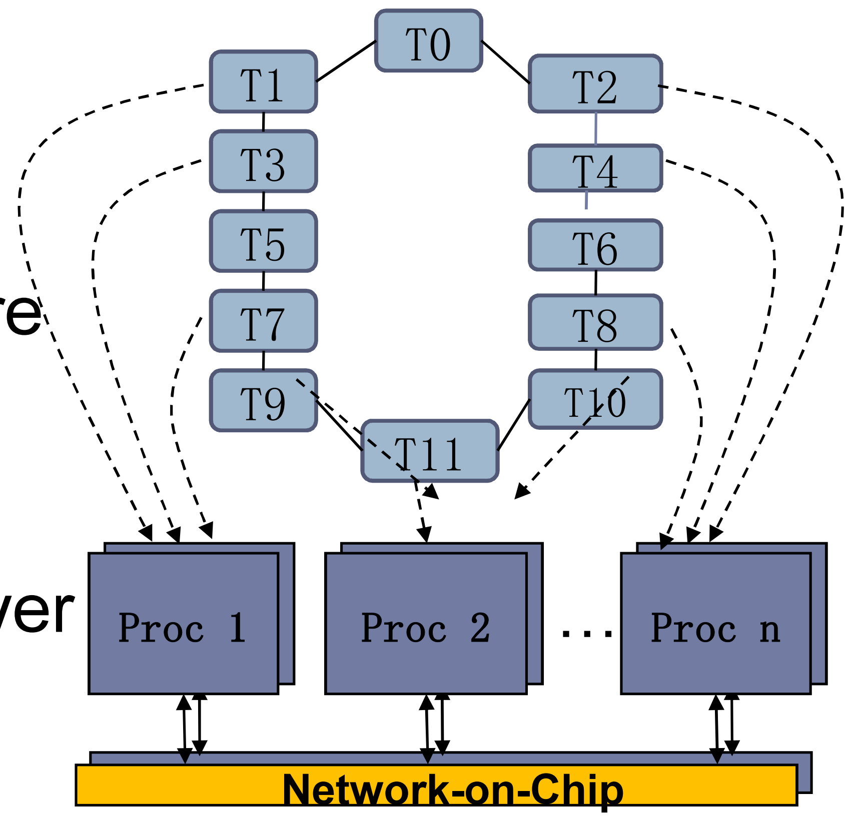


Optical Integration Today

- Intel
  - Integration of high-speed switches and optical fabrics
- HP
  - MACHINE project
    - approximately 75% of the researchers involved
    - silicon photonics is employed to link a multicore system-on-chip to a bank of memristor memory cards
- IBM
  - $3 Billion Research Initiative to Tackle Chip Grand Challenges for Cloud and Big Data Systems
    - Silicon Photonics is one of the explored technologies

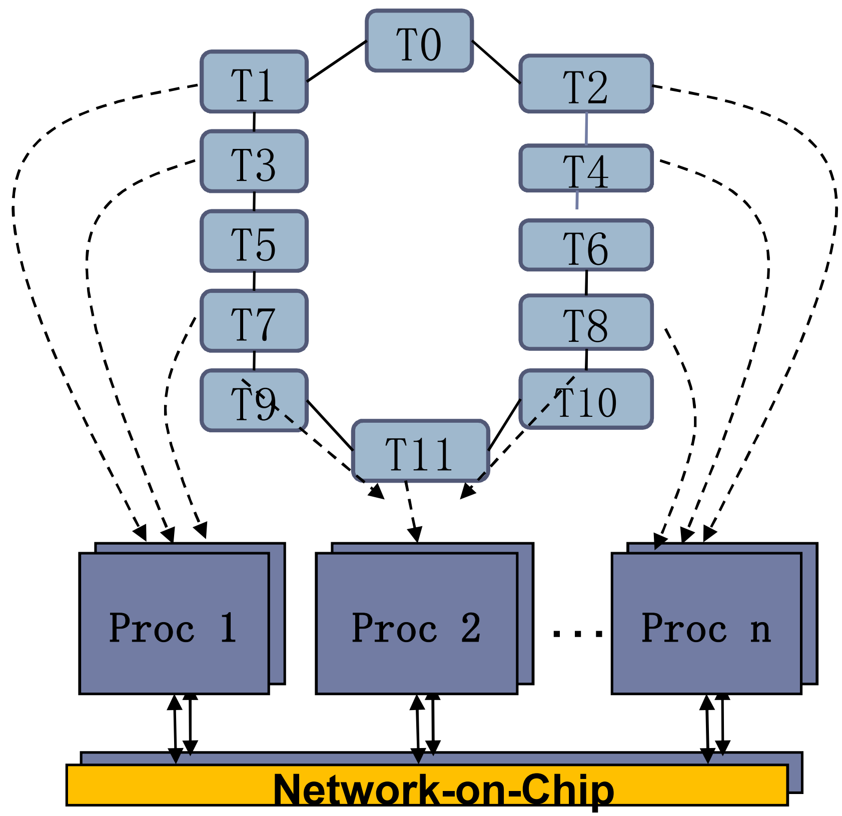
Configuration Parameters in MPSoC Design

- Type of Network on Chip
- Type of routing
- Type of processors
- No. of proc. in the architecture
- No. of proc. per layer (tier)
- No. of layers (tiers)
- Technology used for each layer
- Application Mapping



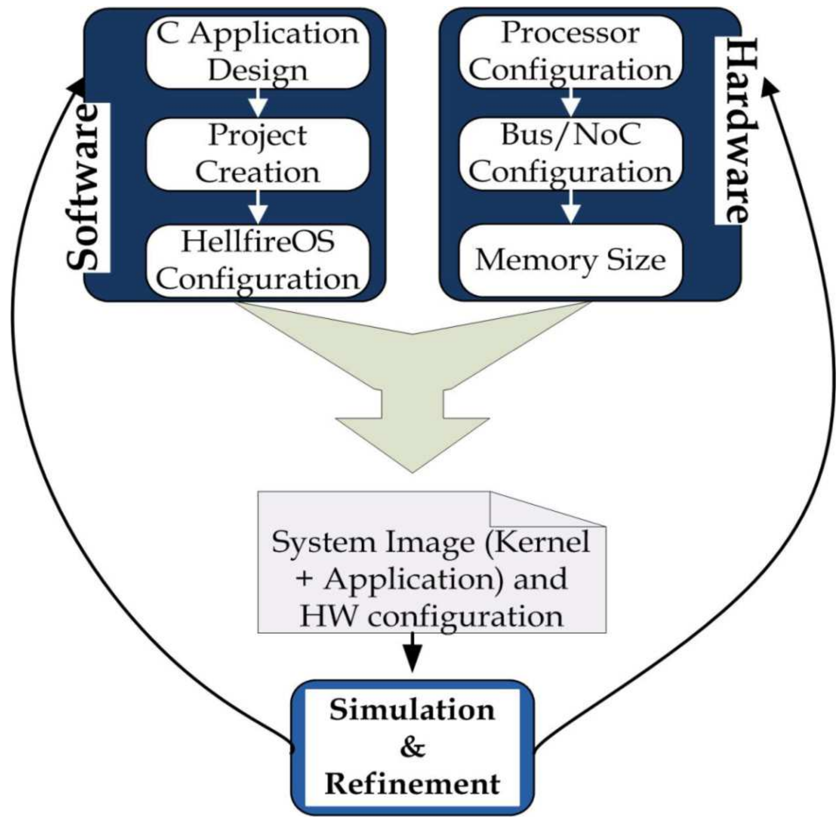
Configuration Parameters in MPSoC Design

- Huge solutions space
  - Fast and accurate system-level tools for design-space exploration are mandatory



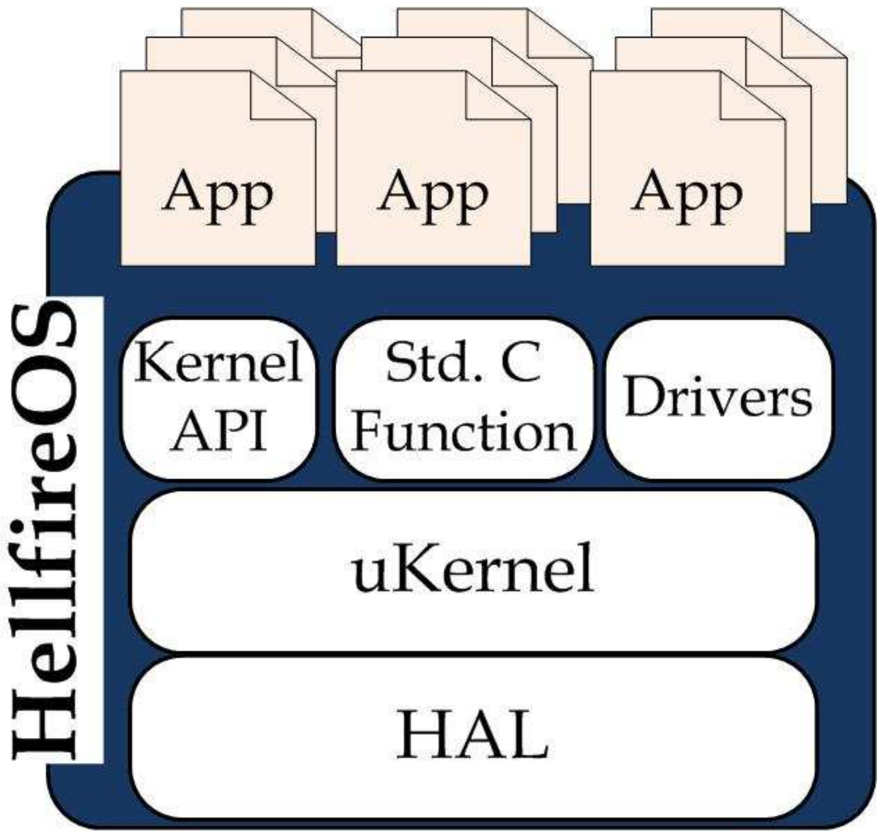
Integrating Optical Network on chip Models to an existing System-Level Platform

- HellFire Framework
  - Proposed design-flow for the deployment of embedded applications
  - Set of tools to aid the designer on the project
    - HellfireOS
    - Simulator
    - Web-GUI



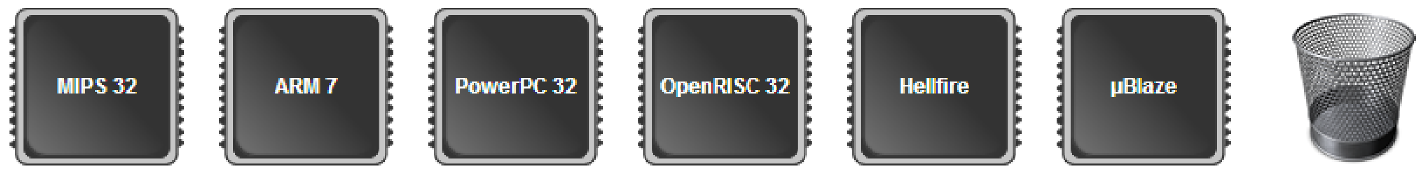
Integrating Optical Network on chip Models to an existing System-Level Platform

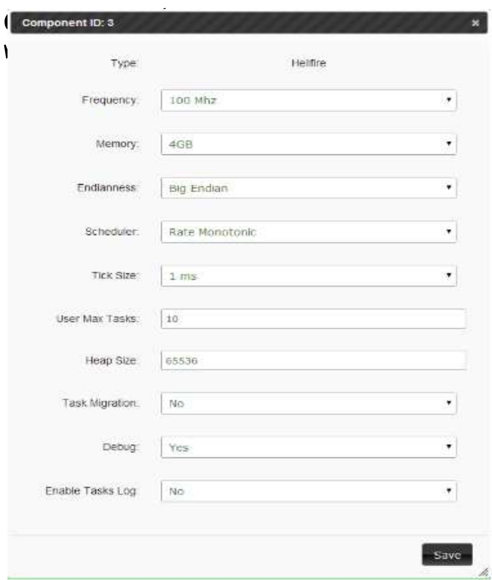
- HellFireOS
  - Modular Structure
  - *POSIX Like*
  - Real-time support
  - Easily portable
  - Parametrizable
  - Stack size (each task)
  - Heap size
  - *Number of user tasks*
  - *Tick size*
  - *Scheduling police*

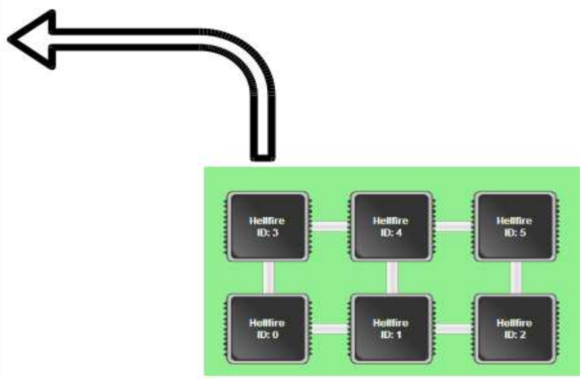


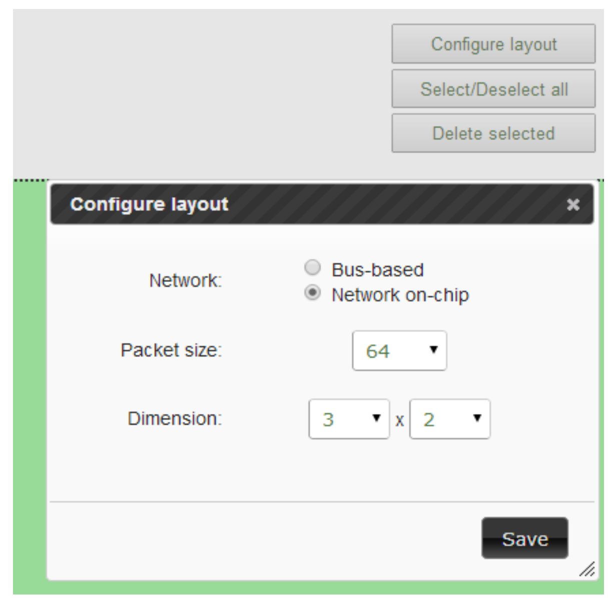
Integrating Optical Network on chip Models to an existing System-Level Platform

- Hellfire GUI and









The next step

- Research is technology-dominated
  - Physical level research
  - New devices and architectures are defined
- System-level vision required
  - Optical engineers
  - Computer engineers
  - Computer scientists
- Multi-disciplinary project

The next step

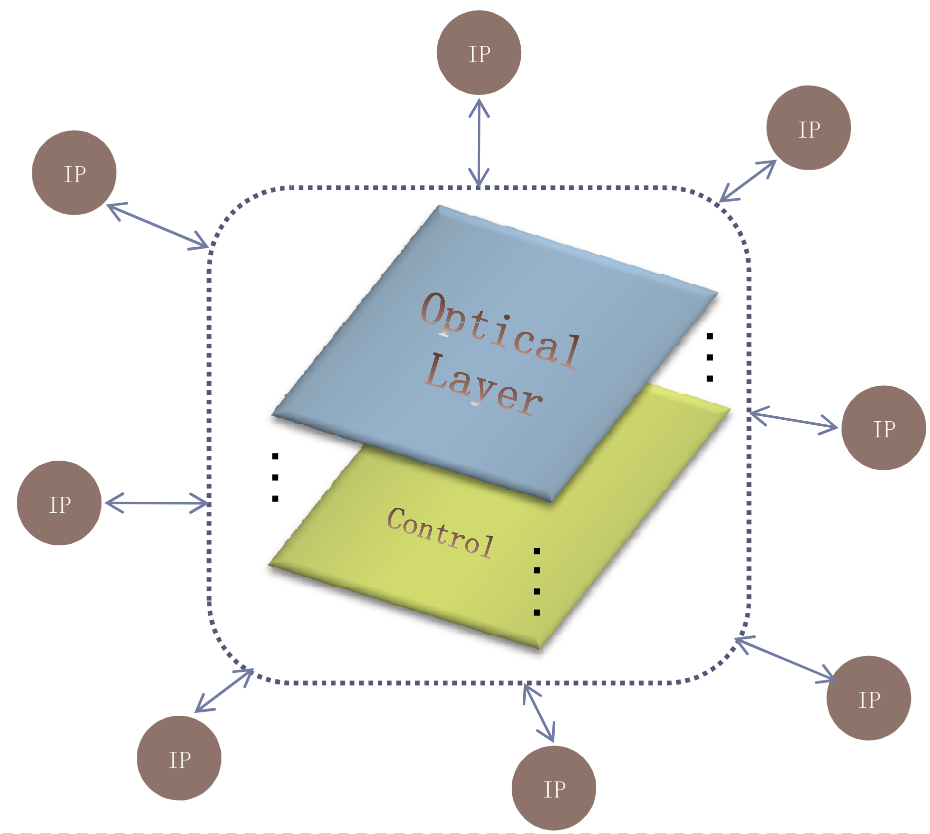
- Nowadays describing methods are well suited for optical components
  - Focus on improving those methods for better express the interactions for an entire system
- Extend available tools in order to provide real-time feedback
  - Available models don't work well on real case scenarios, not expressing variations, like cross-talk and heating dissipation
- Speed X Accuracy
  - Find a reliable and yet computationally feasible method for measuring dynamic system variations

The next step

- Final Goal
  - Provide a tool for the complete design of Optical-based MPSoCs
    - Library of switches, routers and pre-defined networks
    - Dynamic behaviour of components and devices
    - High-speed simulator
    - High-level programming support through an embedded OS

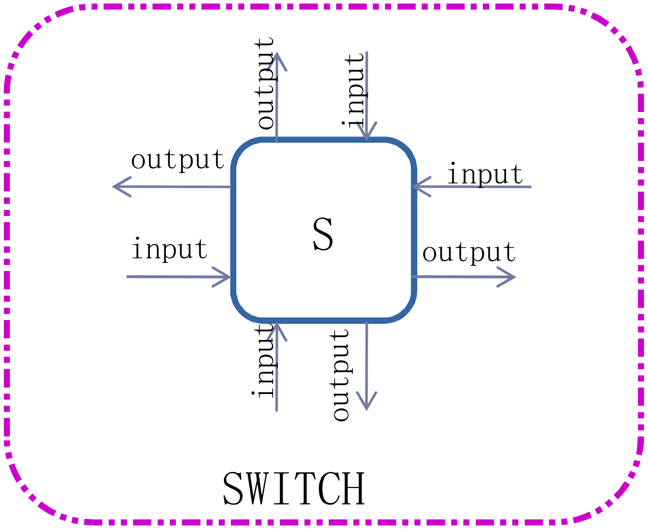
Work in progress

- Optical Network simulator
  - Based on a in-house network model
  - Connects eight IPs
  - Composed by five MZI-based switches
  - Electronic control layer



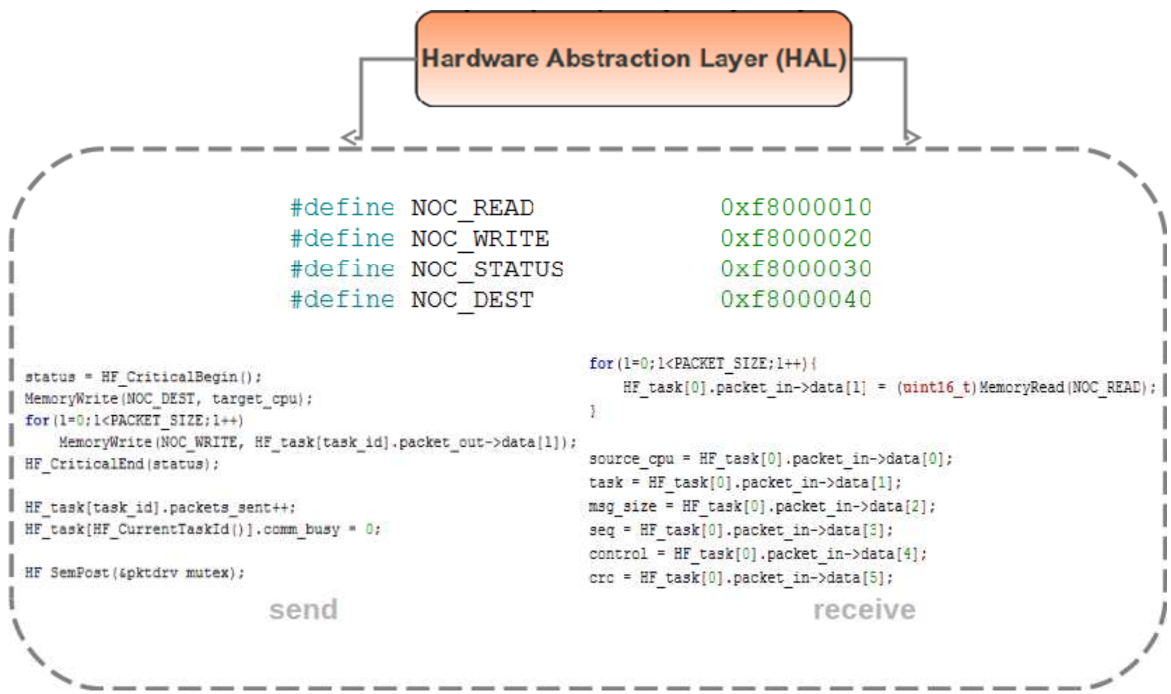
Work in progress

- MZI-based switch
  - 4x4 switch
  - Prototyped for data extraction
  - Low delay design (20 ps)
  - Wavelength based switching
  - Allows simultaneous communications on all ports



Work in progress

- Network modeled in RLT level (VHDL)
- Integrated with a MIPS-like processor
- High-level support available through HFOS



Work in progress

- Network + HFOS

```
void task_send(void){
    uint8_t buf[30] = "hello!";
    uint16_t dest = HF_CurrentCpuId() + 1;

    while(1){
        HF_Send(dest, 2, buf, sizeof(buf));
        printf("\nnode %d to node %d", HF_CurrentCpuId(), dest);
        HF_TaskYield();
    }
}
```

```
==========================================================================
Welcome to the HF-RISC Bootloader - Apr 24 2014 19:49:47
Embedded Systems Group - GSE, PUCRS - [2006 - 2014]
==========================================================================
===============================================================
HellfireOS RT Lite v1.4
Jun 19 2014, 17:04:34 (gcc 4.6.1)
Embedded Systems Group - GSE, PUCRS - [2007 - 2014]
===============================================================
CPU ID:                 1
Architecture:           HF-RISC
Clock frequency:        25000 kHz
System tick time:       10485 us
TCB entry size:         224 bytes
TCB size:               1120 bytes
Heap size:              65535 bytes
Packet buffer size:     128 flits in sw FIFOs (each task), 32 flits in /
out hw FIFOs
Message delivery:       no ack
Maximum tasks:          5
*
node 1 to node 2
node 1 to node 2
node 1 to node 2
node 1 to node 2
node 1 to node 2
node 1 to node 2
```

```
void task_recv(void){
    uint16_t source_cpu;
    uint8_t source_id;
    uint16_t size;
    uint8_t buf[31];

    while(1){
        HF_Receive(&source_cpu, &source_id, buf, &size);
        printf("\nthread %d -> message from node %d thread %d size %d -> %s"
        , HF_CurrentTaskId(), source_cpu, source_id, size, buf);
        HF_TaskYield();
    }
}
```

```
==========================================================================
Welcome to the HF-RISC Bootloader - Apr 24 2014 19:49:47
Embedded Systems Group - GSE, PUCRS - [2006 - 2014]
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===============================================================
HellfireOS RT Lite v1.4
Jun 19 2014, 17:04:36 (gcc 4.6.1)
Embedded Systems Group - GSE, PUCRS - [2007 - 2014]
===============================================================
CPU ID:                 2
Architecture:           HF-RISC
Clock frequency:        25000 kHz
System tick time:       10485 us
TCB entry size:         224 bytes
TCB size:               1120 bytes
Heap size:              65535 bytes
Packet buffer size:     128 flits in sw FIFOs (each task), 32 flits in /
out hw FIFOs
Message delivery:       no ack
Maximum tasks:          5
*
thread 2 -> message from node 1 thread 2 size 30 -> hello!
thread 2 -> message from node 1 thread 2 size 30 -> hello!
thread 2 -> message from node 1 thread 2 size 30 -> hello!
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thread 2 -> message from node 1 thread 2 size 30 -> hello!
thread 2 -> message from node 1 thread 2 size 30 -> hello!
```

CONCLUSIONS

- Standard NoC implementations shows important drawbacks
- Optical-NoC cames as a possible solution
- Design methods for basic devices well matured
- Lack of tools for system-level design
- Extension of HFFW

Multi-disciplinary Project Team

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