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DESIGN, AUTOMATION & TEST IN EUROPE
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The European Event for Electronic System Design & Test

The Last Mile?
Remaining Challenges in Optical Interconnect

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My life with optical interconnect

Analog Integrated Circuits and Signal Processing, 29, 37–47, 2001

Behavioral Modeling and Simulation of Optical Integrated Devices

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"On-chip optical interconnect could become reality in five years" (I. O'Connor, 2001)

Design Automation and Test in Europe, Grenoble, France, 9-13 March 2015

Thermal Aware Design Method for
VCSEL-based On-Chip Optical Interconnect

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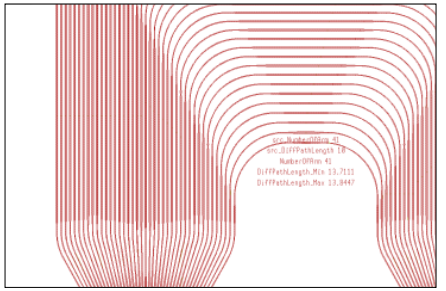
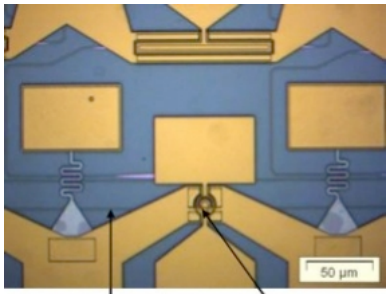
"On-chip optical interconnect could become reality one day" (I. O'Connor, 2015)

Challenges at the physical level

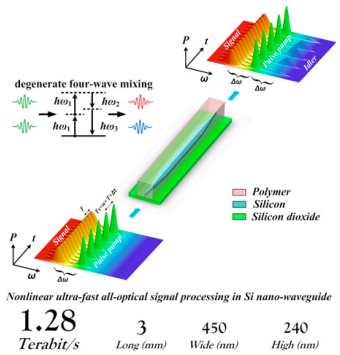
- **Physical design tools**
  - Curvilinear structures
  - Structure-functionality entanglement
- **Source integration strategy**
  - Off-chip source + on-chip modulators
  - On-chip sources + direct modulation
- **Information coding strategy**
  - Level-based coding
  - Pulse-based coding
- **Silicon real estate**



Source: Mentor Graphics



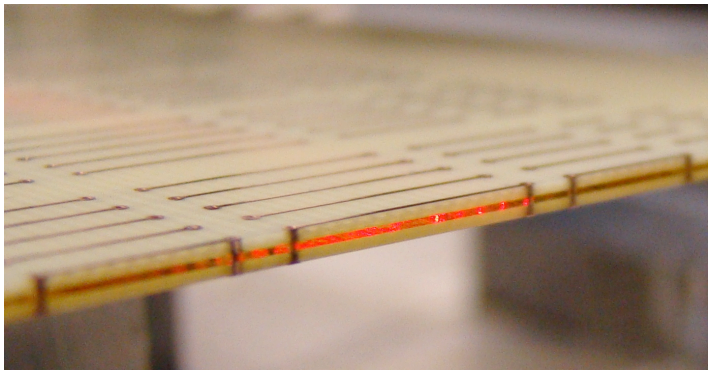
Source: INL



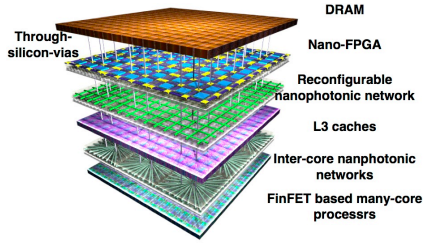
Source: Technical University of Denmark

Challenges at the system level

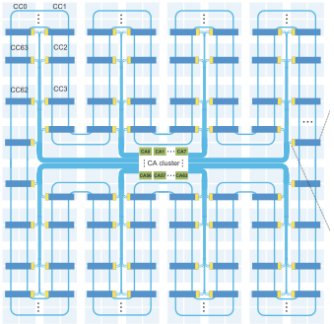
- **Scale of integration**
  - Optical I/O
  - 3D interposers
  - On-chip interconnect
- **Simulation and design tools**
  - Vector-based optical signals
  - Heterogeneous system
- **Network topology**
  - One size fits all (ring? mesh?)
  - Adapting to requirements
  - Intelligence in the routing
- **Killer application + ecosystem**



Source: Fraunhofer



Source: University of Colorado at Boulder



Source: HKUST

Challenges due to thermal variations

- Heavy focus on wavelength-routing architectures
  - Wavelength-resonance and source efficiency depend on temperature
  - Thermal variations can lead to severe loss of functionality
  - Compensation techniques
    - Overhead: power and silicon real estate
- Alternative?
  - Spatial multiplexing
  - Multiple parallel waveguides to bundle signals in point-to-point links with no wavelength routing
  - Clear area penalties

Thermal tuning

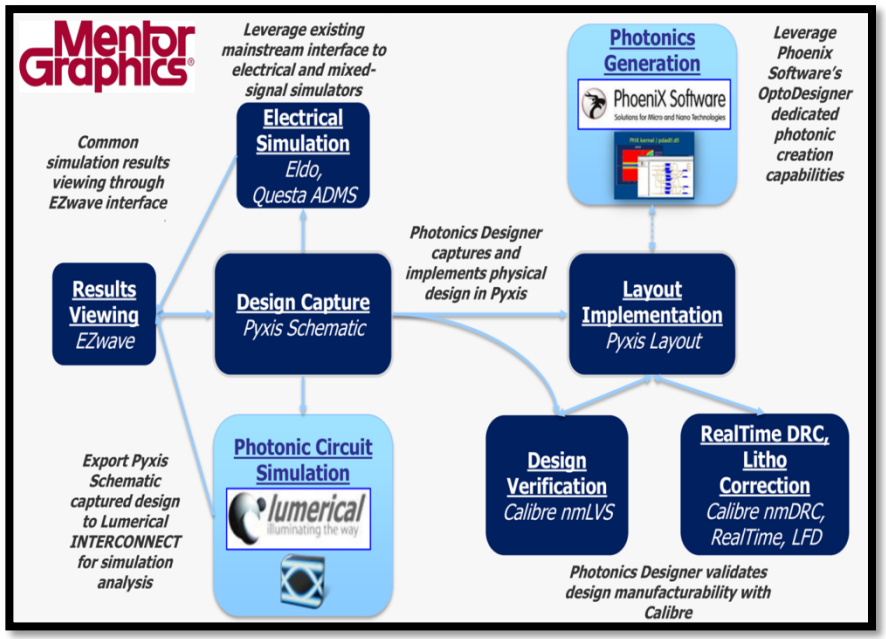
Panel

- ***In your view, what is the most significant challenge to overcome before widespread adoption of optical/photonic interconnects for computing systems, and why ?***
- **Panelists:**
  - **John Ferguson, Mentor Graphics Corp, US**
  - **Antonio La Porta, IBM, Zurich Research Laboratory, CH**
  - **Davide Bertozzi, University of Ferrara, IT**
  - **Jiang Xu, Hong Kong University of Science and Technology, CN**
  - **Olivier Sentieys, INRIA - University of Rennes 1, FR**
  - **Gabriela Nicolescu, Ecole Polytechnique de Montreal, CA**

John Ferguson

Dedicated Photonics Custom Design Platform

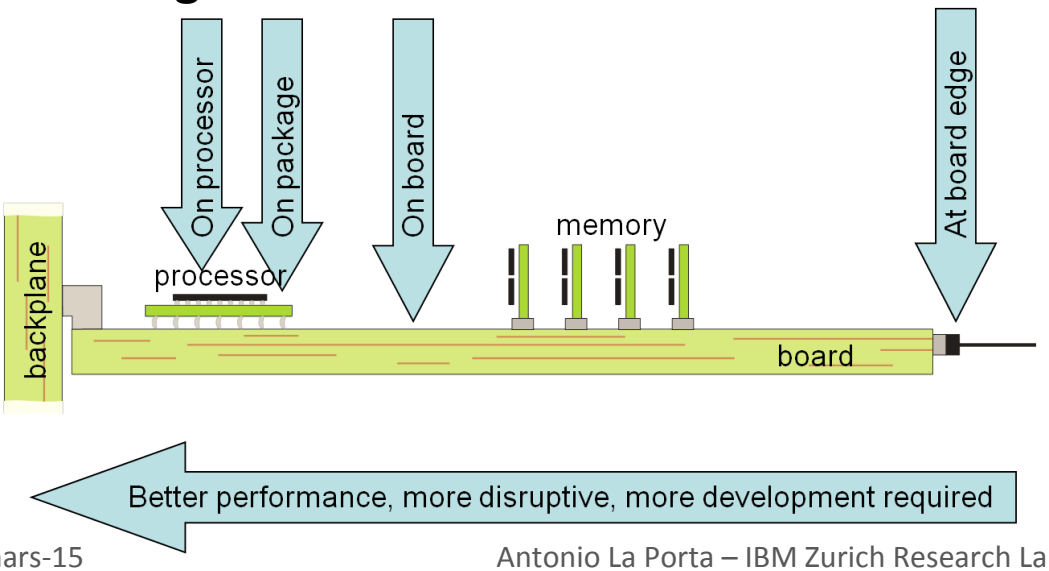
- Mentor Graphics
  - *Pyxis Custom*: schematic, layout, simulation
  - *Calibre:* industry standard PV and DFM
- Lumerical Solutions – OpenDoor partner
  - *INTERCONNECT:* time and frequency domain photonic circuit simulation
- PhoeniX Software– OpenDoor partner
  - *OptoDesigner:* layout generation of advanced photonics structures



- Design tools alone are not enough
  - Qualified PDK's are required

Antonio La Porta

- Higher level of photonic functionality integration
  - What it really means for computer systems:
    - System- or chip-level? Co-package of what with what? Hybrid or monolithic integration?
  - How and where to bring the optics?
    - For each scenario, what do we really gain?



IBM's "Sequoia" BlueGene/Q @ LLNL

Davide Bertozzi

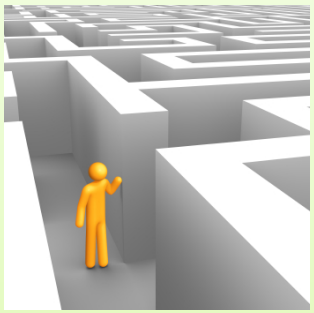
Companies will do their best to resist the change...

Hey, it's an expensive technology!

We are very good at further optimizing electronics!

However there are early signs that they will be stuck in the middle of a labyrinth...

- *Need to move more data through pin-limited chip interfaces*
- *Need to move more and more data through IP core interfaces on the chip*



...with no easy way out (i.e., out-of-reach for electronics)

- Wider flit-width ENoCs will soon incur routing congestion, in addition to significant area/seq. Power overhead
- At 4/5 hops (2mm each) in the ENoC, ONoCs already achieves the energy breakeven point at 0.6pJ/bit in 40nm

Historically, whenever optical links succeed in delivering superior point-to-point connections, penetration into the switching fabric is the next step

Once there, we should be ready to deliver companies what they actually need:

- ✓***Design methodologies and synthesis toolflows with cross-layer optimizations: it's time!***
- ✓***EDA can lead to concrete evaluations of new technologies***
- ✓***Gating methods for optical components to alleviate the static power concern***
- ✓***Rethink the system architecture: e.g., no NUMA effects, how to partition and reconfigure,..***

However the good news is that today industry is on the watch for this new technology

A Different "Building Material"

Stone
Solkan Bridge
Slovenia 1906

Steel
Cold Spring Bridge
USA 1963

Steel
Tsing Ma Bridge
Hong Kong 1997

- **Pros**
  - **High bandwidth**
  - **Low propagation delay**
  - **Low propagation loss**
  - **Low sensitivity to environmental EMI**
- **Cons**
  - **Crosstalk noise**
  - **Thermal sensitivity**
  - **Process variation**
  - **Electrical/optical conversion overheads**
  - **Optical signals are difficult to "buffer"**

Differences bring both challenges and opportunities

Olivier Sentieys

Computer architect's point of view

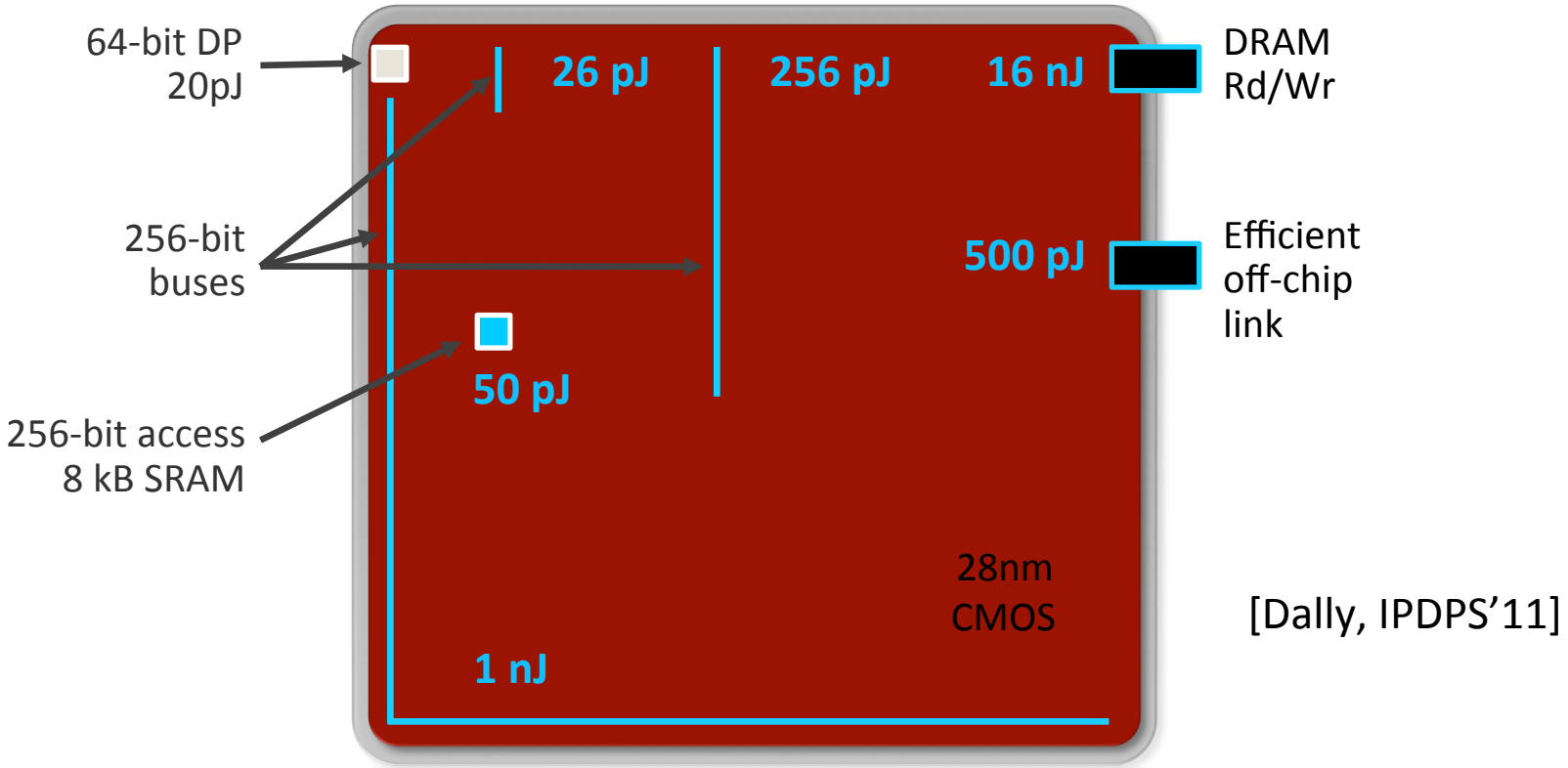
- Are we really bandwidth-limited for on-chip communications?
  - Not really true in current computer architectures
  - But big data will maybe change the game
- What are the big challenges?
  - Amdhal's law
    - Even with 95% of parallel code, speedup ***S < 20***

$$S(N) = \frac{1}{(1-P) + \frac{P}{N}}$$

  - **Power!**
    - Energy efficiency is not scaling along with integration capacity
    - Data movement costs more than computing
- So maybe **energy efficiency** is the real challenge

The Energy Cost of Data Movement

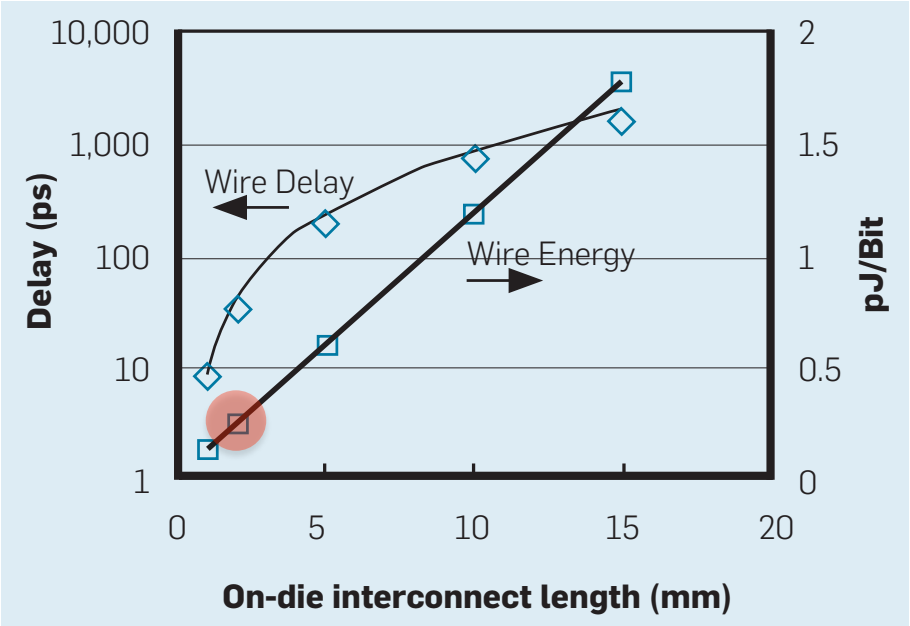
- **Fetching operands costs more than computing**



[Dally, IPDPS'11]

The Energy Cost of Data Movement

- Future processor up to 3 Tera-op/sec
- At minimum requires 64b x 9 Tera-operands to be moved each second
- If on average 1mm (10% of die size) then
  - 0.1pJ/bit x 576 Tbits/s
  - consumes 58 Watts!



Gabriela Nicolescu

Challenge for Optical Interconnect Adoption

Outstanding solutions & tools

Cross-cutting challenge:
multi-scale, multi-technology and multi-domain models