Inter/Intra-Chip Optical Networks

Opportunities & Challenges

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Acknowledgement

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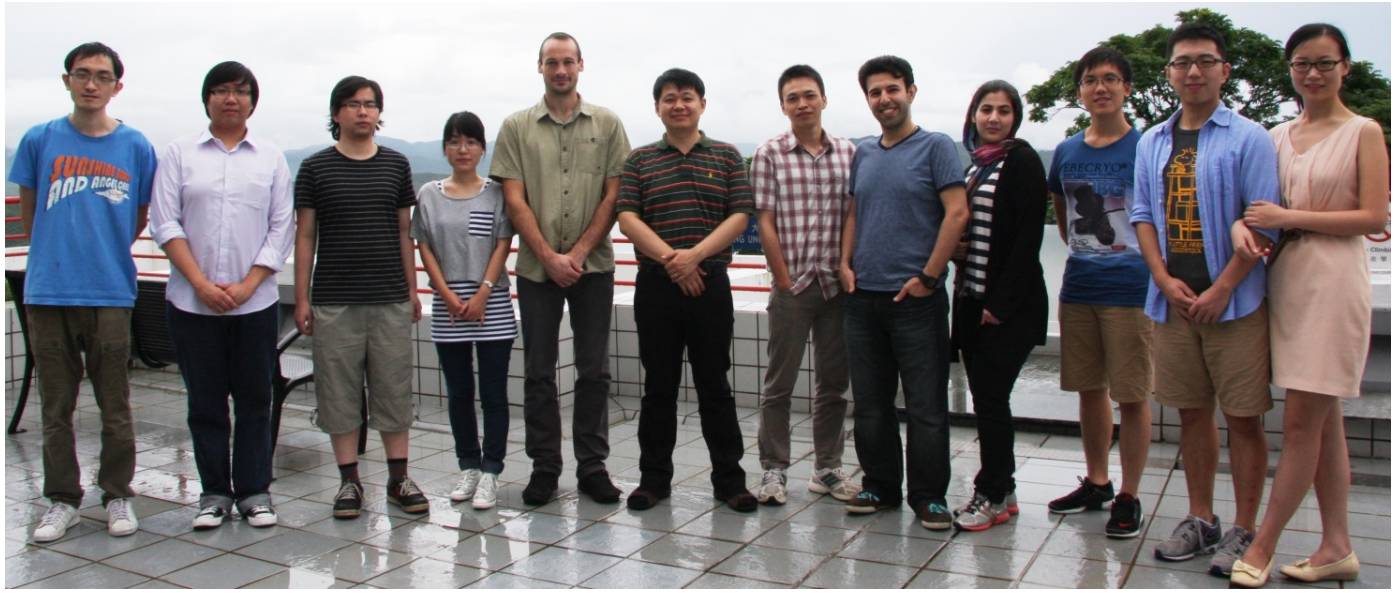

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intel

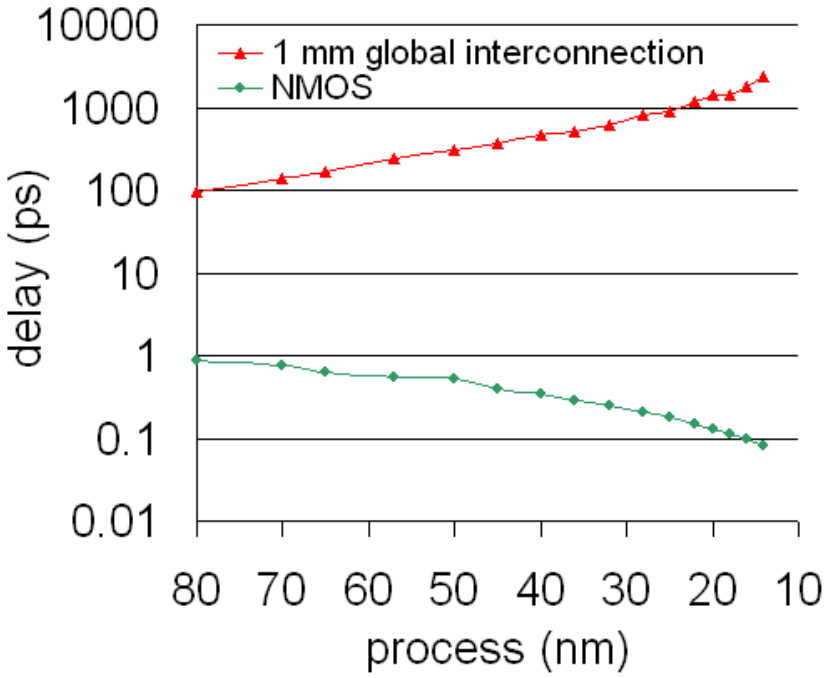
XILINX

HUAWEI

Performance and Power Wall of Electrical Interconnects

- More cores require more communications
  - Hundreds of cores on a single chip
  - Cisco QuantumFlow (40), Intel Phi (61), Tilera Tile (72), Cisco SPP (188), PicoChip (300) …
- Higher power consumption
  - Dynamic and leakage power of drivers and buffers
  - Kilowatts of power by 2020*
- Larger latency
  - Multiple clock cycles are required to cross a chip
- Tighter chip I/O bandwidth
  - High pin count, packaging cost, and expensive PCB design

Year	2015	2020	2025
MP process (nm)	25	13	7
Clock (GHz)	4.4	5.3	6.5
Transistor (billion)	3.1	12	49

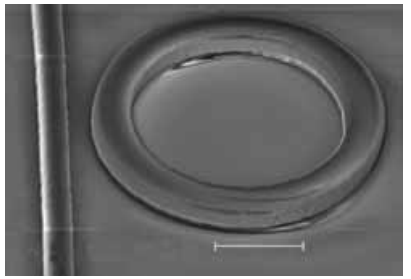


*R.G. Beausoleil, *et al.*, "Nanoelectronic and Nanophotonic Interconnect," Proceedings of the IEEE, Feb. 2008.

** Based on ITRS2012 update

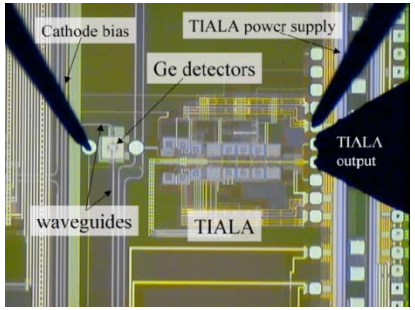
Optical Interconnects

- Photonic technologies have been successfully used in WAN, LAN, and board level
  - Showed strengths in multicomputer systems and Internet core routers
- Base on waveguide and microresonator (MR)
  - Silicon based and CMOS compatible
  - MR is as small as 3μm in diameter
  - 30ps switching time has been demonstrated
- Commercialization efforts
  - Demonstrated by IBM, Intel (Omni-Scale), HP (Machine), NEC, Fujitsu, Oracle (UNIC/DARPA), NTT, STMicro, Huawei …
  - Startups: Luxtera, Lightwire/Cisco, Kotura/Mellanox, Caliopa/Huawei, Aurrion, OneChip, Skorpios …



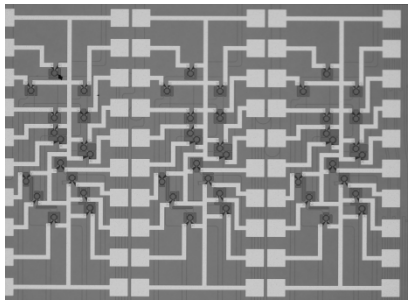
Silicon-based Waveguide and MR

R. G. Beausoleil *et al.*, "A Nanophotonic Interconnect for High-Performance Many-Core Computation", IEEE LEOS June 2008



Integrated EO and OE Interfaces

G. Masini, *et al.*, "A 1550nm 10Gbps monolithic optical receiver in 130nm CMOS with integrated Ge waveguide photodetector", IEEE International Conference on Group IV Photonics, 2007



On-Chip Optical Routers

R. Ji, J. Xu, L. Yang, "Five-Port Optical Router Based on Microring Switches for Photonic Networks-on-Chip", IEEE Photonics Technology Letters, March, 2013

Fundamentally Different "Building Material"

- Advantages
  - Ultra-high bandwidth
  - Low propagation delay
  - Low propagation loss
  - Low sensitivity to environmental EMI
- Disadvantages
  - Thermal sensitivity
  - Crosstalk noise
  - Process variations
  - Electrical/optical conversion overheads
  - Optical signals are difficult to "buffer"
- Differences bring new opportunities and challenges

Stone
Solkan Bridge
Slovenia, 1906

Steel
Cold Spring Bridge
USA, 1963

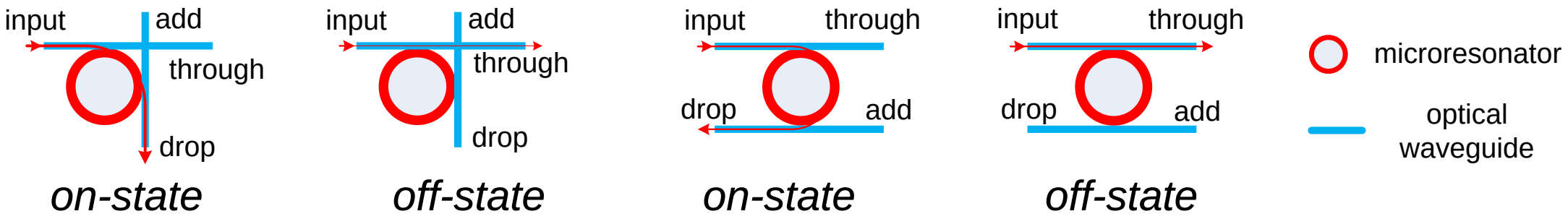
Steel
Tsing Ma Bridge
Hong Kong, 1997

Outline

- Introduction
- Optical Routers
- Unified Inter/Intra-Chip Optical Network
- Thermal Modeling
- Optical Crosstalk Noise Analysis
- Open-Source Research and Development Tools
- Summary

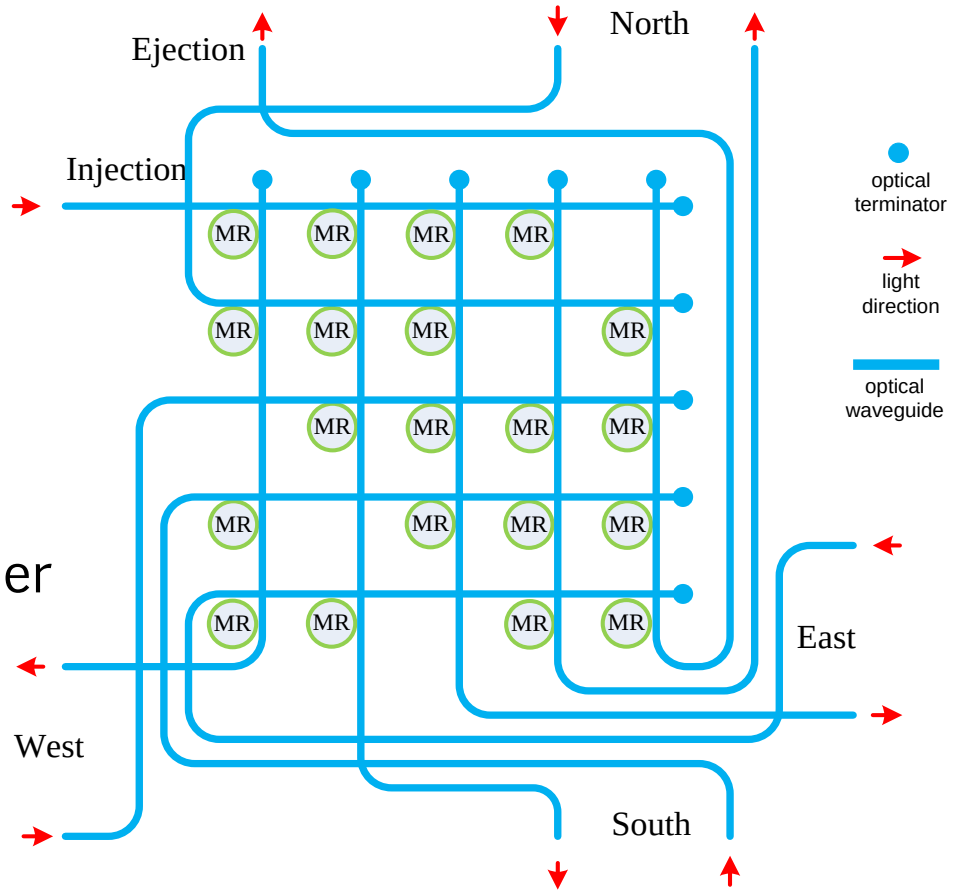
Basic Optical Switching Element (BOSE)

- Two types of 1x2 BOSEs
  - Crossing element and parallel element
  - Both composed of an MR and two optical waveguides
- Crossing element can be considered as a parallel element plus a waveguide crossing
  - And hence additional crossing insertion loss
- Optical components are still in the range of microns
  - Minimizing the number of MRs is necessary



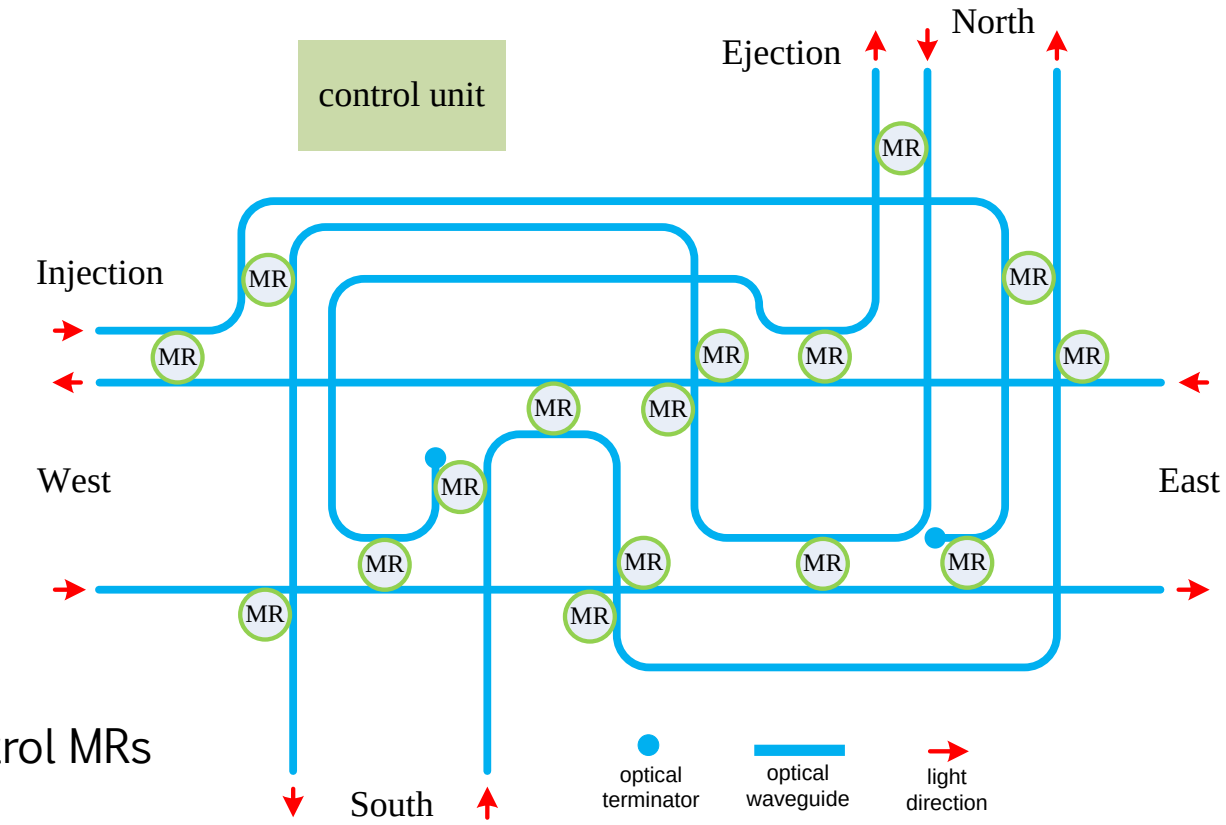
Optimized 5x5 Optical Crossbar

- For mesh and torus based optical NoCs
- Ports are aligned to intended directions
- No U-turns
- 20 MRs and 10 terminators
- Many waveguide crossings
  - Cause large loss in a network, on average 1.08dB loss per router
- Could we do better?
  - Reduce optical power loss
  - Use less MRs and terminators

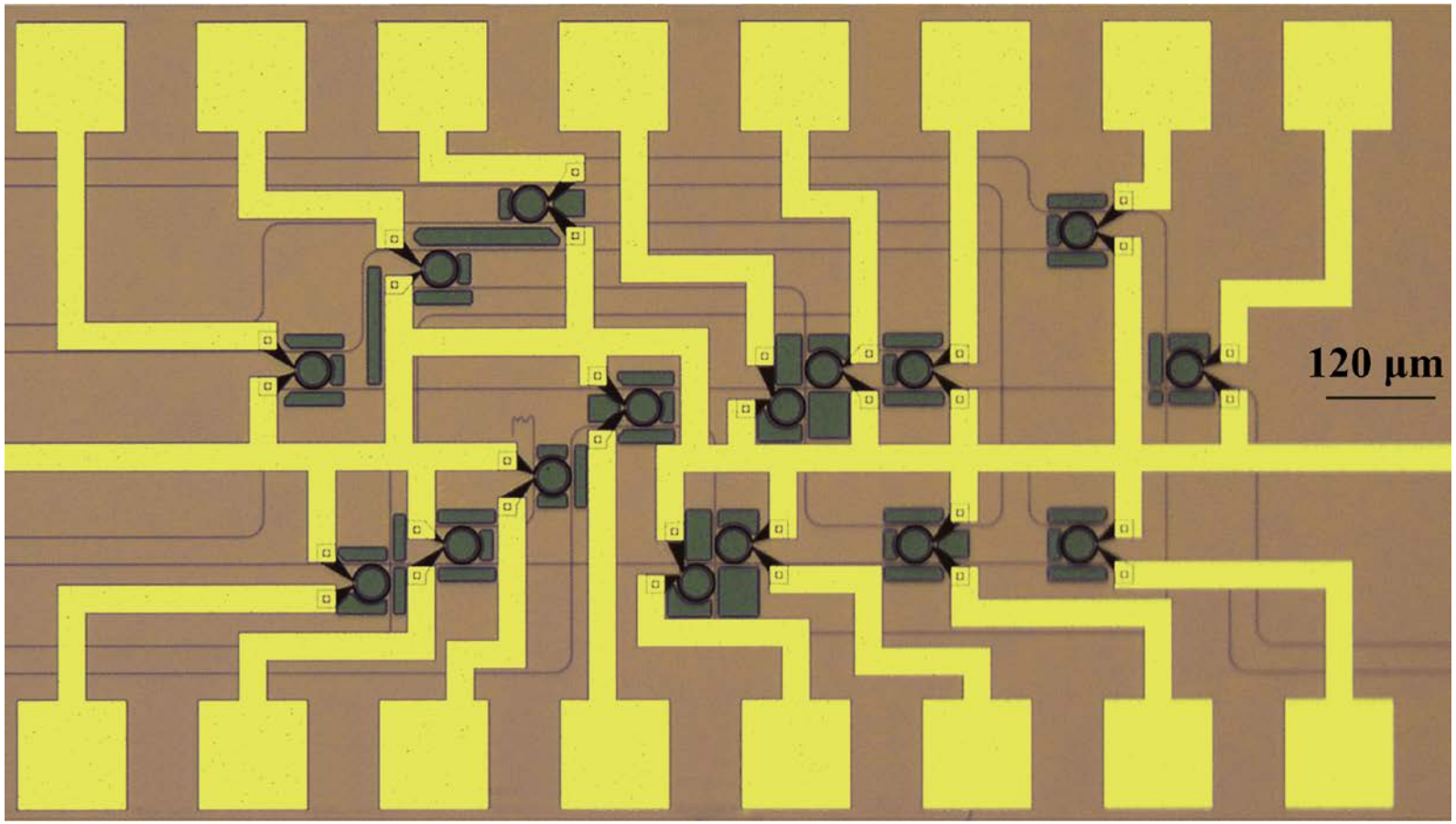


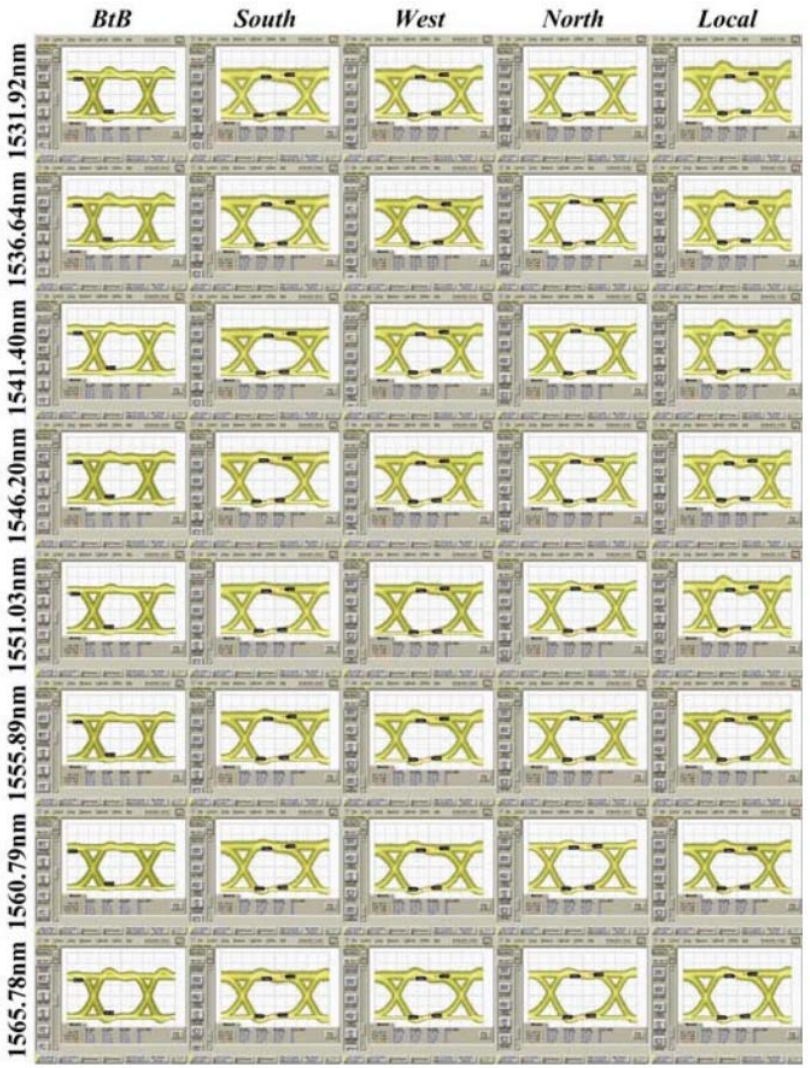
Cygnus Optical Router

- 5x5 switching function
- Strictly non-blocking
  - Support any routing algorithm
- Ports are aligned to intended directions
- Switching fabric
  - Minimized crossing and MRs
  - Only 16 MRs and 2 terminators
- Control unit
  - Implement routing algorithm and electronically control MRs
- Special feature
  - Passively rout packets between ports in the same dimension



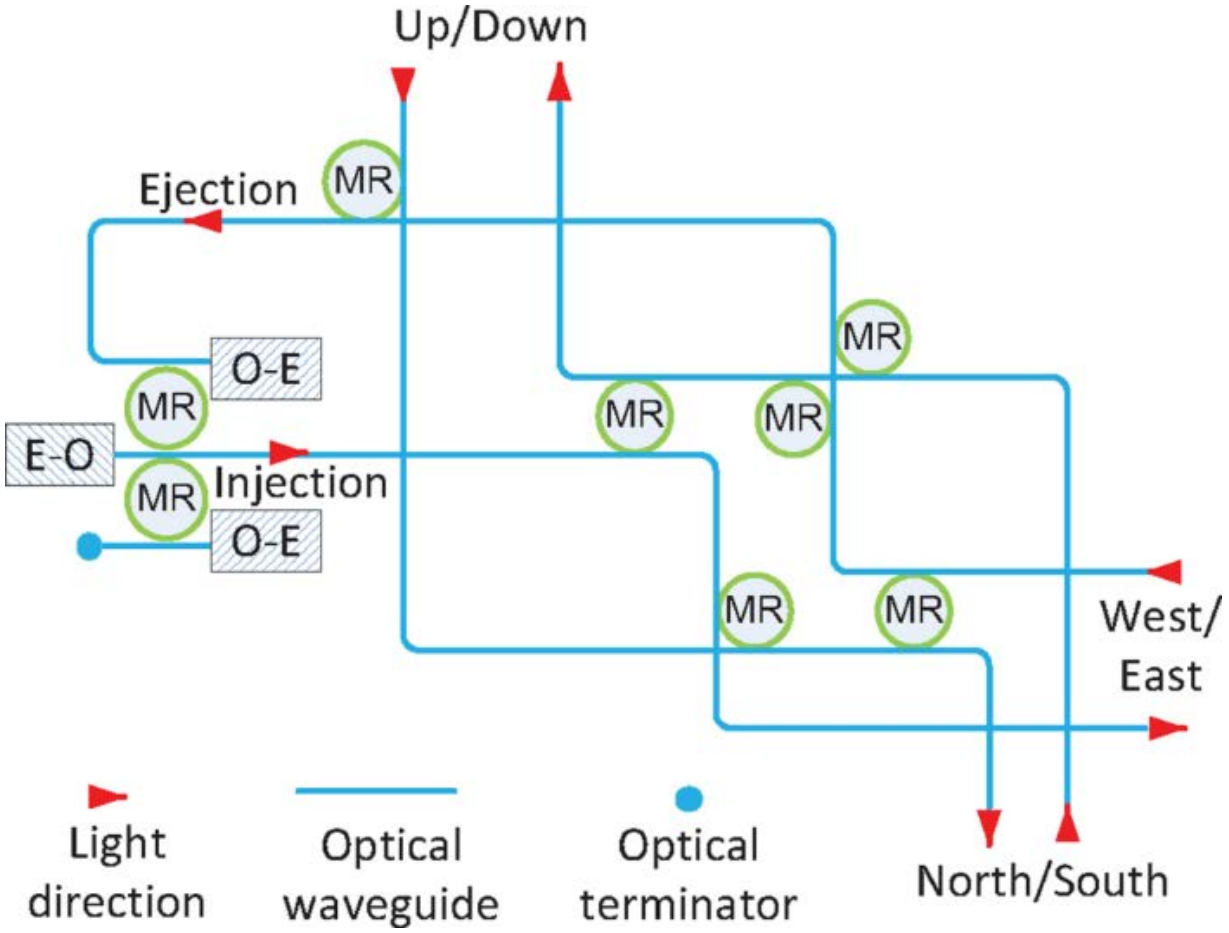
Implementation and Testing



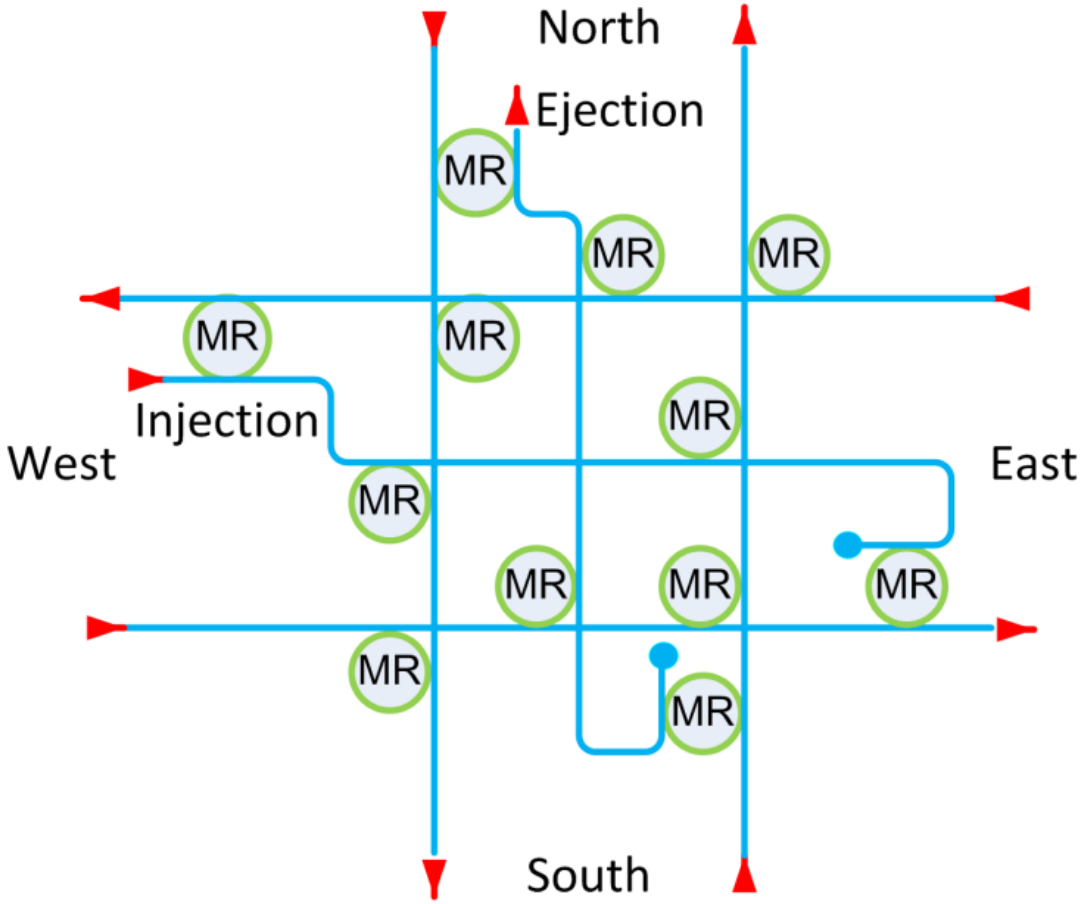


* Ruiqiang Ji, Jiang Xu, Lin Yang, “Five-Port Optical Router Based on Microring Switches for Photonic Networks-on-Chip”, IEEE Photonics Technology Letters, March 2013

More 4x4 and 5x5 Optical Routers

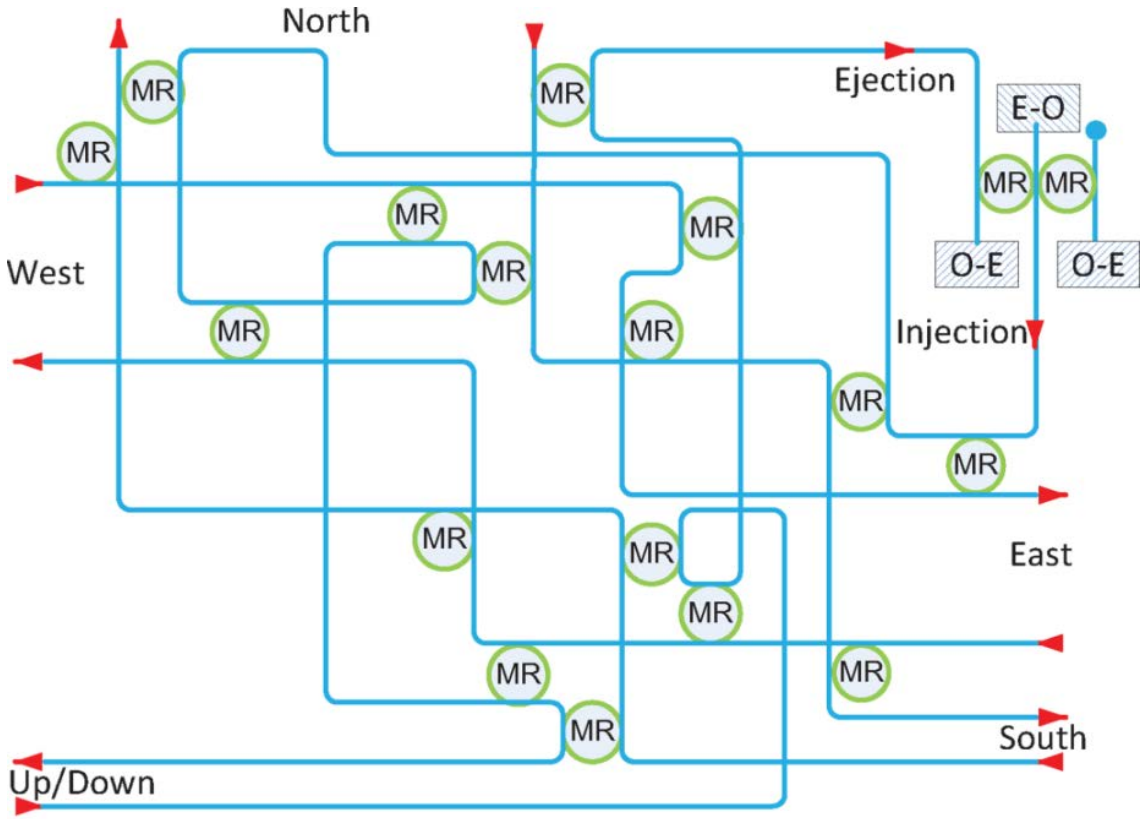


4x4 optical router

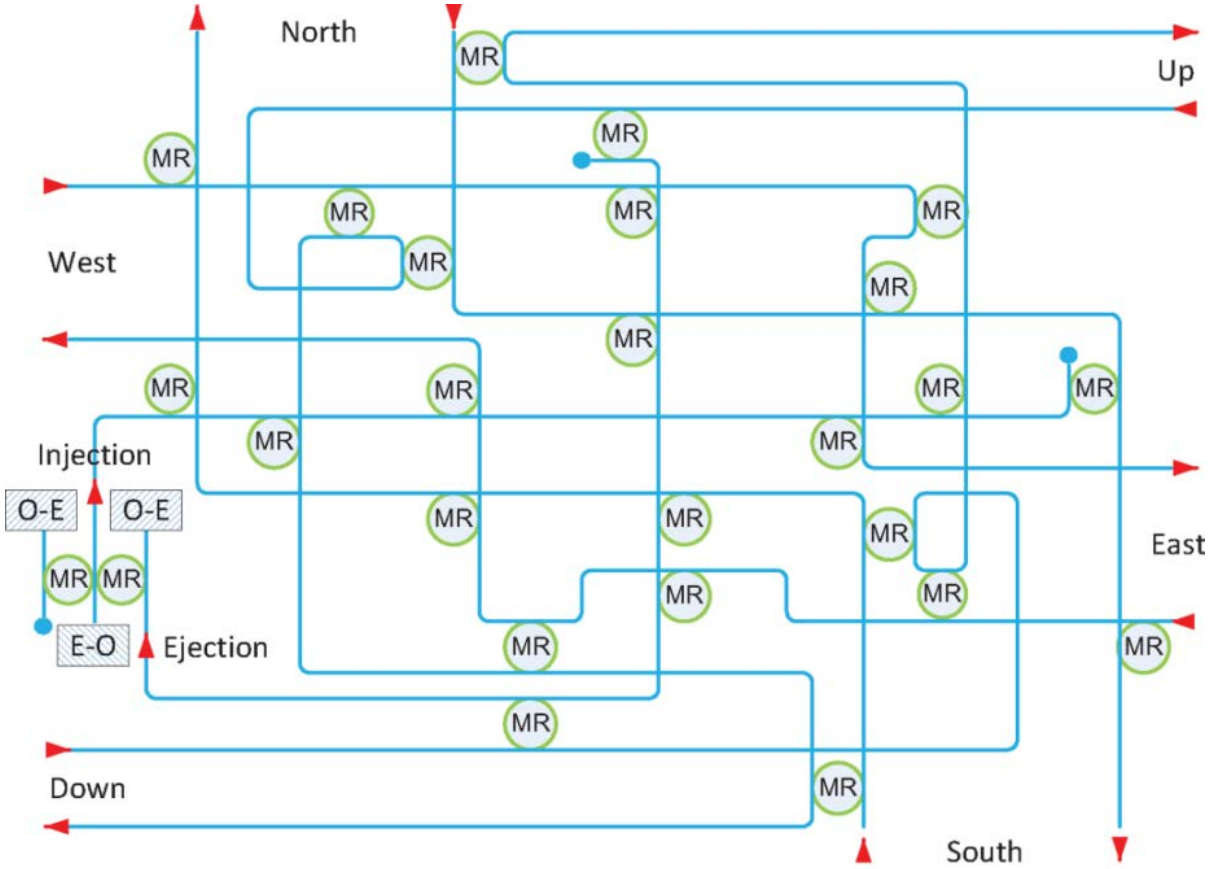


Crux optical router

6x6 and 7x7 Optical Routers



6x6 optical router



7x7 optical router

Optical Router Comparison

	Cygnus	Crux	OXY	ODOR	[14]	[15]	[16]	[17]
Routing algorithm	Arbitrary	XY routing	XY routing	XY routing	Arbitrary	Arbitrary	Arbitrary	XY routing
Nonblocking	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
Passive routing	Yes	Yes	Yes	Yes	No	No	No	Yes
N_{MR}	16	12	12	12	20	16	15	12
$N_{Terminator}$	2	2	2	5	10	2	0	2
$N_{Crossing}$	13	9	11	19	26	14	15	12
$L_{average}$	0.78dB	0.64dB	0.73dB	0.87dB	1.15dB	0.87dB	0.77dB	0.96dB

[14] A. Poon, *et al.* "Cascaded microresonator-based matrix switch for silicon on-chip optical interconnection," *IEEE Proceedings, 2009.*
[15] R. Ji, *et al.* "Five-port optical router for photonic networks-on-chip," *Optical Express,* Oct 2011.
[16] R. Min, *et al.* "Scalable non-blocking optical routers for photonic networks-on-chip," *IEEE Optical Interconnects Conference*, 2012.
[17] J. Chan, *et al.* "Physical-layer modeling and system-level design of chip-scale photonic interconnection networks," *IEEE TCAD,* 2011.

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- Thermal Modeling
- Optical Crosstalk Noise Analysis
- Open-Source Research and Development Tools
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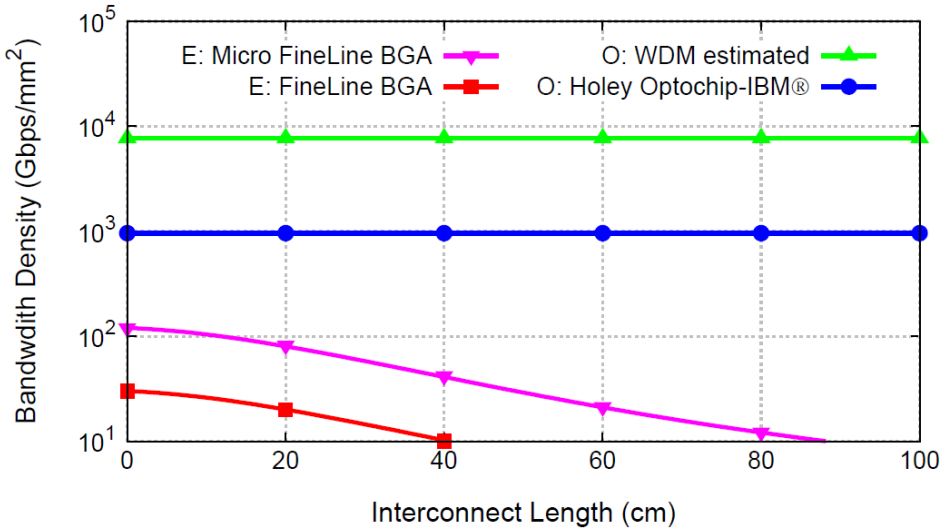
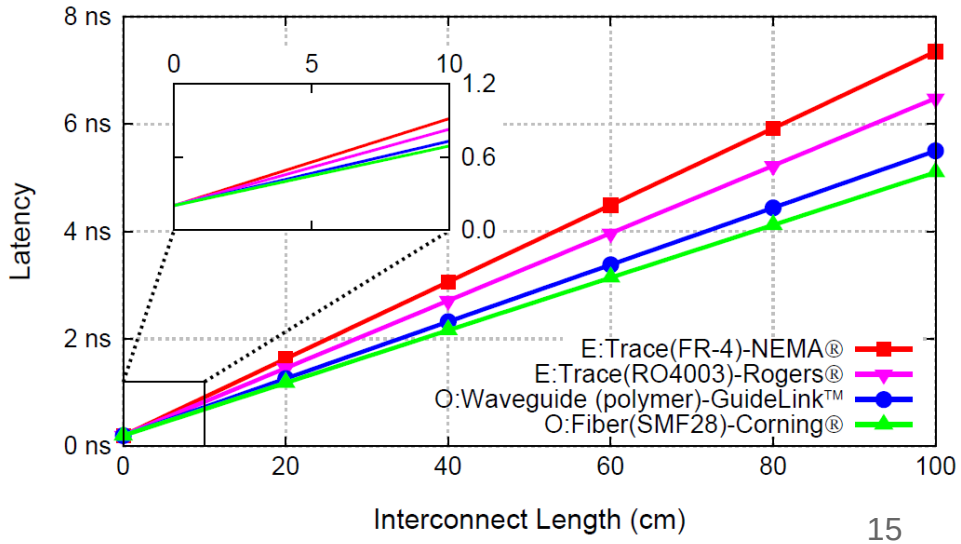
Codesign Inter/Intra-Chip Communication Architecture

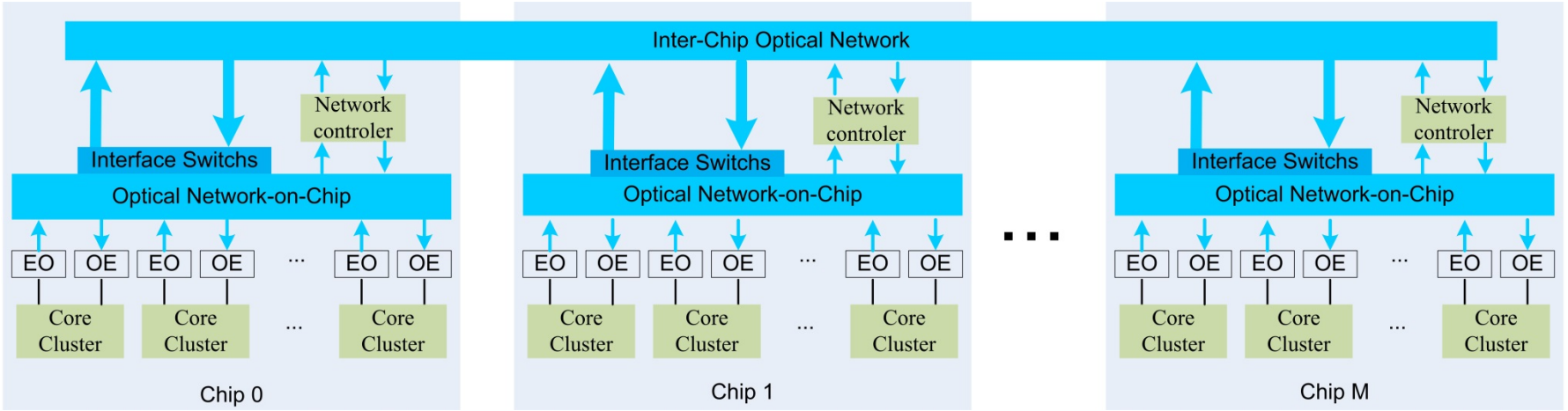
- Inter- and intra-chip CMAs based on electrical interconnects are separately designed
  - Limited and expensive chip I/Os create a sharp chip boundary
  - Different on-chip and on-board constraints
  - Maximize design flexibility and allow third-party system integration
- We estimate optical interconnects can offer 10X~100X chip I/O bandwidth than electrical chip pins*
- Jointly design inter/intra-chip CMAs could potentially take the full advantage of optical interconnects
  - Reduce buffering and large E/O conversion overheads





* Zhehui Wang, Jiang Xu, *et al.*, "Alleviate Chip I/O Pin Constraints for Multicore Processors through Optical Interconnects", ASP-DAC 2015.

UNION: Unified Inter/Intra-Chip Optical Network

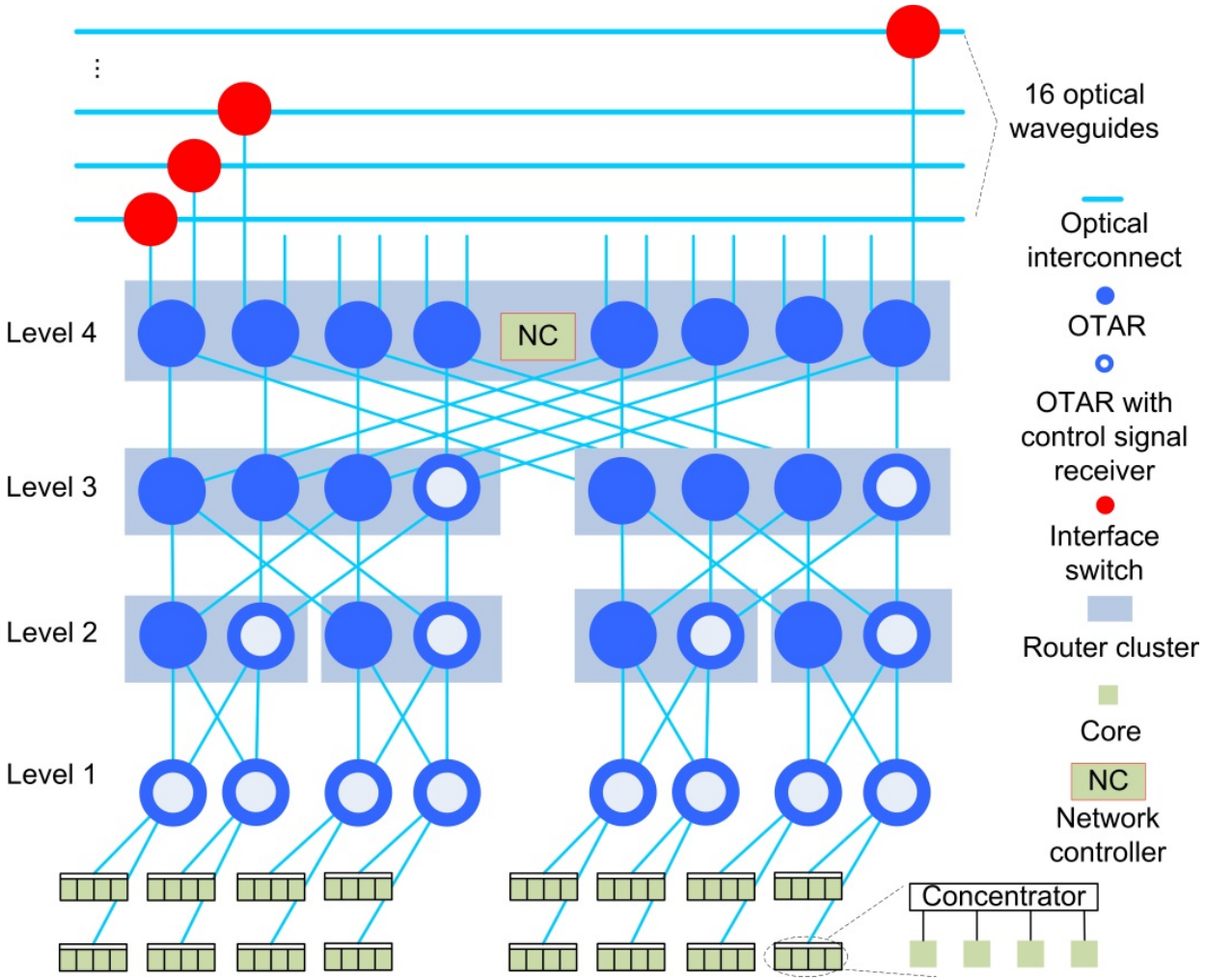


- Hierarchical optical network for multiple chips
- Optical network-on-chip (ONoC) is the intra-chip network
- Inter-chip optical network (ICON) collaborates with ONoC to handle inter-chip traffic
- Payload and control packets share the same optical network

* Xiaowen Wu, Yaoyao Ye, Jiang Xu, *et al.*, "UNION: A Unified Inter/Intra-Chip Optical Network for Chip Multiprocessors", IEEE TVLSI 2013

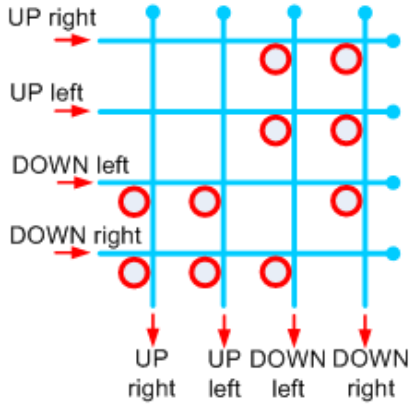
Fat Tree based ONoC

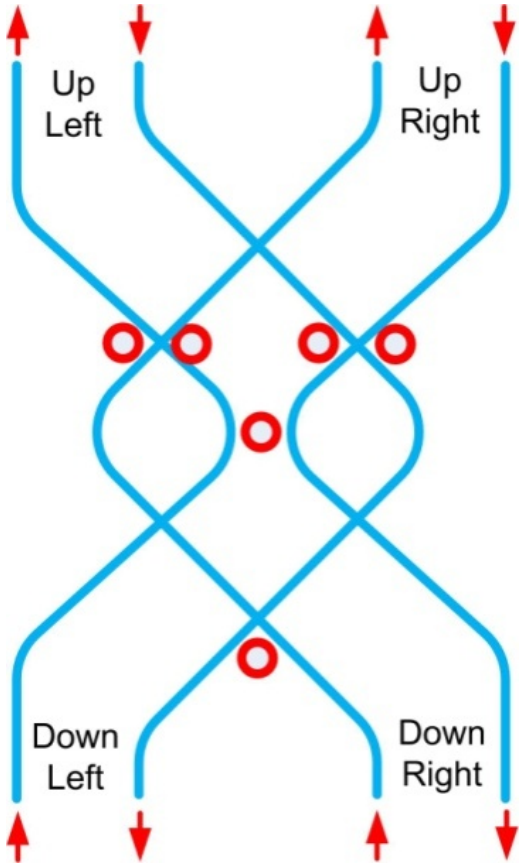
- A *k*-core chip uses an *l*-level tree
  - Electronic concentrator connects four cores
  - Routers are grouped into router clusters
  - $l = \log_2(k/4)$ network levels
  - $(k/8)\log_2(k/4)$ optical routers
  - k/4 crossbar-based concentrators
- Use turnaround routing algorithm
  - Centralized control decision but distributed execution
- Dynamic optical power control
  - Adjust EO interface power based on different optical paths
  - Lasers are off when ideal



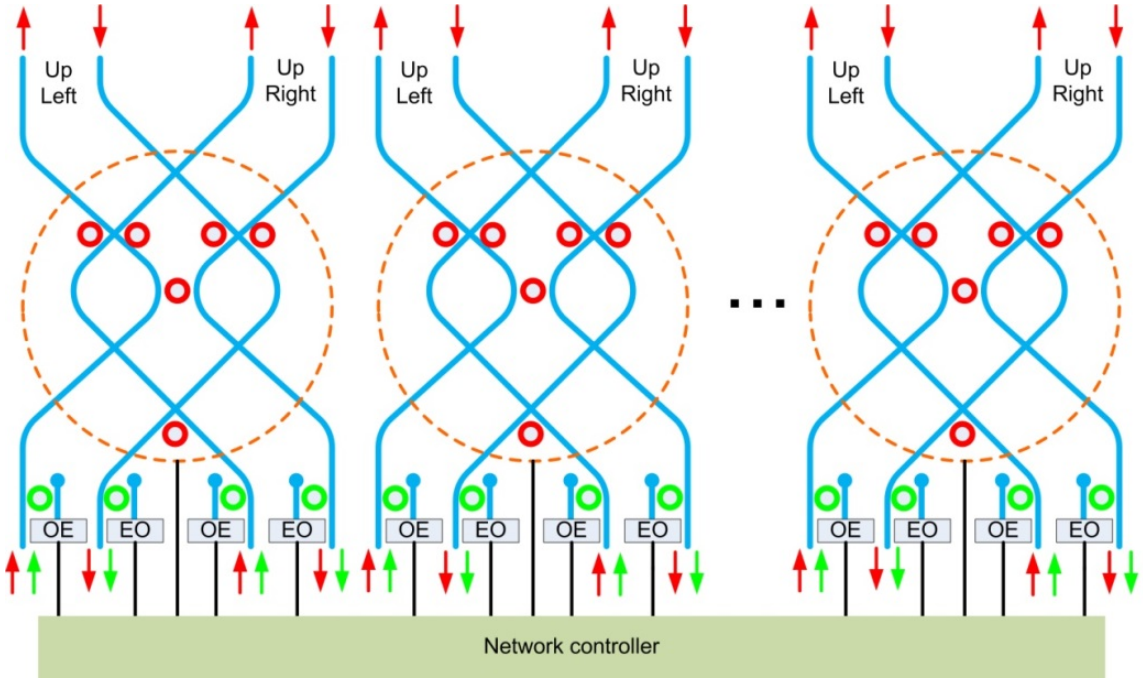
Optical Turnaround Router (OTAR)

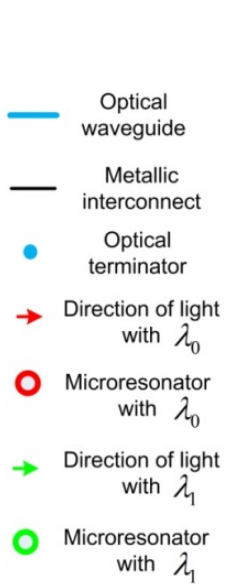
- 4x4 switching function
- Strictly non-blocking for turnaround routing algorithm
- Better than optimized optical crossbars
  - Six MRs, four waveguides, no terminators
  - Minimized waveguide crossing insertion loss
  - Ports are aligned to intend directions
- Passively route packets
  - Between UP-left and DOWN-left as well as UP-right and DOWN-right
  - Save power and reduce MR insertion loss in 40% cases

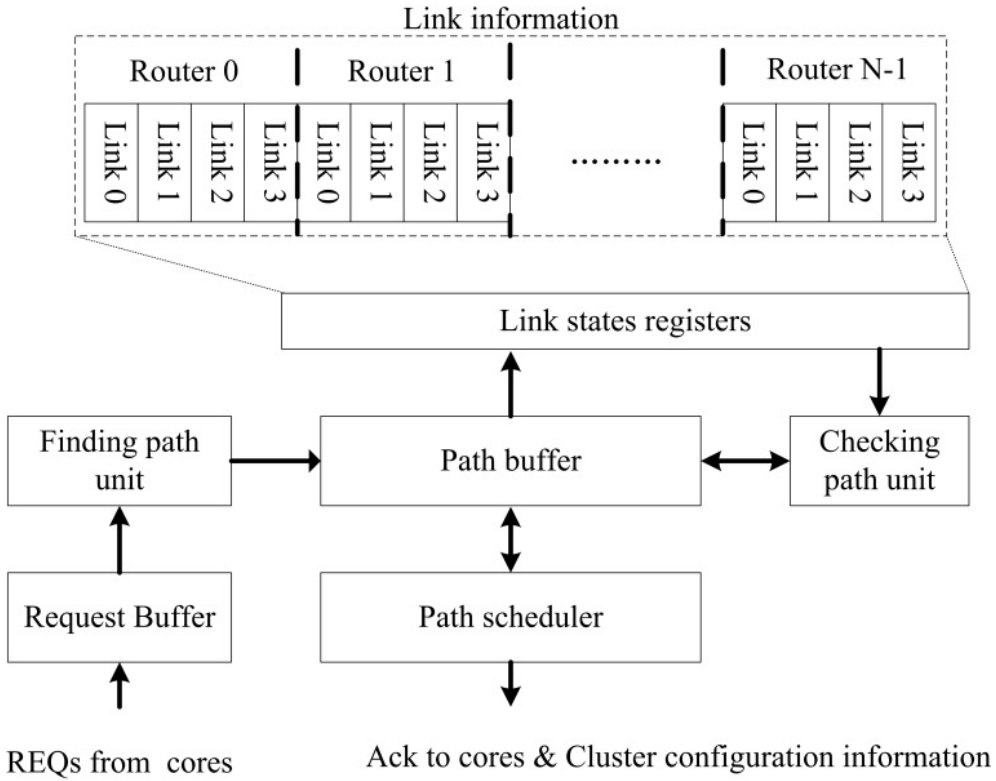




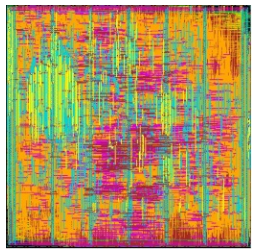
Network Controller







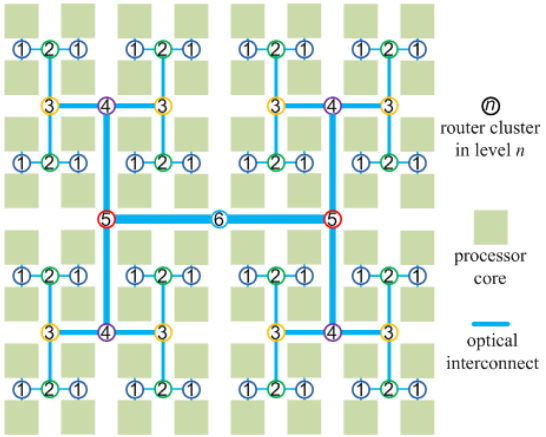
- Connected to the top level router cluster
- Deterministic turnaround routing algorithm
  - Complexity is $O(n \log n)$

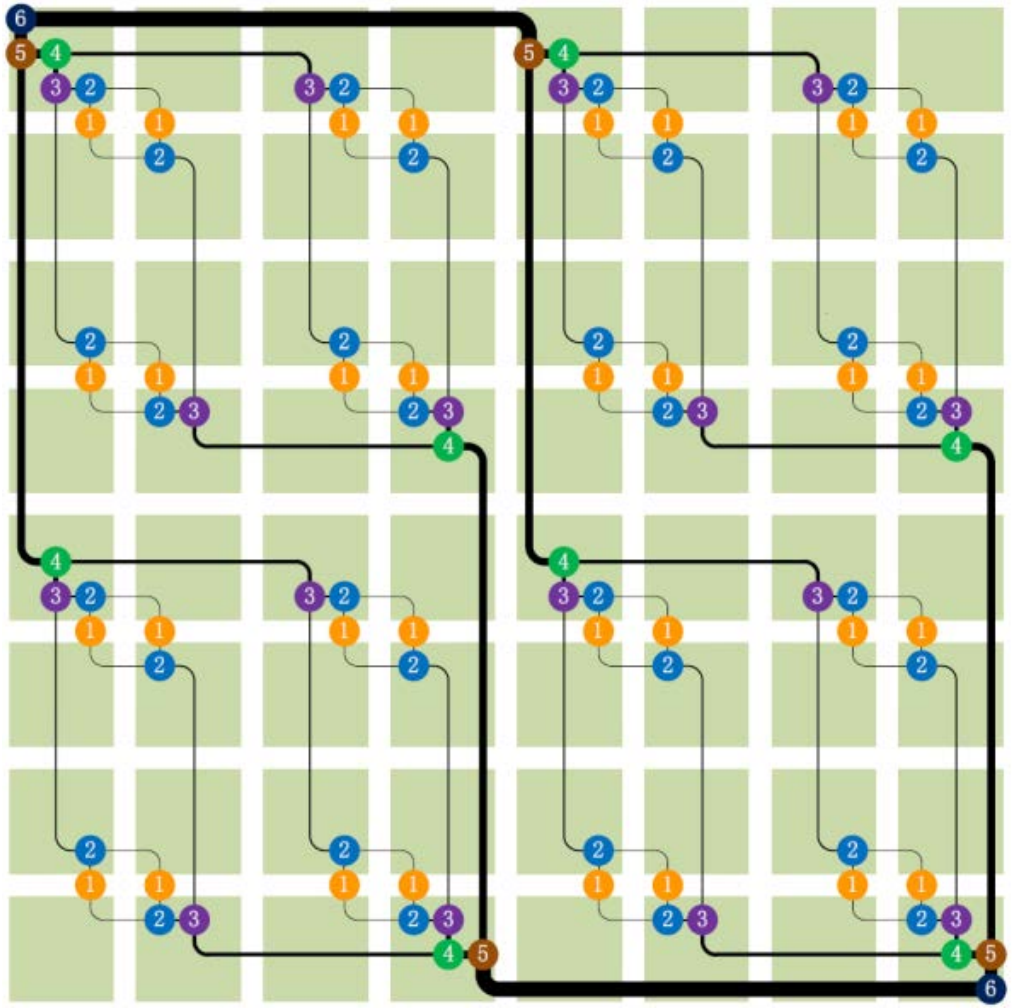


- Cost is 0.11mm2 and 31μW/MHz for 64-core 1.25GHz multicore processor in 45nm

Floorplan of Fat Tree Based ONoC

- Cluster the routers
- The optimized floorplan minimizes the number of waveguide crossings
  - Waveguide crossing is the major cause of optical power loss
  - 87% reduction compared to the H-tree floorplan

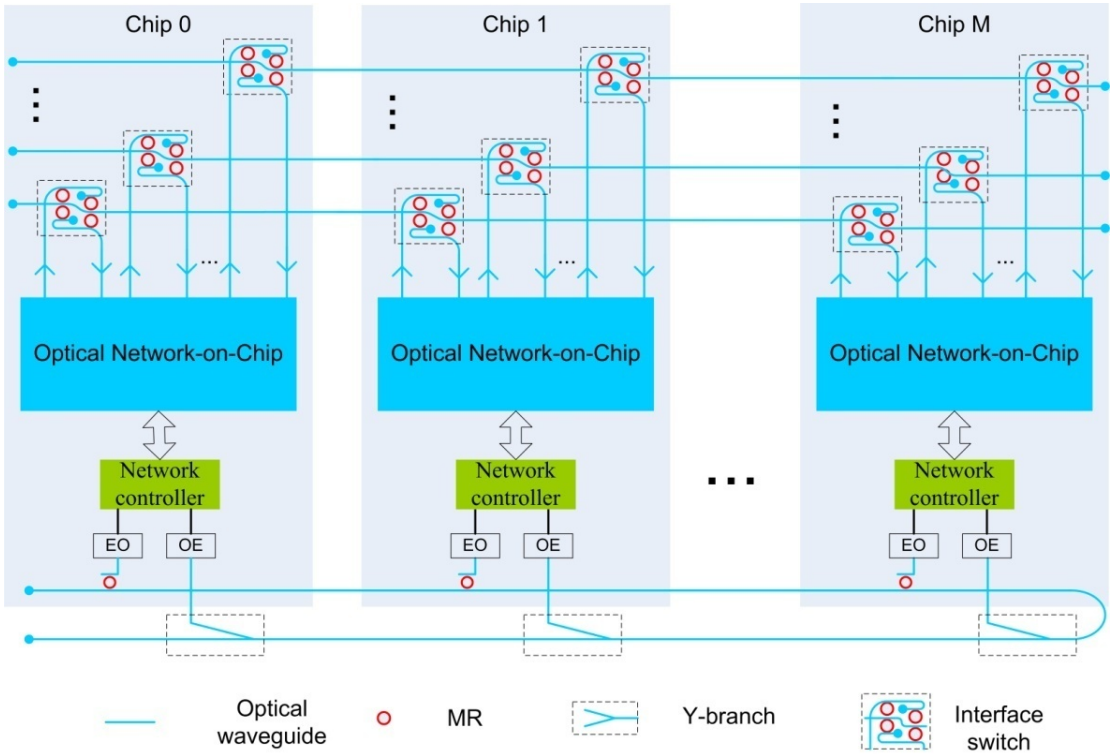


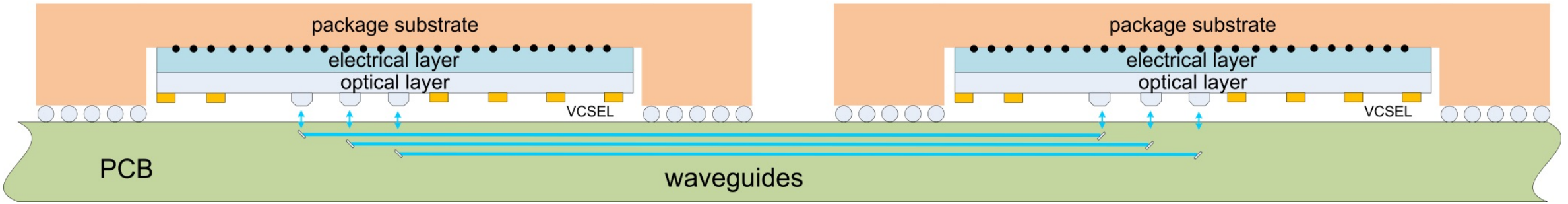


* Zhehui Wang, Jiang Xu, *et al.*, "Floorplan Optimization of Fat-Tree Based Networks-on-Chip for Chip Multiprocessors", IEEE Transactions on Computers 2012

Inter-Chip Optical Network

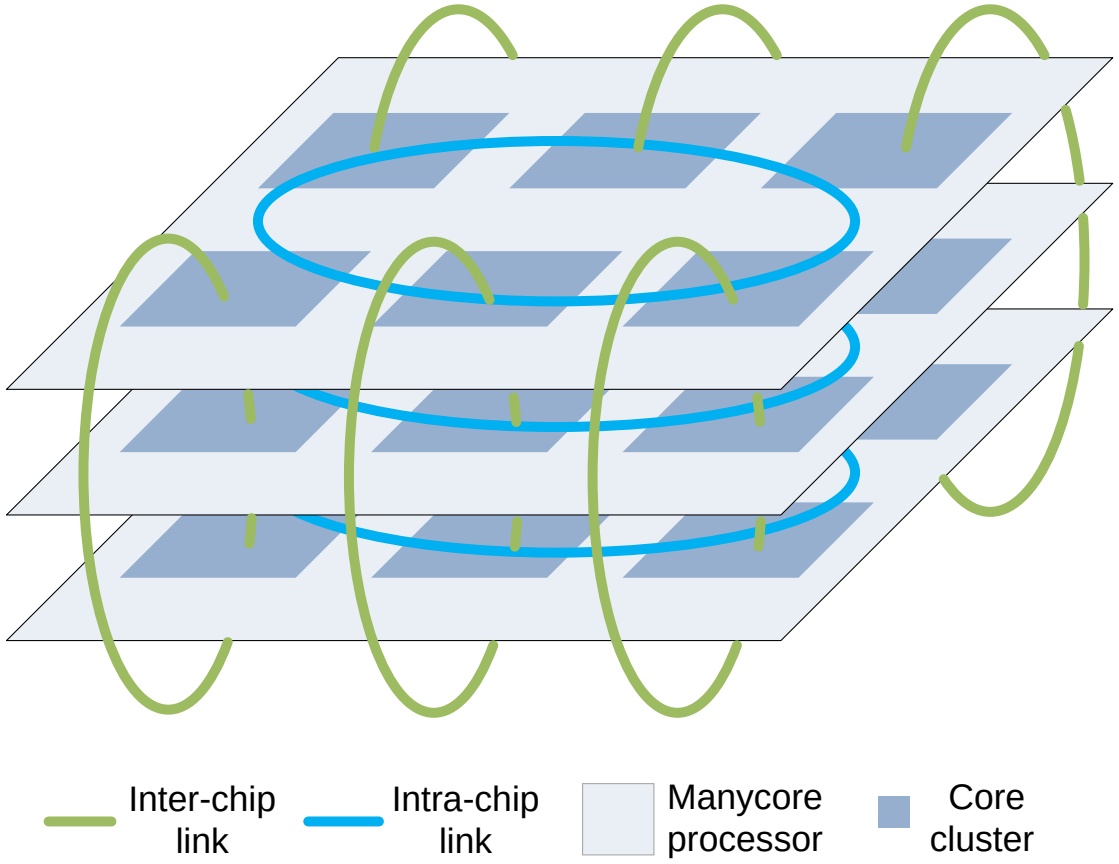
- Multichannel data bus
  - One channel per top-level router
  - Each half-duplex bidirectional channel uses one waveguide
  - Each channel can be dynamically divided to carry multiple point-to-point communications simultaneously
  - Interface switches are controlled by network controllers
- Control bus uses a single waveguide



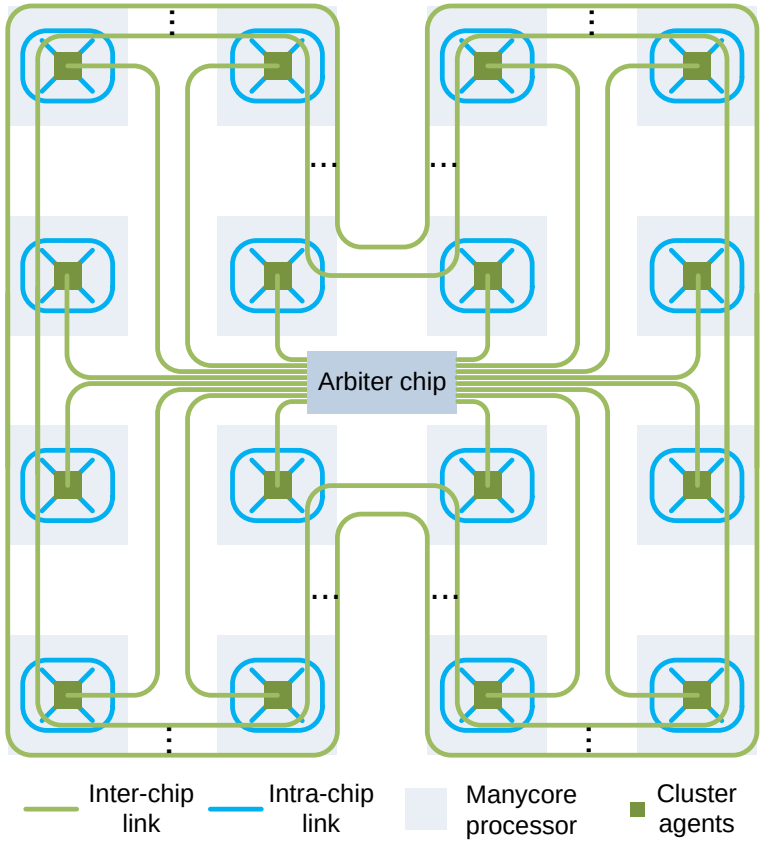


I²CON: Ring-Based Inter/Intra-Chip Optical Network

Logical view



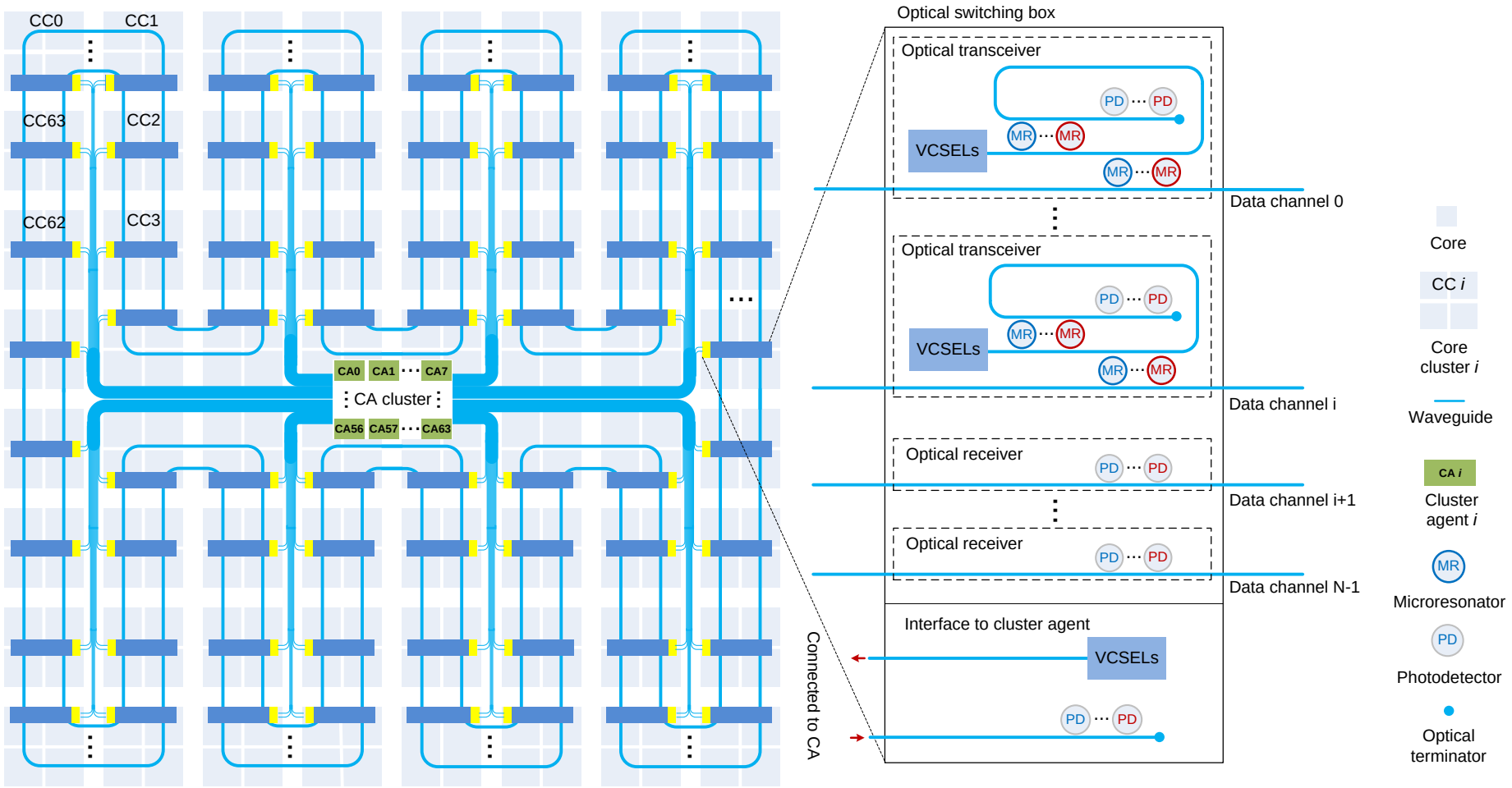
Multi-chip floorplan



*Xiaowen Wu, Jiang Xu, *et al.*, “An Inter/Intra-chip Optical Network for Manycore Processors," TVLSI 2014

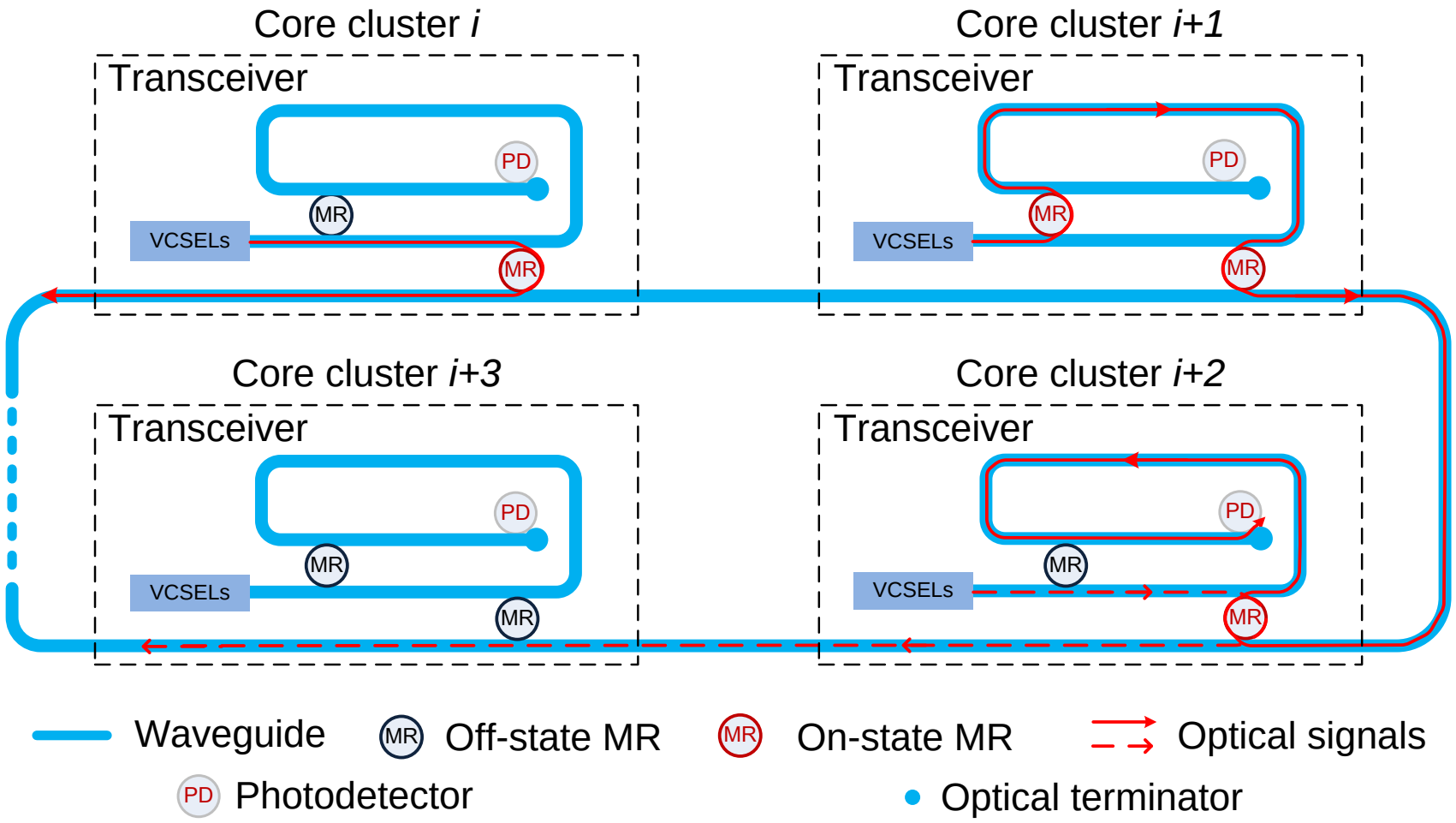
SUOR for Intra-chip Network

- SUOR: Sectioned Undirectional Optical Ring



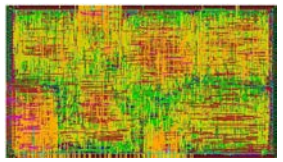
Data Channels

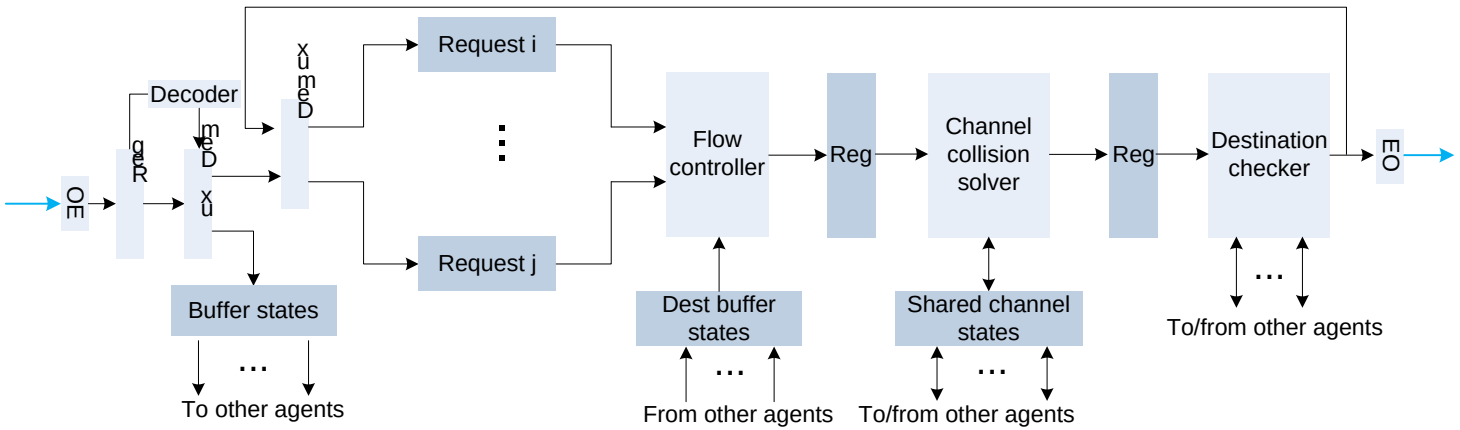
- Segmentation and bidirection to improve channel utilizations

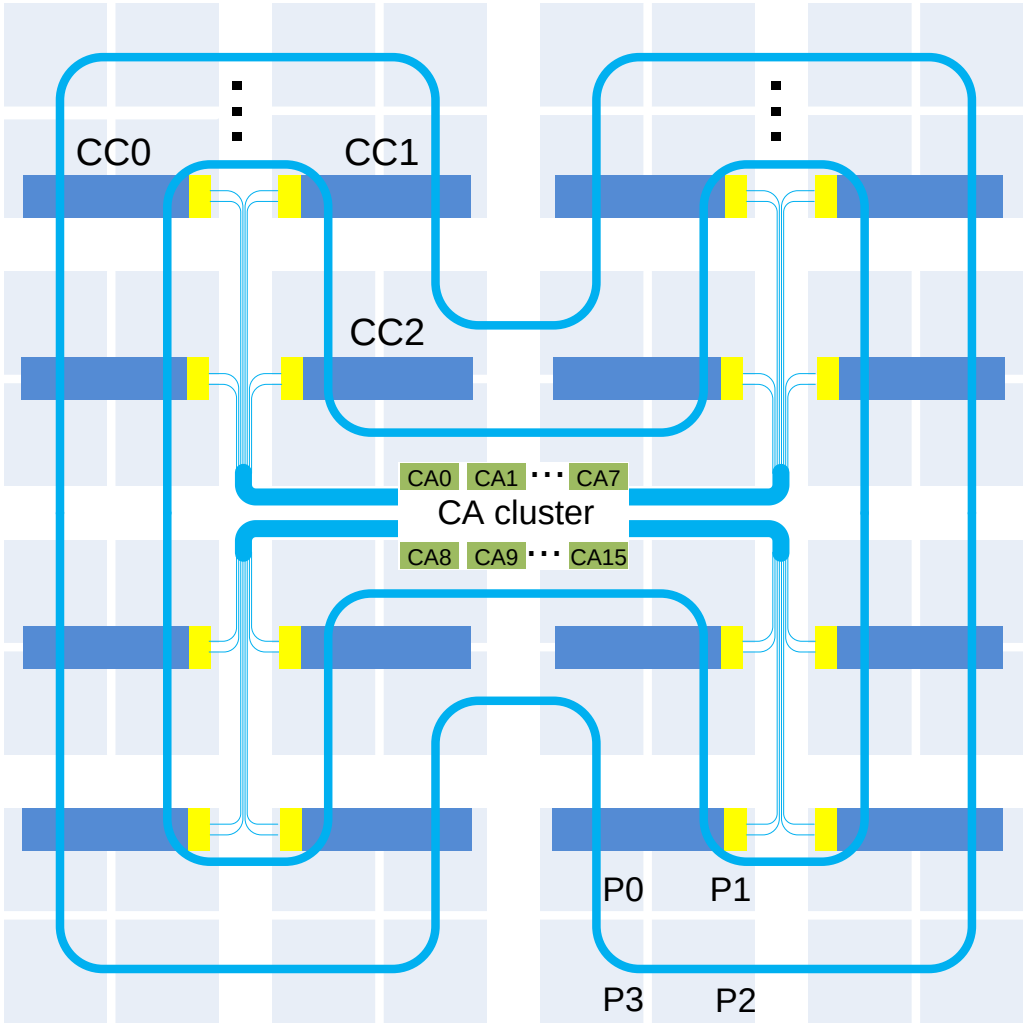


Physically Centralized Logically Distributed Control

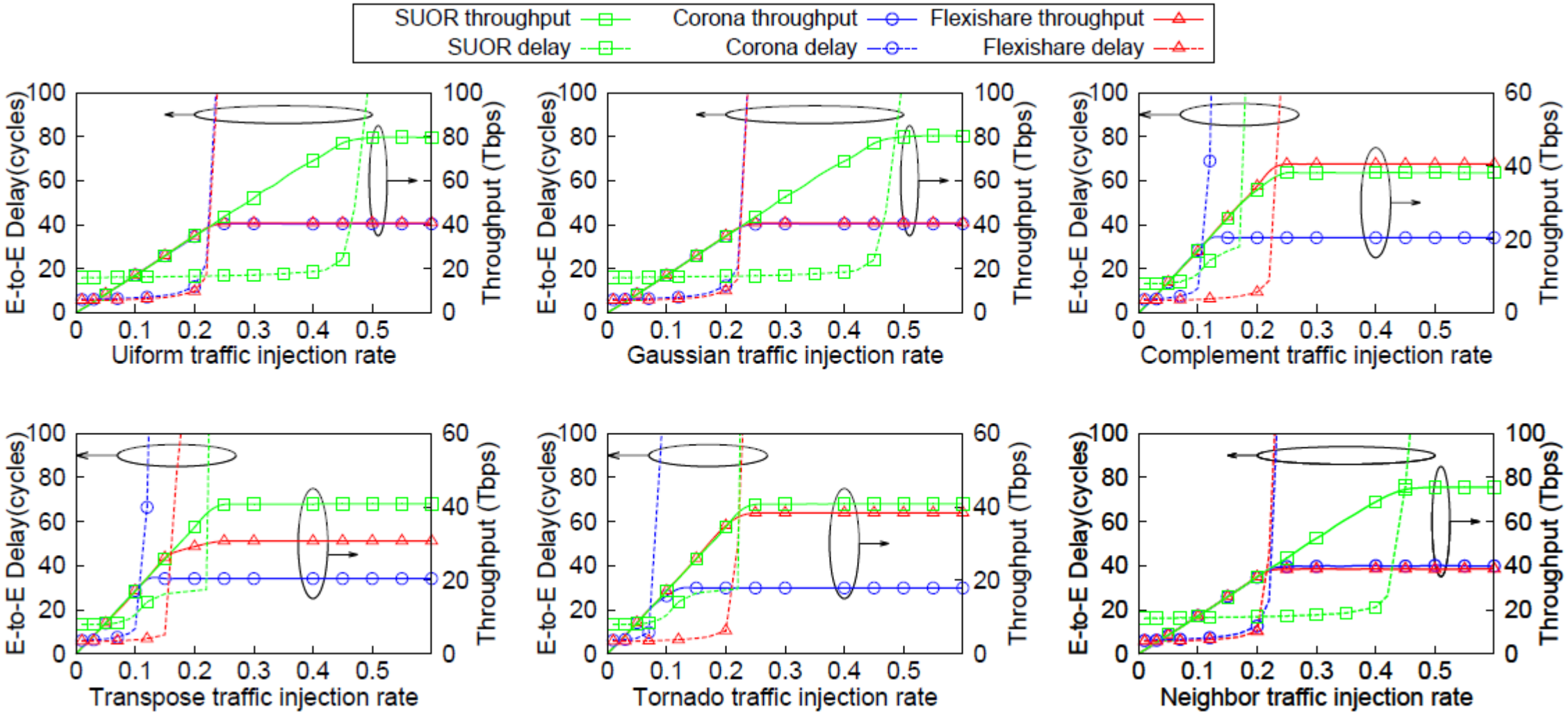
- A cluster agent for each cluster
- Agents are in the center of chip
  - Optically connected with clusters
  - Electrically connected with each other



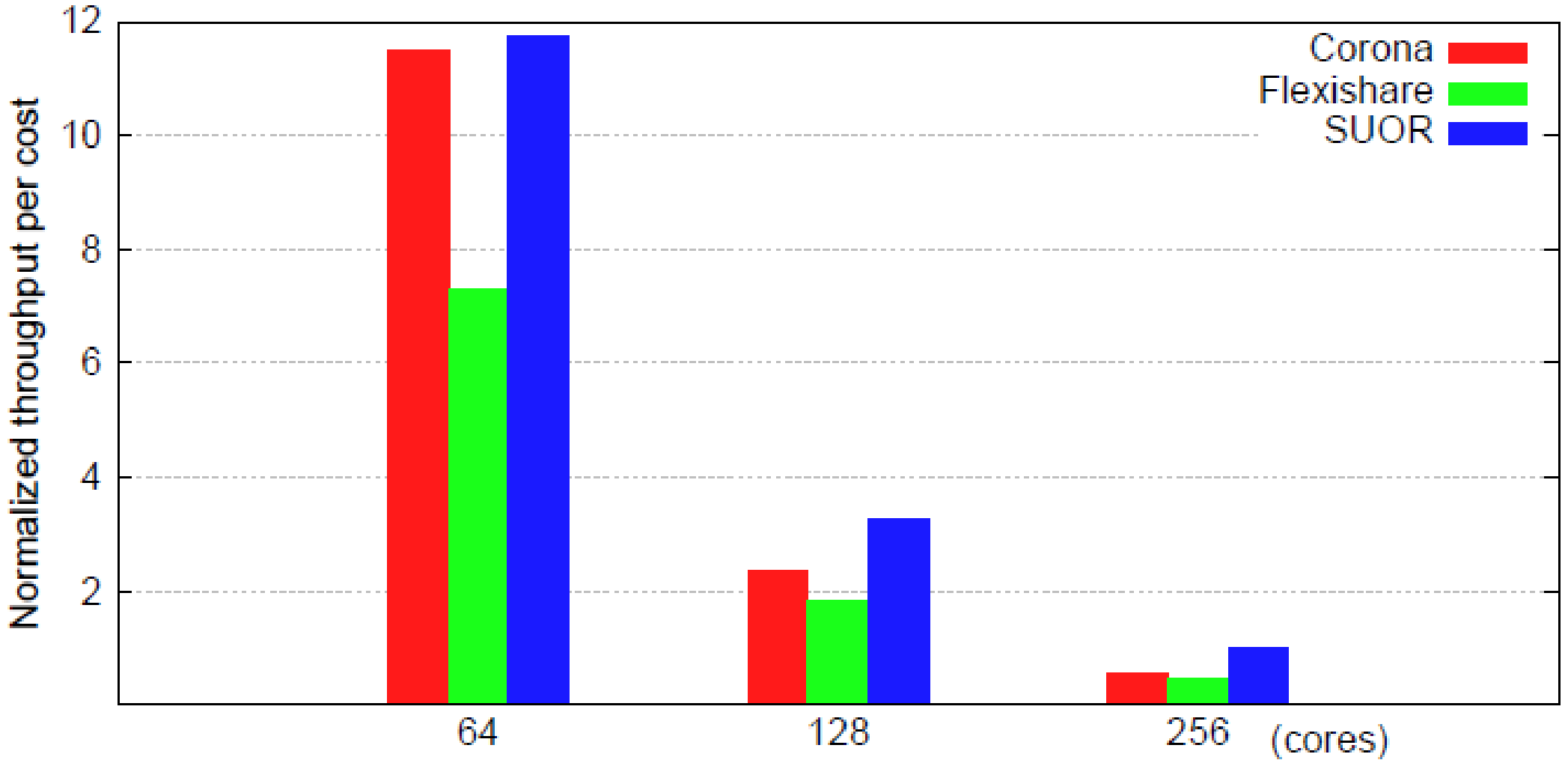




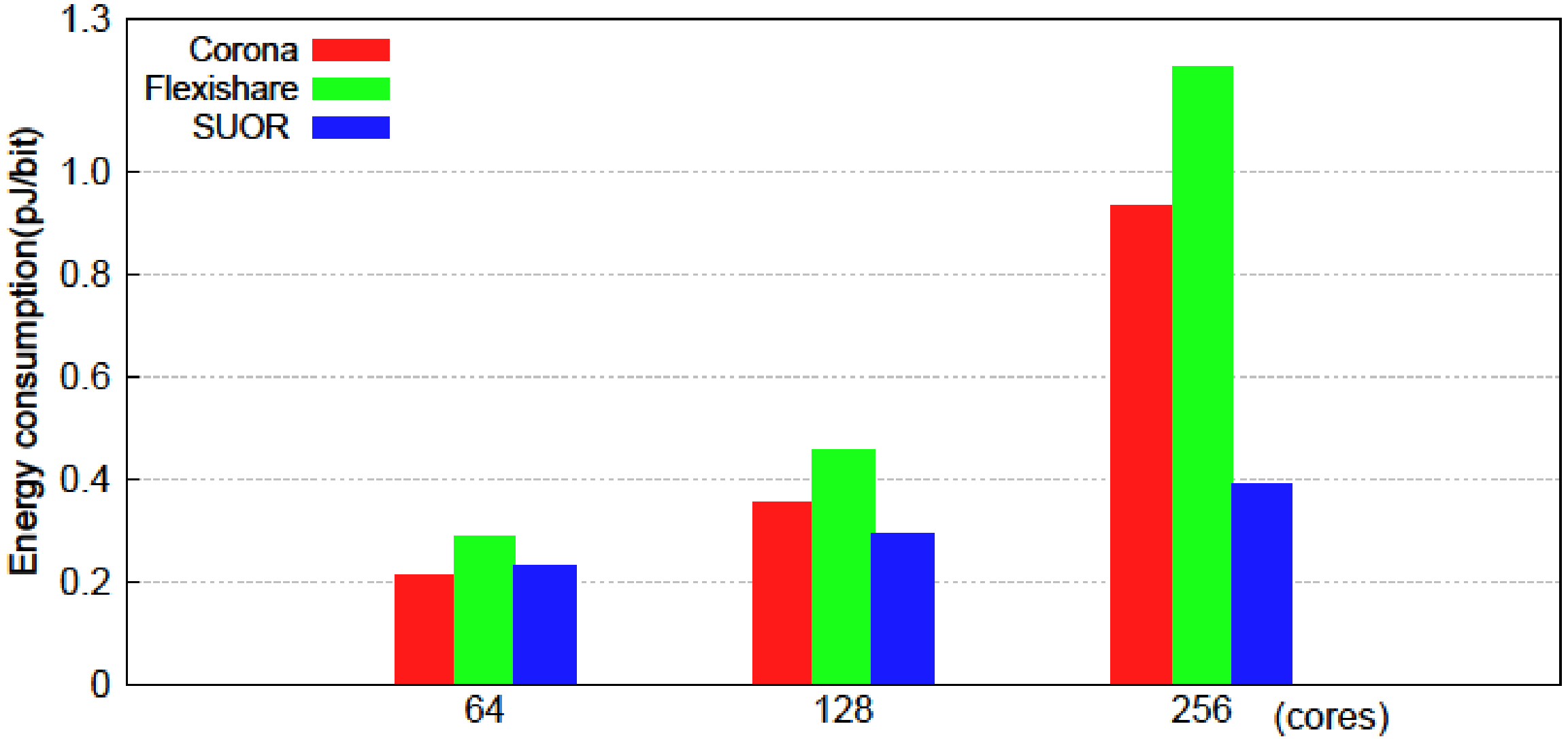
Intra-Chip Network Evaluation: SUOR Performance



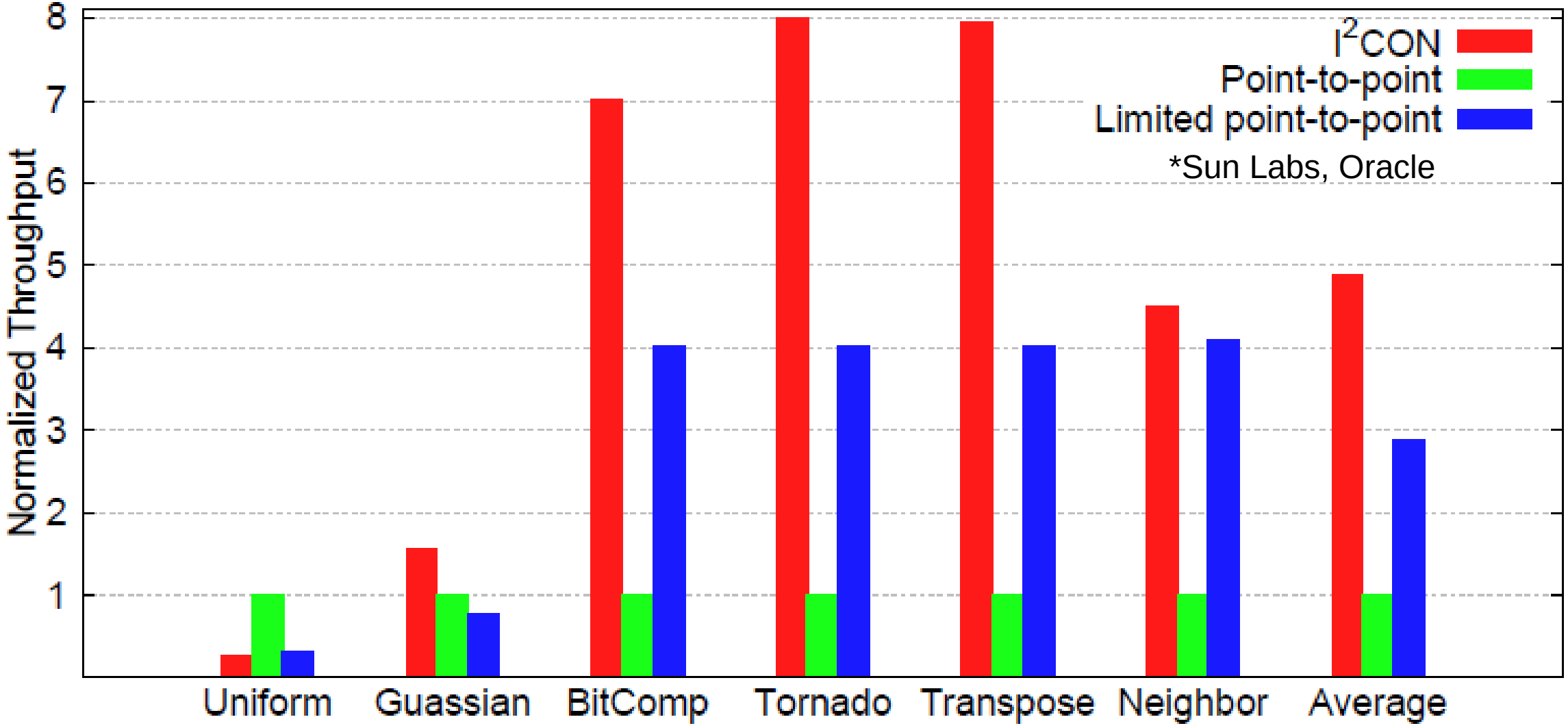
Intra-Chip Network Evaluation: SUOR Cost



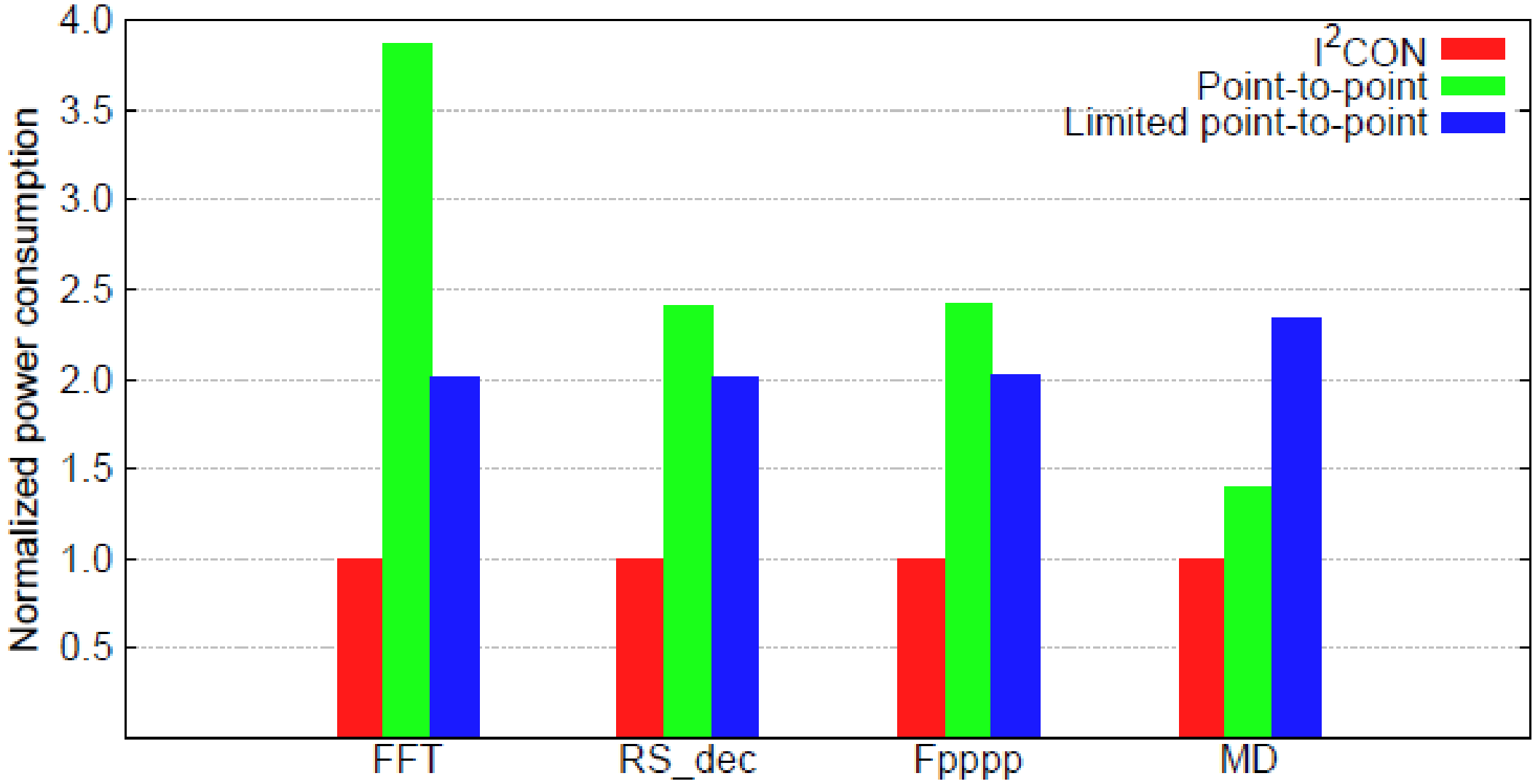
Intra-Chip Network Evaluation: SUOR Energy Efficiency



I²CON Performance



I²CON Energy Efficiency



Wide Ranges of Parameters are Evaluated

MR passing loss(MR_P)	0.001 dB	0.1 dB
MR drop loss(MR_D)	1.5 dB	0.5 dB
Inter-layer coupler loss(CP)	0.45 dB	1.4 dB
Silicon waveguide loss(S_WG)	1dB/cm	0.274 dB/cm
Polymer waveguide loss(P_WG)	0.07dB/cm	0.5 dB/cm
Photodetector sensitivity(PD)	-20 dBm	-14.2 dBm
On-chip Laser efficiency(Laser)	15%	10%
OE/EO conversion power(OE/EO)	100 fJ/bit	500fJ/bit
Tuning power(Tuning)	20 μW	100 μW

Outline

- Introduction
- Optical Routers
- Unified Inter/Intra-Chip Optical Network
- Thermal Modeling
- Optical Crosstalk Noise Analysis
- Open-Source Research and Development Tools
- Summary

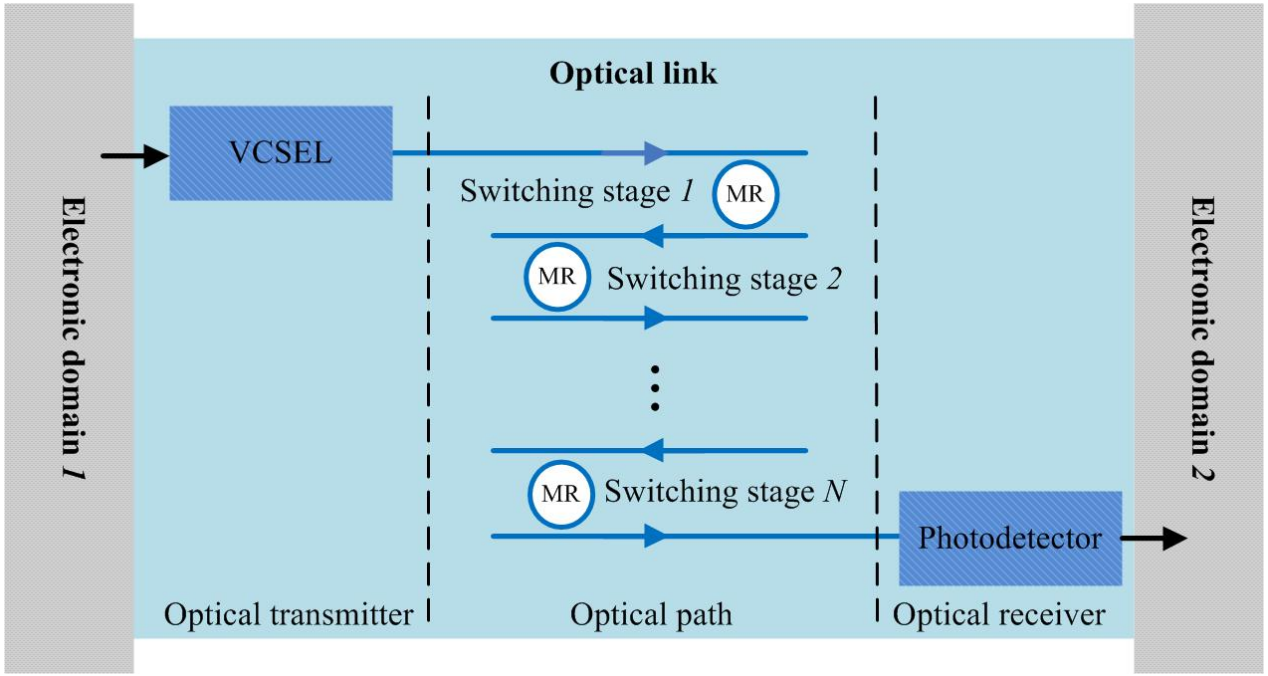
Thermal Modeling

- Chip temperatures vary a lot over both time and space
- Thermal effects can cause
  - Laser power efficiency degradation
  - Temperature-dependent wavelength shifting
  - Optical power loss caused by wavelength mismatch
- System-level thermal model needs to consider
  - VCSEL temperature-dependent wavelength shifting and power efficiency
  - Microresonator temperature-dependent wavelength shifting and optical power loss
  - Waveguide propagation loss variation
  - Photodetector sensitivity and dark current
  - Chip temperature distribution

* Yaoyao Ye, Zhehui Wang, Peng Yang, Jiang Xu, *et al.*, “System-Level Modeling and Analysis of Thermal Effects in WDM-Based Optical Networks-on-Chip,” IEEE TCAD 2014
* Yaoyao Ye, Jiang Xu, *et al.*, “Modeling and Analysis of Thermal Effects in Optical Networks-on-Chip”, ISVLSI 2011

Thermal Model of Optical Interconnects

- Necessary condition for an functional optical link
  - Optical power reaching the receiver must be larger than the receiver sensitivity



$$P_{TX} - L_{SW} - L_{WG} \geq S_{RX}$$

$$P_{TX} = (I - \alpha - \beta(T_{VCSEL} - T_{th})^2)(\varepsilon - \gamma \cdot T_{VCSEL})$$

$$L_{SW} = \sum_{i=1}^{N} 10log((\frac{2\kappa^2 + \kappa_p^2}{2\kappa^2})^2 \cdot (1 + (\lambda_{VCSEL\_min} + \rho_{VCSEL}(T_{VCSEL} - T_{min}) - \rho_{MR}(T_{MR_i} - T_{min}) - \lambda_{MR\_min})^2/\delta^2))$$

$$10log((I - \alpha - \beta(T_{VCSEL} - T_{th})^2)(\varepsilon - \gamma \cdot T_{VCSEL})) - \sum_{i=1}^{N} 10log((\frac{2\kappa^2 + \kappa_p^2}{2\kappa^2})^2 \cdot (1 + \delta^{-2}(\lambda_{VCSEL\_min}$$
$$+\rho_{VCSEL}(T_{VCSEL} - T_{min}) - \rho_{MR}(T_{MR_i} - T_{min}) - \lambda_{MR\_min})^2)) - L_{WG} \geq S_{RX}$$

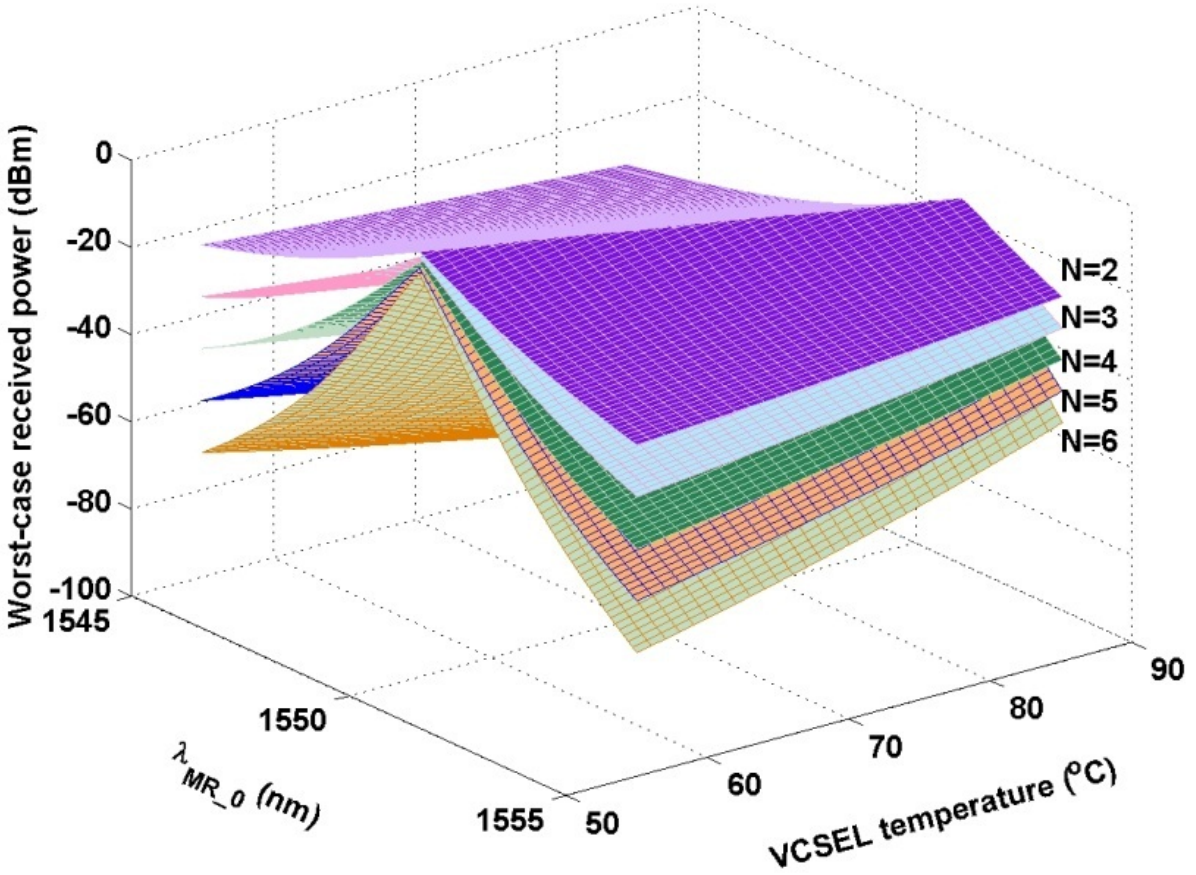
Optimal Initial Device Settings

- Total power consumption

$$P_{total} = P_{VCSEL} + P_{driver} + P_{MRs} + P_{SerDes} + P_{receiver}$$

- There are optimal initial device settings to minimize power

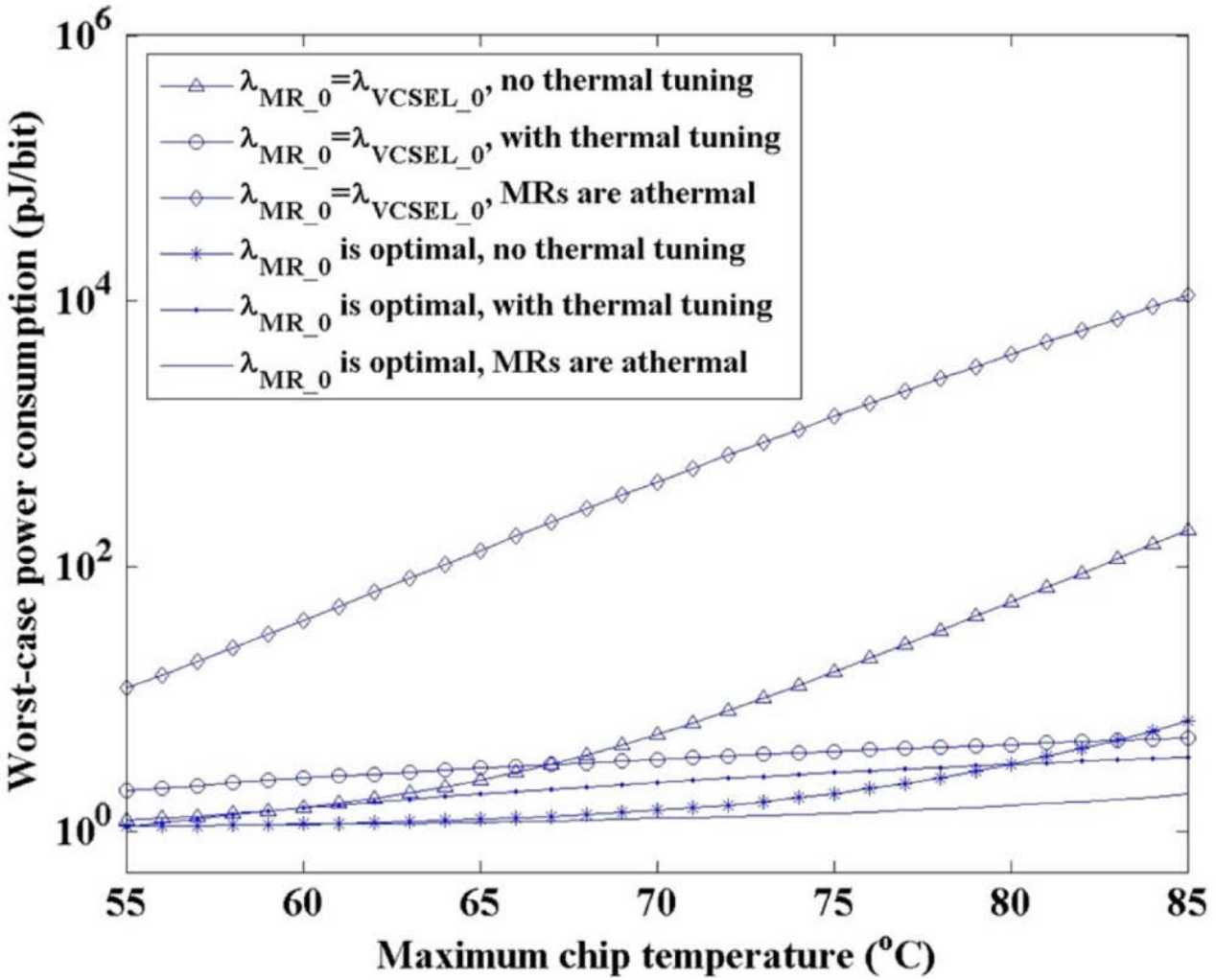
$$\lambda_{MR\_0} = \lambda_{VCSEL\_0} + \frac{\rho_{VCSEL} - \rho_{MR}}{2} \cdot (T_{max} + T_{min} - 2T_0)$$



Worst-case optical power received at the receiver (N is the number of switching stages)

Worst-Case Power Consumption

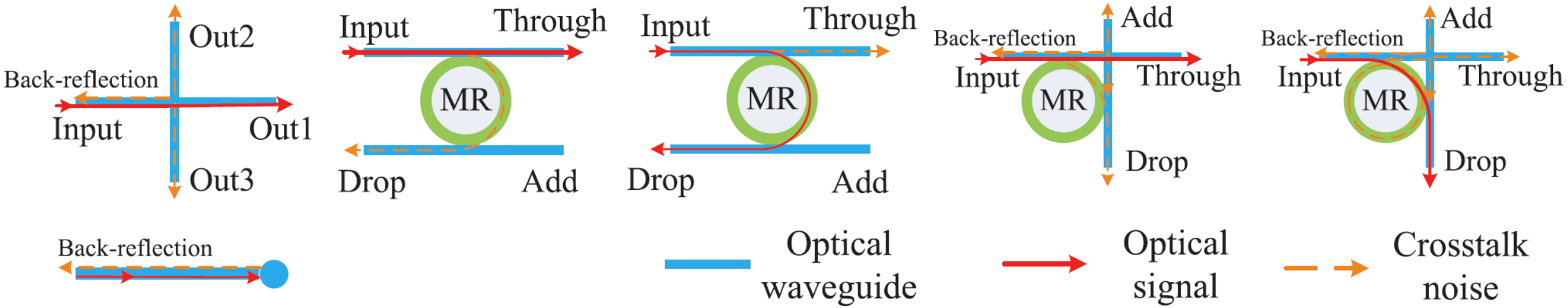
- Thermal tuning can compensate resonant wavelength deviations
- Default setting: λ_{MR_0}= λ_{VCSEL_0}=1550nm at room temperature
  - 5 pJ/bit when temperature reaches 85°C
- Optimal settings can improve the power efficiency by 29%



3-dB bandwidth is 3.1nm, three switching stages

Optical Crosstalk Noise

- Crosstalk noise is an intrinsic characteristic of optical components
  - Very small at device level: 0.01% ~ 0.1% of signals at device level
  - Was ignored at router and network levels
- We modeled them in the power domain



* Mahdi Nikdast, Jiang Xu, *et al.*, "Crosstalk Noise in WDM-based Optical Networks-on-Chip: a Formal Study and Comparison," IEEE TVLSI 2014
* Yiyuan Xie, Mahdi Nikdast, Jiang Xu, *et al.*, "Crosstalk Noise and Bit Error Rate Analysis for Optical Network-on-Chip", DAC 2010

Worst-Case Signal-to-Noise Ratio

- For arbitrary MxN mesh network using arbitrary optical routers

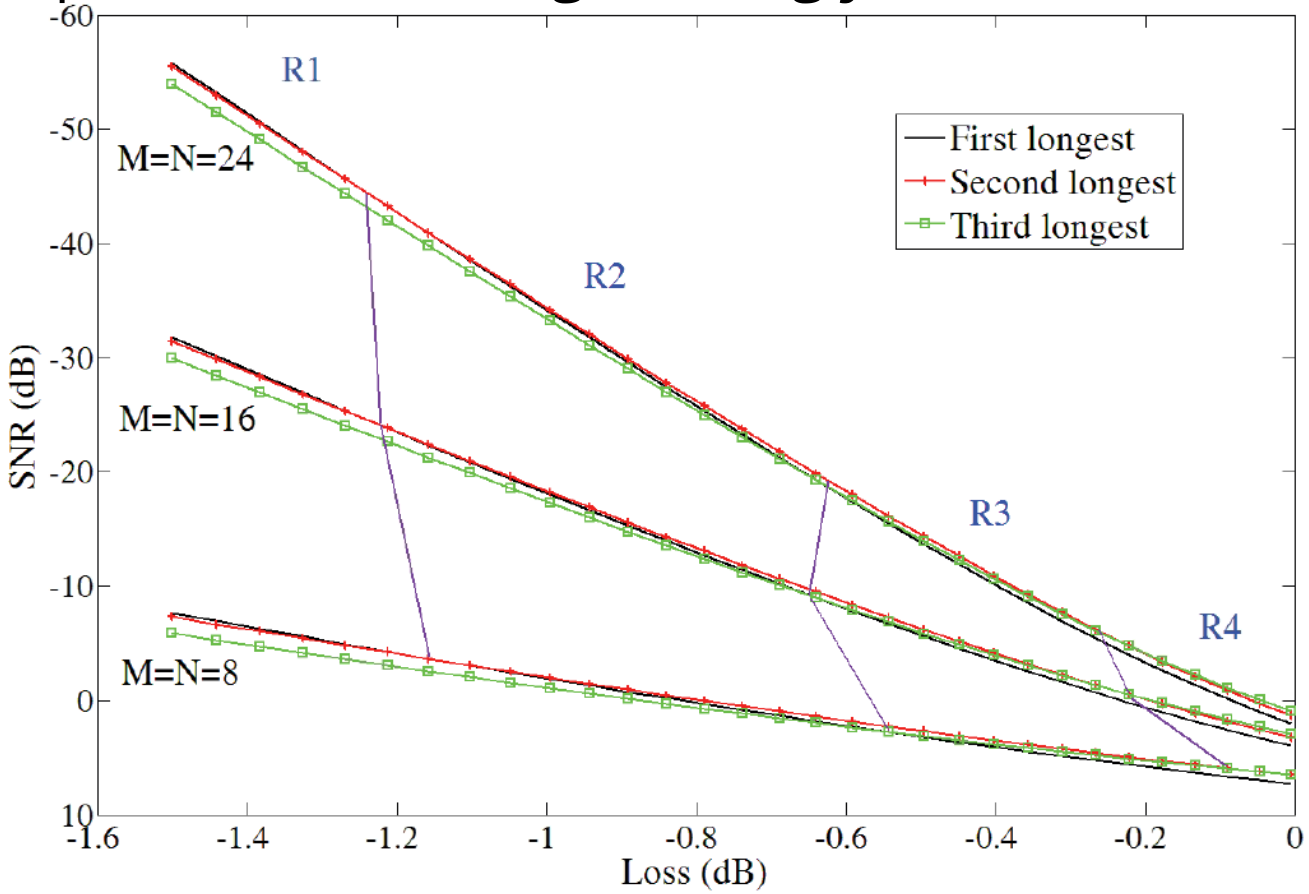
$$SNR_{a,\min,M,N} = \frac{L_{a,In,E} L_{a,W,E}^{N-3} L_{a,W,S} L_{a,N,S}^{M-3} L_{a,N,Ej}}{N_{a,X,1} L_{a,W,E}^{N-3} L_{a,W,S} L_{a,N,S}^{M-3} L_{a,N,Ej} + L_{a,W,S} L_{a,N,S}^{M-3} L_{a,N,Ej} \left(\frac{1-L_{a,W,E}^{N-3}}{1-L_{a,W,E}} N_{a,X,2} \right) + L_{a,N,Ej} L_{a,N,S}^{M-3} N_{a,Y,2} + L_{a,N,Ej} \left(\frac{1-L_{a,N,S}^{M-3}}{1-L_{a,N,S}} N_{a,Y,3} \right) + N_{a,Y,M}}$$

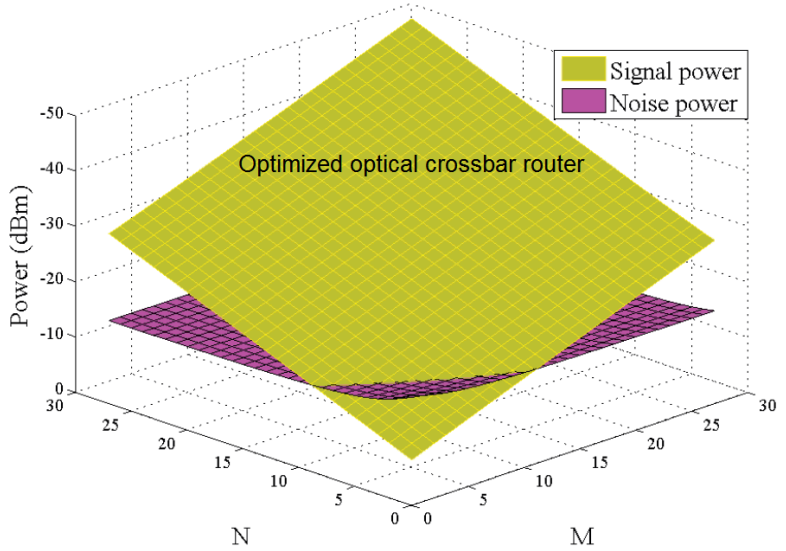
$$N_{a,X,j} = \begin{cases} L_{a,In,S} P_{in} \dfrac{L_{a,N,S}}{L_{C1}} L_{C2} L_B (k_1 + L_C^2 k_2) + L_{a,In,W} L_{a,E,Ej} P_{in} L_{C2} L_B k_1 & j = 1 \\ L_{a,In,W} \dfrac{L_{a,W,E}}{L_C^2 L_B} P_{in} k_1 + L_{a,In,W} L_{a,E,Ej} P_{in} L_{C2} L_B (k_1 + L_C^2 k_2) + L_{a,In,N} L_{a,S,N} \dfrac{L_{a,W,E}}{L_C^3 L_B^4} P_{in} k_1 + L_{a,In,S} \dfrac{L_{a,N,S}}{L_{C1}} P_{in} L_{C2} L_B (k_1 + L_C^2 k_2) & 2 \le j \le N-2 \end{cases}$$

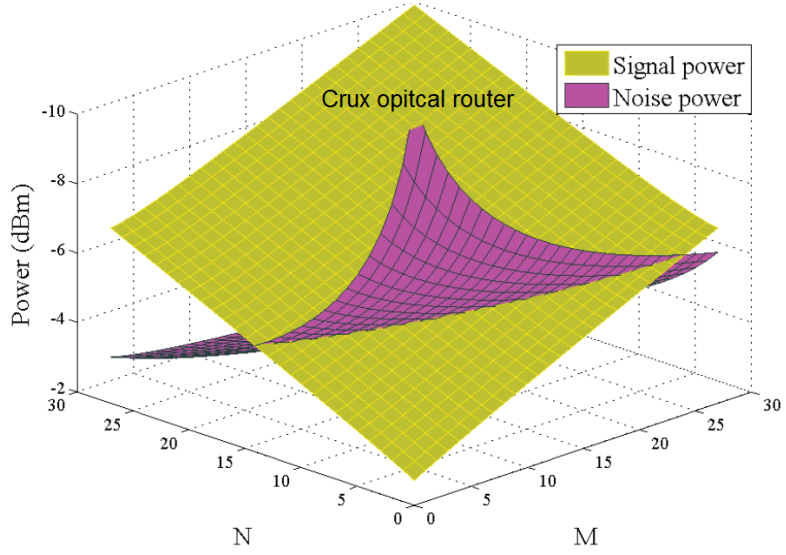
$$N_{a,Y,i} = \begin{cases} L_{a,In,W} \dfrac{L_{a,W,S}}{L_c^2 L_B} P_{in} k_1 + L_{a,In,S} \dfrac{L_{a,N,Ej}}{L_{C1}} P_{in} L_{C2} (k_1 + L_C^2 k_2) + L_{a,In,W} L_{a,E,N} \dfrac{L_{a,W,S}}{L_c^3 L_B^4} P_{in} k_1 + L_{a,In,W} \dfrac{L_{a,E,N}}{L_{C1} L_B^4} P_{in} L_{C2} (k_1 + L_C^2 k_2) & i = 2 \\ L_{a,In,W} \dfrac{L_{a,E,Ej}}{L_{C1}} P_{in} L_{C2} (k_1 + L_C^2 k_2) + \dfrac{L_{a,In,E}}{L_{C1} L_B L_{C2}} P_{in} (k_2 + L_{p1}^2 k1) & 3 \le i \le M-1 \\ L_{a,In,W} \dfrac{L_{a,E,W}}{L_c^4 L_B} P_{in} L_{C2} L_{C1} k_1 + P_{in} L_{C1}^3 k_1 & i = M \end{cases}$$

Worst-Case SNR

- Crosstalk significantly lowers SNR of mesh network
- Optical router design strongly affects SNR







Open-Source Research and Development Tools

- COSMIC Heterogeneous Multiprocessor Benchmark Suite
- MCSL Realistic Network-on-Chip Traffic Patterns
- CLAP Optical Crosstalk and Loss Analysis Platform
- OTEMP Optical Thermal Effect Modeling Platform
- Inter/Intra-Chip Optical Network Bibliography

www.ece.ust.hk/~eexu

Summary

- Optical interconnect is a promising technology
- Some techniques have been explored
- But much more could be done
- Open source tools help exploring new challenges

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