DESIGN, AUTOMATION & TEST IN EUROPE
9 – 13 March, 2015 · Grenoble · France
The European Event for Electronic System Design & Test

# Building a Scalable Design Environment for Silicon Photonics through PDKs

John Ferguson

Mentor Graphics®

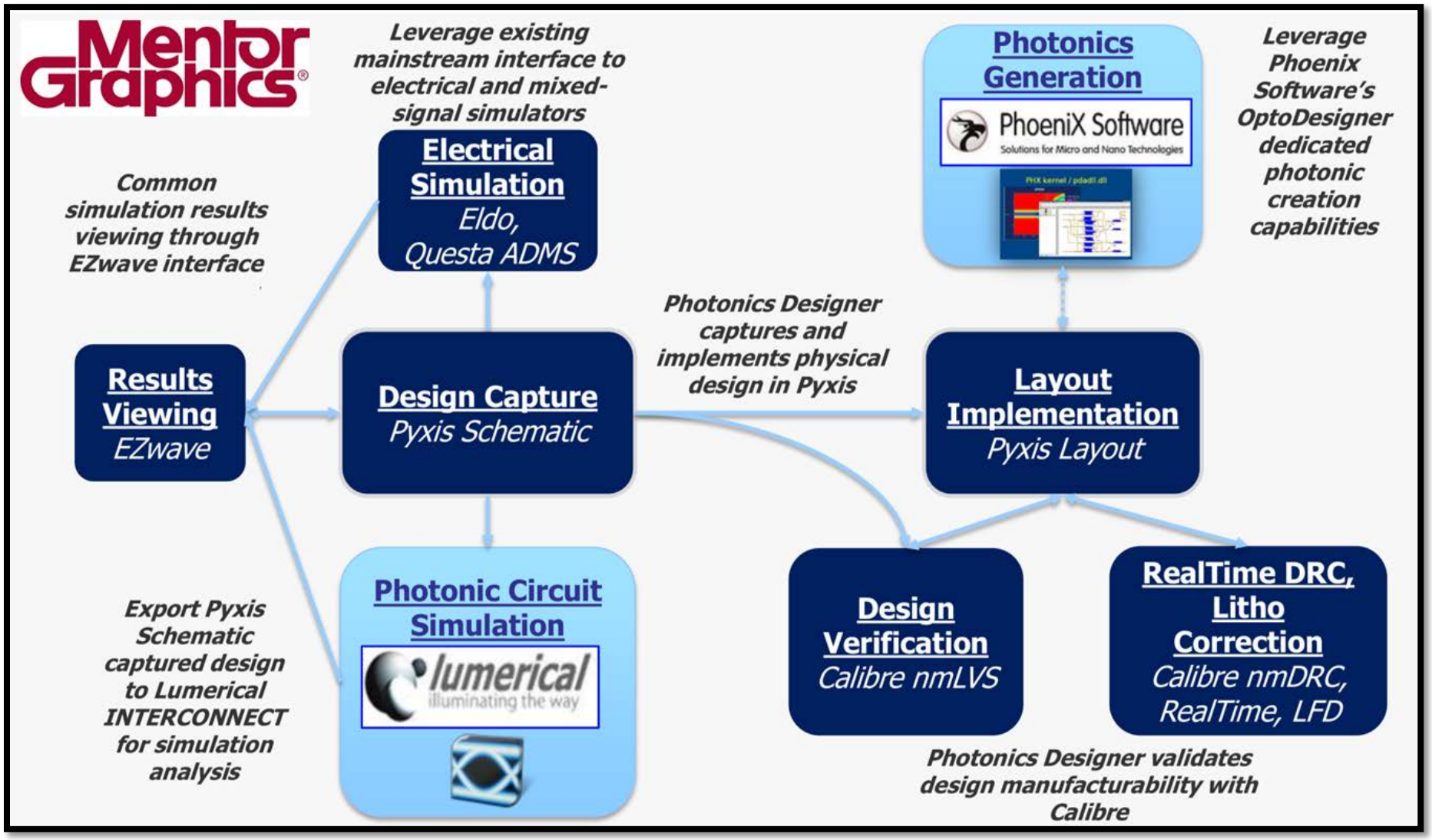
# Objective: Scalable Photonics Design Infrastructure

- **The electronic IC market has benefitted greatly from the scalability attributed to Moore's Law**
- **Meanwhile the photonic market remains limited to relatively small circuits**
  - **Design differentiation still focused on device physics as opposed to novel device and subcircuit re-use**

# What is Required to Move Forward?

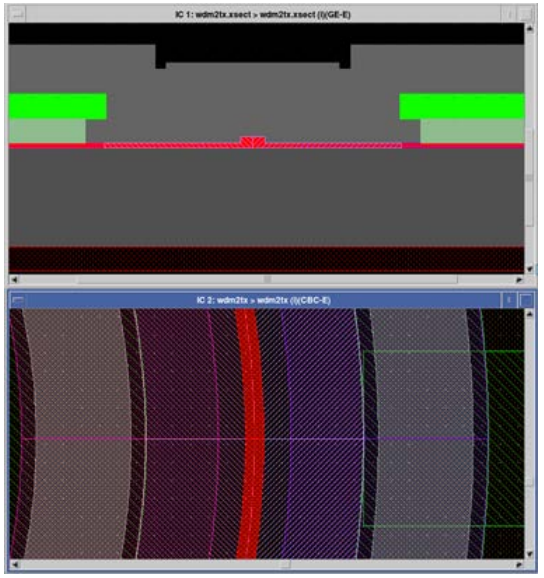
- Scalable Design Tools
  - Large scale optical simulation based on compact models
  - Automated/semi-automated layout
  - Physical verification and DFM
- Dedicated Process Development Kits (PDKs)
  - Foundry Supplied
  - Pre-characterized compact models
  - Pre-characterized device pcells
  - Process specific PV and DFM decks
  - Validated Tool Settings
- Reference Flows
  - Validated Design Flows
  - Device Characterization Procedures
  - Test and Measurement Methodologies
- Validated Re-Usable IP?

# Dedicated Photonics Custom Design Platform

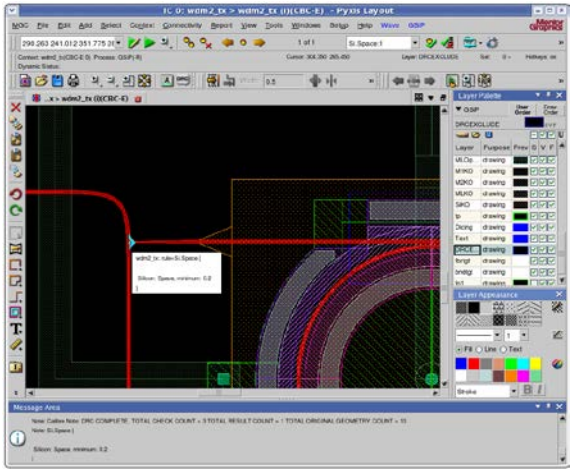


# Why Mentor Graphics?

- **Pyxis**
  - ✓ **No OA database angle restrictions**
  - ✓ **Strong integration to Calibre**
  - ✓ **Flexible framework enables new design methodologies**
  - ✓ **Excellent custom design assembly capabilities**

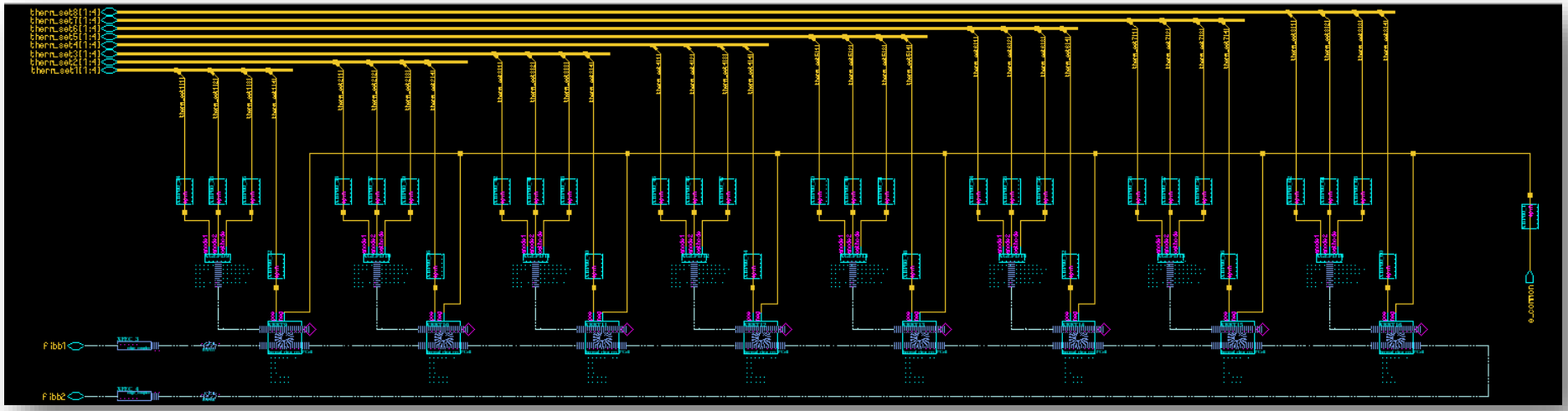


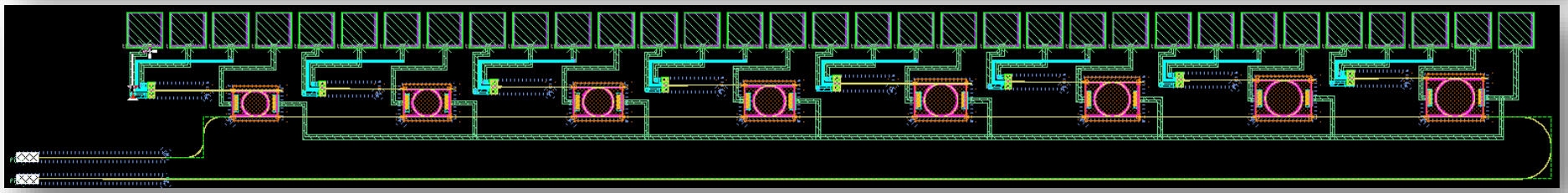
- **Calibre**
  - ✓ **Market and industry standard**
  - ✓ **Equation DRC handles complex curves**
  - ✓ **LVS of arbitrary devices and shapes**
  - ✓ **Calibre LFD enables “short loop” component analysis**



# Silicon Photonics Schematic Driven Layout

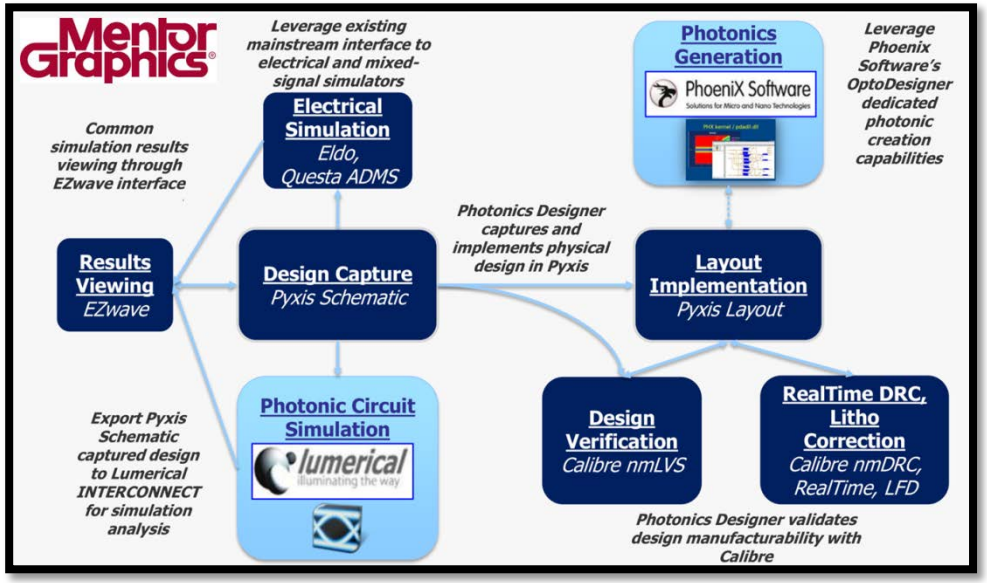
- Differentiated photonic and electrical connections
- PDK supplied schematic checks for photonic connections
- Schematic connectivity drives layout directly





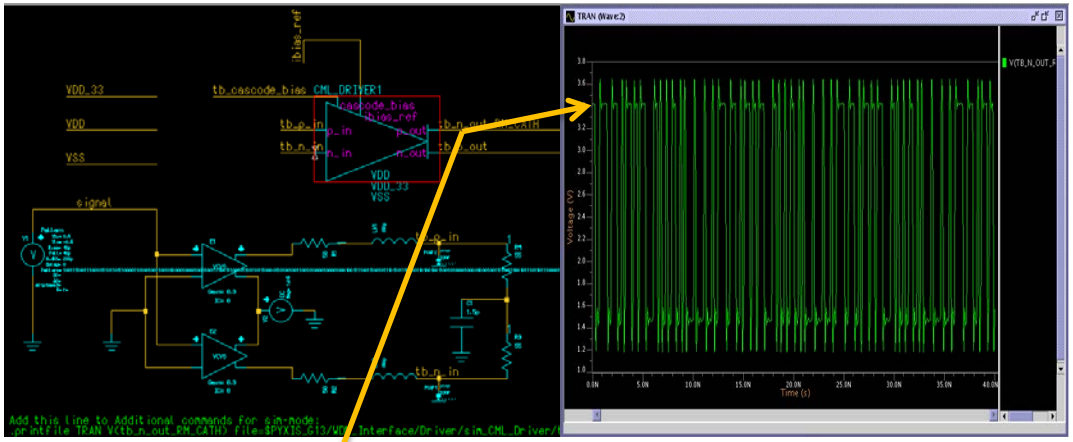
# Collaboration

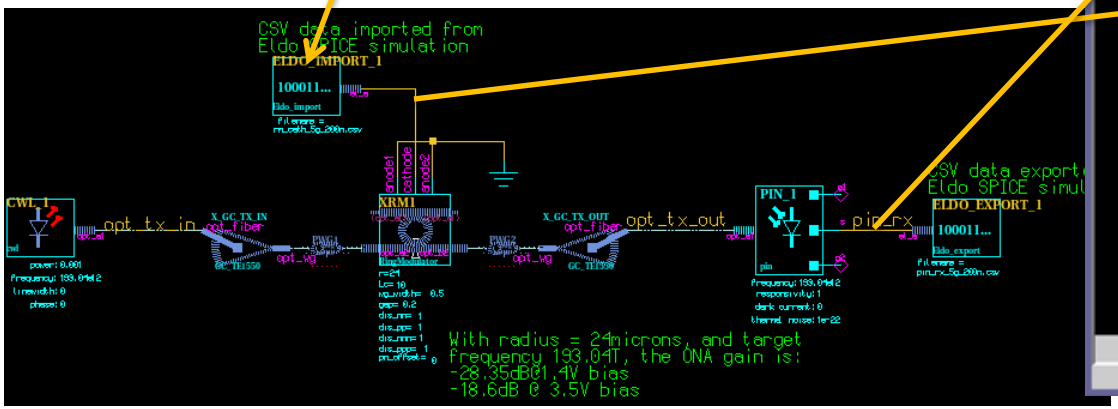
- **Mentor is offering full flow silicon photonics solution through collaboration**
- **Lumerical Solutions – OpenDoor partner**
  - ***INTERCONNECT* provides world-class time and frequency domain photonic circuit simulation**
  - **Integration to Pyxis Schematic allows designers to run simulation and LVS on the same schematic**
- **PhoeniX Software– OpenDoor partner**
  - ***OptoDesigner* is the dominant tool for the layout generation of advanced photonics structures**
  - **Developing flow for existing PhoeniX customers so they can leverage their existing PhoeniX photonics libraries**

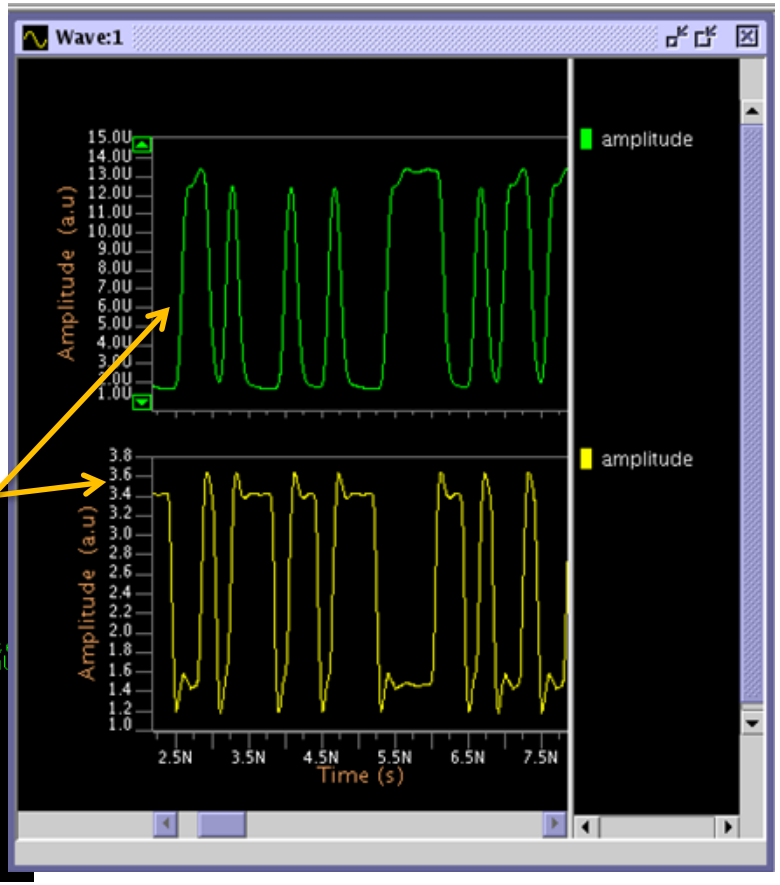


# Pyxis Silicon Photonics Activity

- **System Level Simulation**
  - **Driven from Pyxis Schematic / Layout**
  - **EZwave cockpit for electrical and optical simulation**



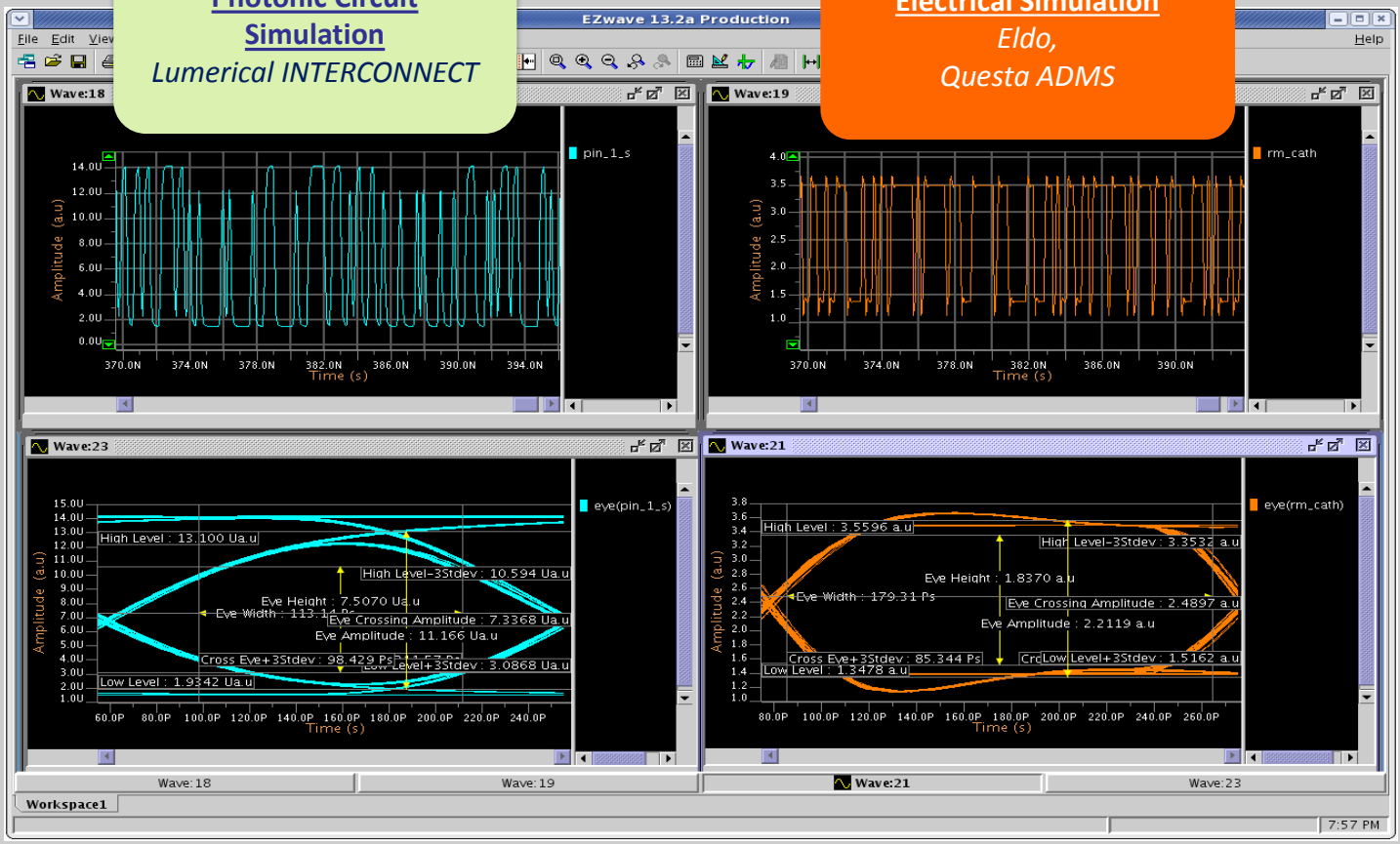



# Pyxis Silicon Photonics Activity

## Pyxis Schematic / EZwave Cockpit

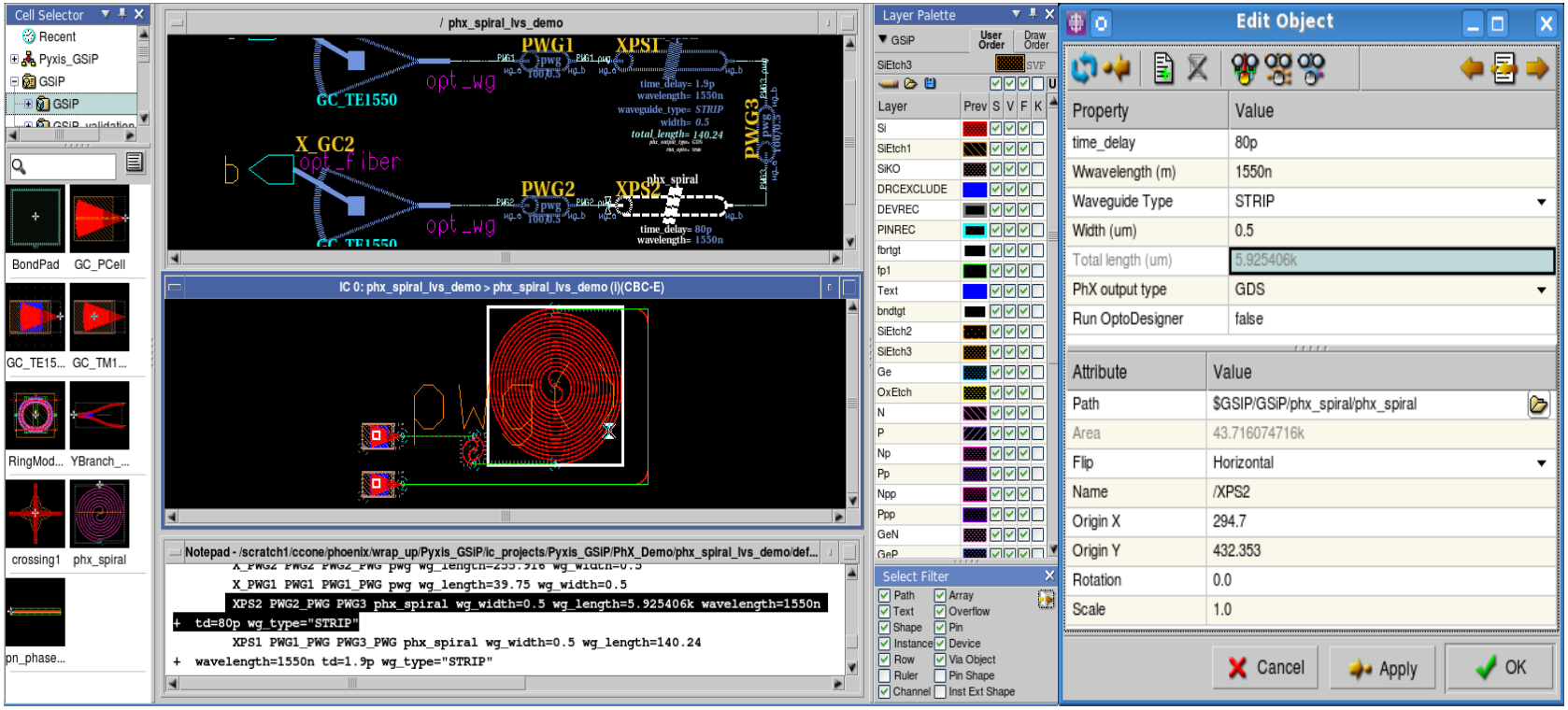
**Photonic Circuit Simulation**
*Lumerical INTERCONNECT*

**Electrical Simulation**
*Eldo,*
*Questa ADMS*



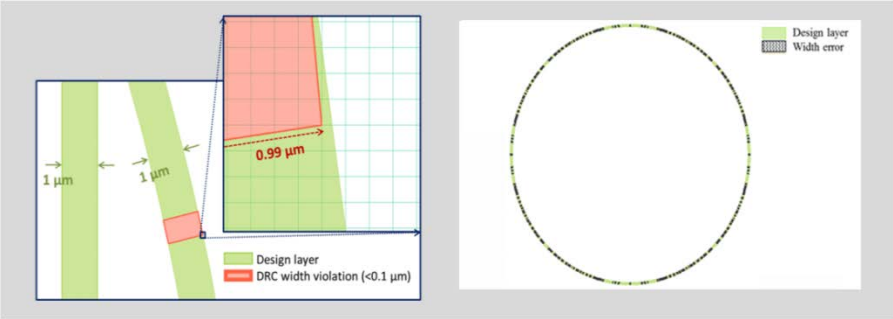
# Silicon Photonics PDKs
# Using PhoeniX OptoDesigner for Callbacks and PCell

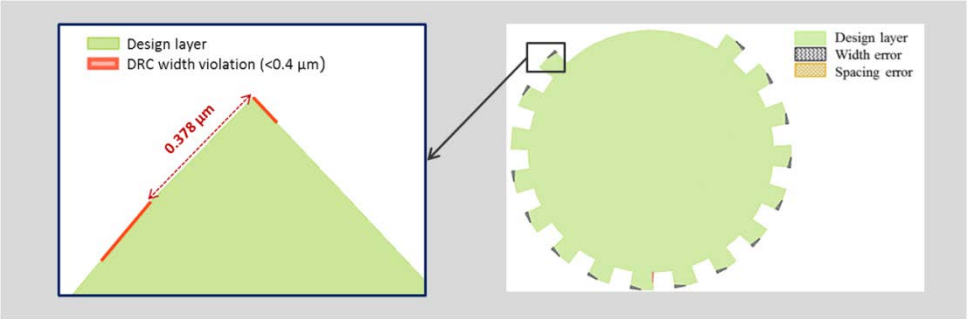
- **Using CMS Call backs for system property editing**
  - **Designer enters delay, width, wavelength and waveguide type**
  - **PhoeniX returns system parameters to schematic and layout**
  - **PCell created enabling full Schematic Driven Layout flow**



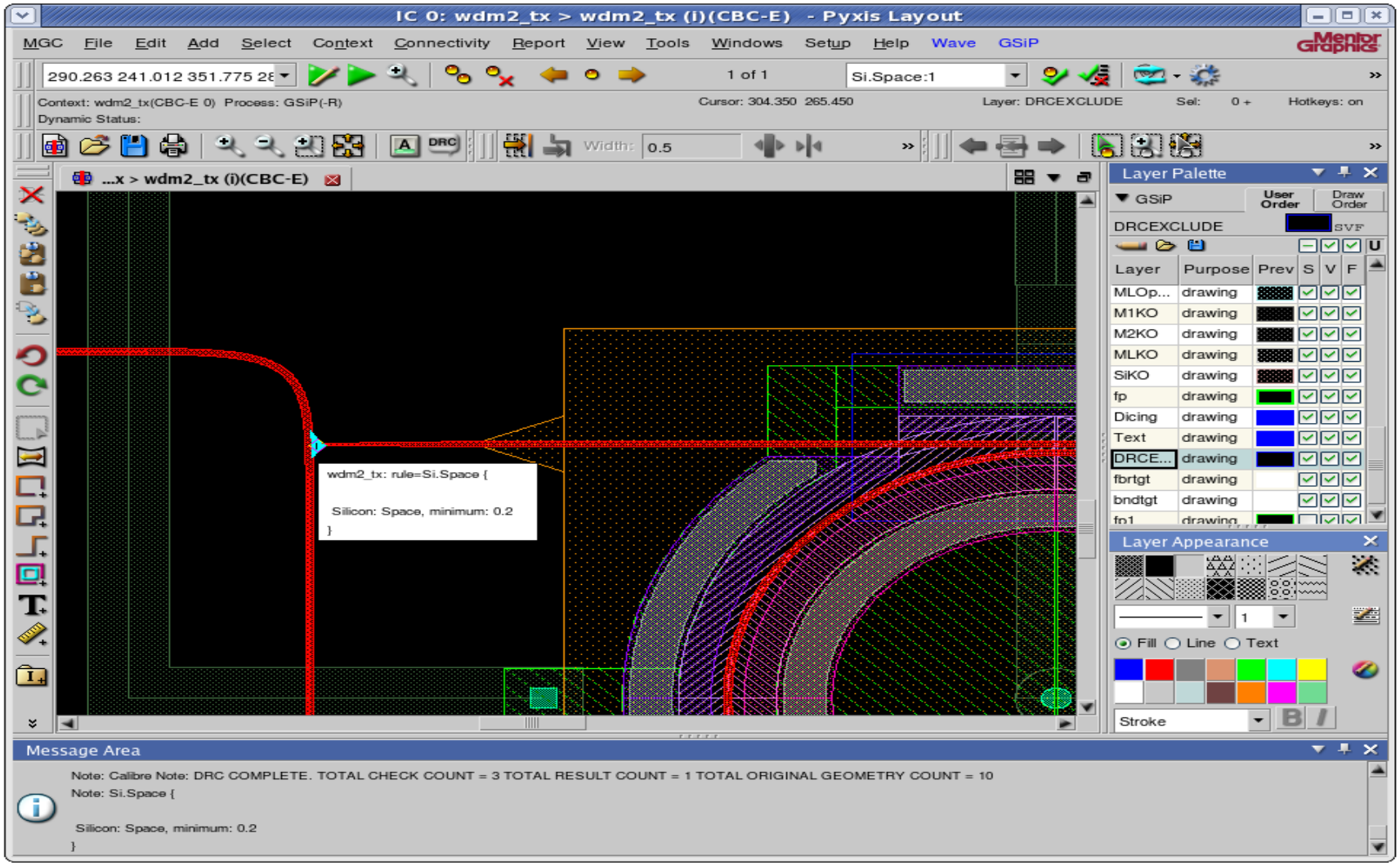
# DRC for Silicon Photonics

- **Design rules targeting CMOS processes will flag thousands of false errors in photonic structures**
  - **Curve rendering to gridded database**
  - **Default rule settings anticipate Manhattan shapes**
- **Photonic specific DRC rules can minimize false errors**
  - **Check options anticipating angled geometries**
  - **eqDRC for multi-dimensional PV analysis**



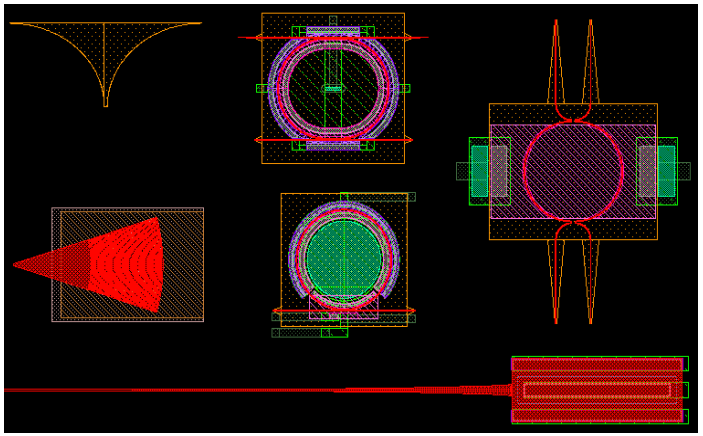



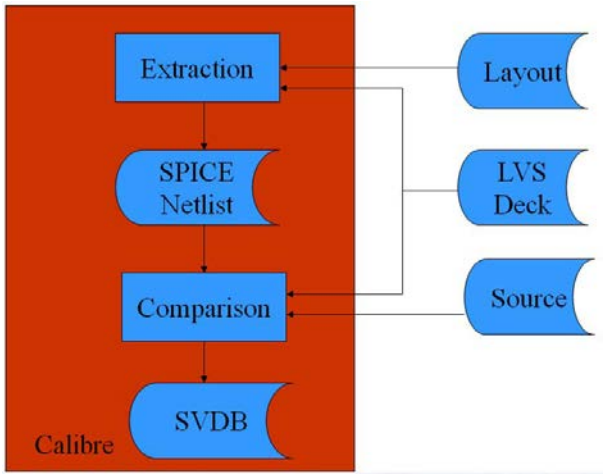
# Calibre RealTime DRC Integration to Pyxis



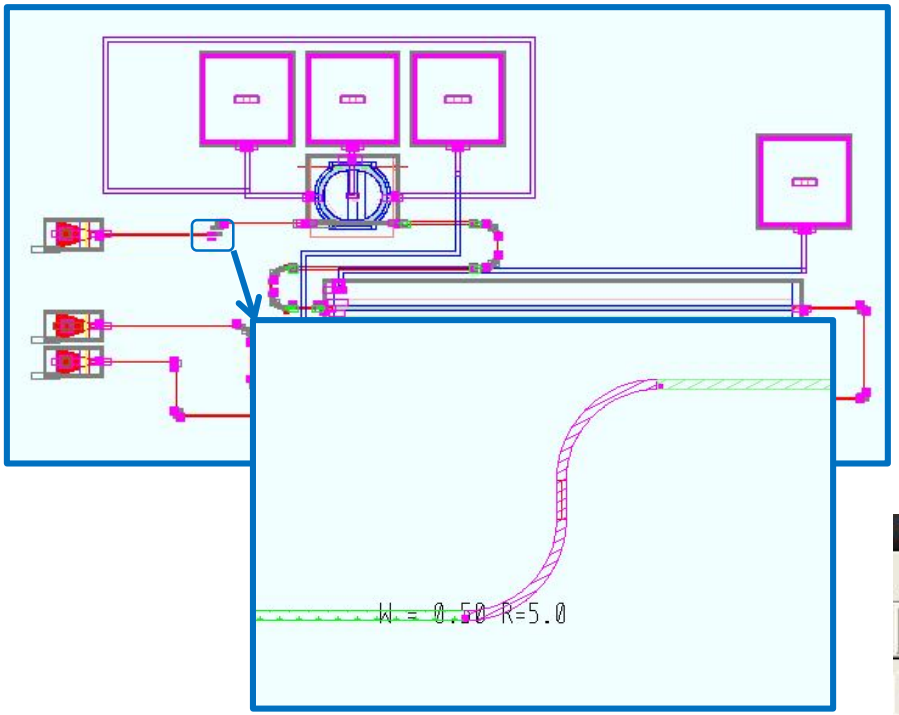
# Calibre Layout Extraction and Comparison

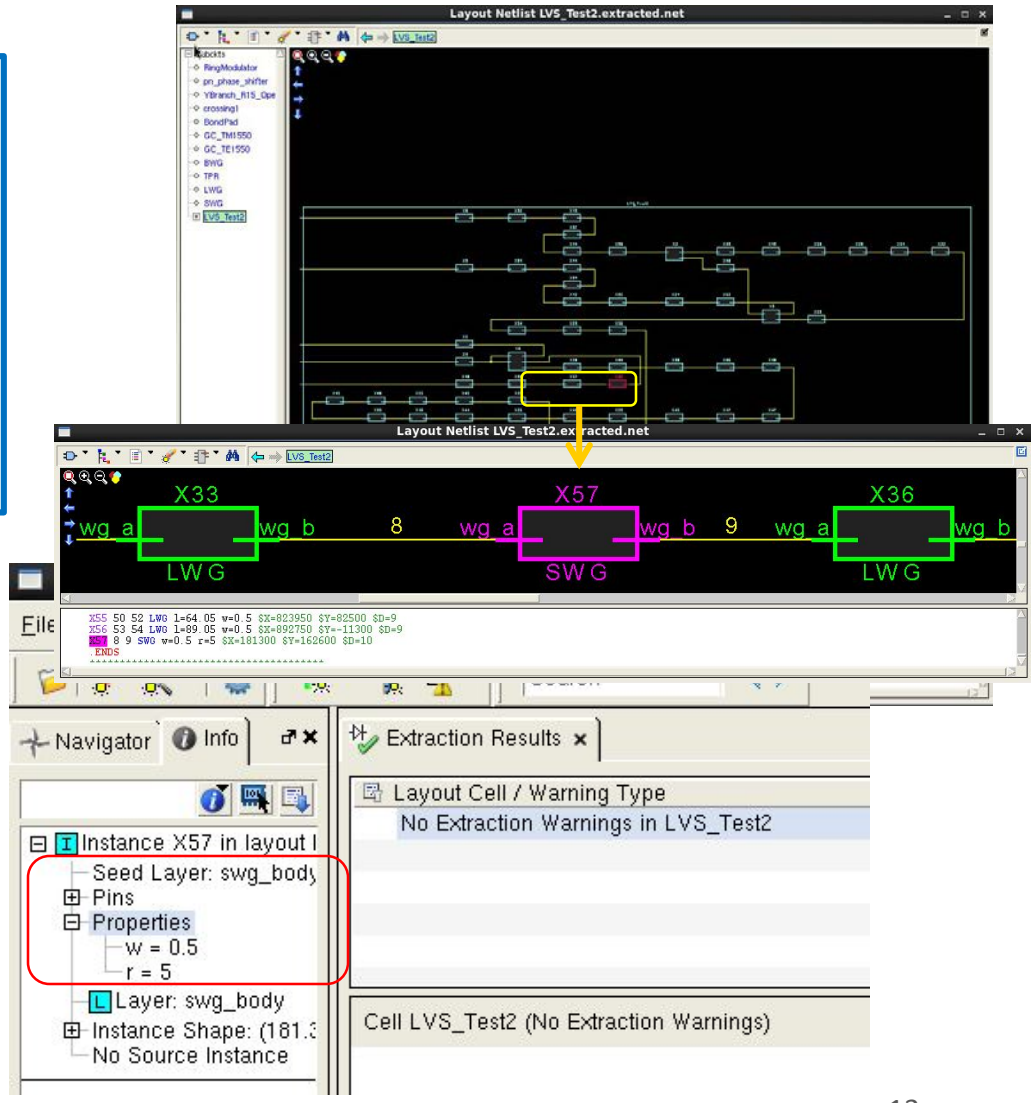
- Device Extraction
  - Device Parameter Extraction
- Interconnect Extraction
  - Wave guide lengths, widths, bend radii
- Use With or Without Comparison to a Source Netlist





# Calibre Layout Extraction: Arbitrary Curves

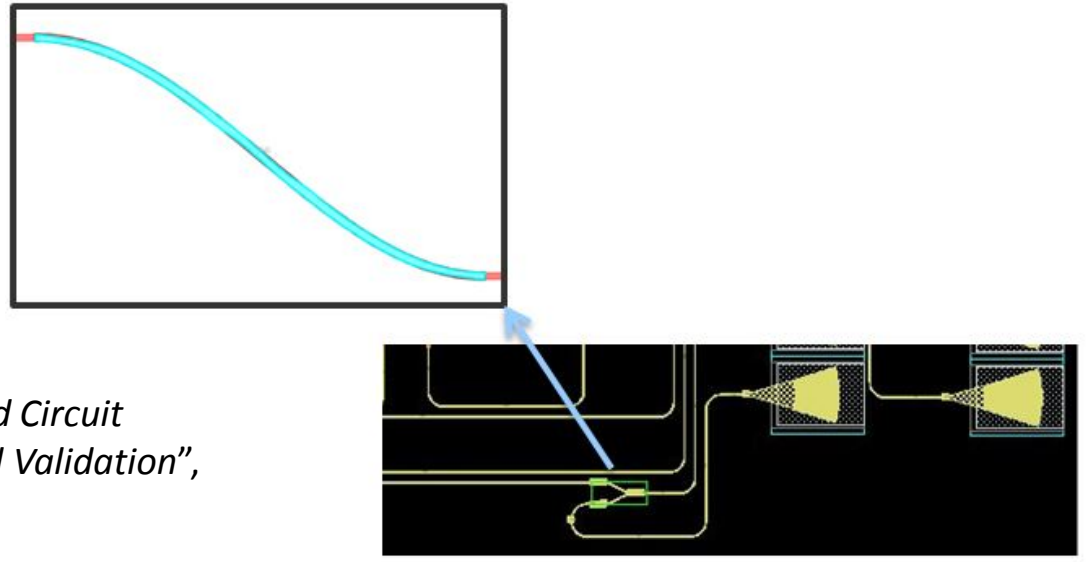



- Extracted Elements Captured to Spice
  - All devices and parameters
  - Interconnect parameters

# Calibre Photonic: Device Characterization

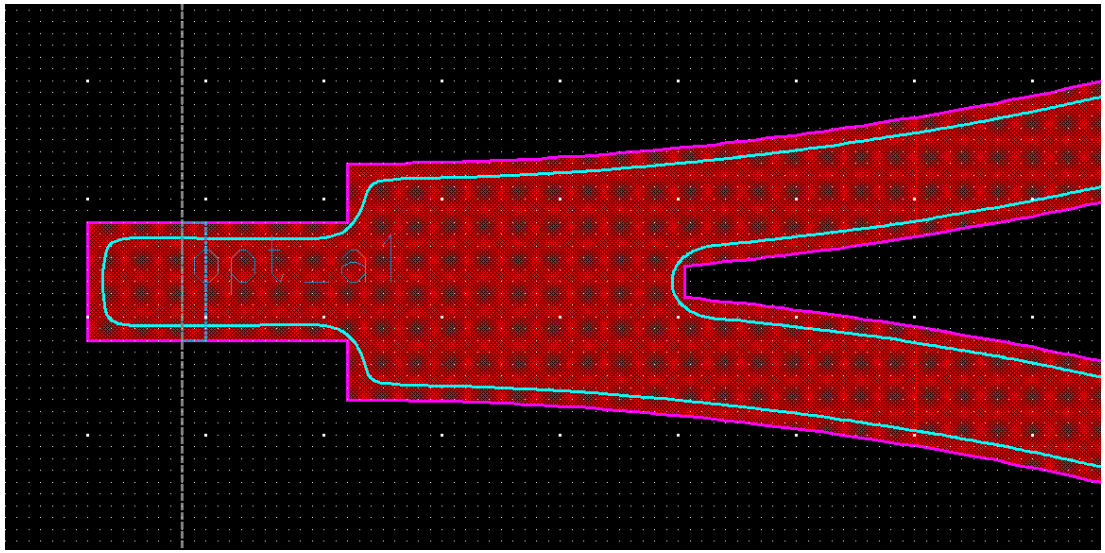
- Done by foundry, IP provider or device designer
- Compare layout to Calibre rendering of curve equation
  - Phoenix OptoDesigner for intended topology
  - Outliers output as DRC errors
  - Original parameters passed to extracted netlist



"*LVS Check for Photonic Integrated Circuit Curvilinear Feature Extraction and Validation*", to be presented at DATE 2015

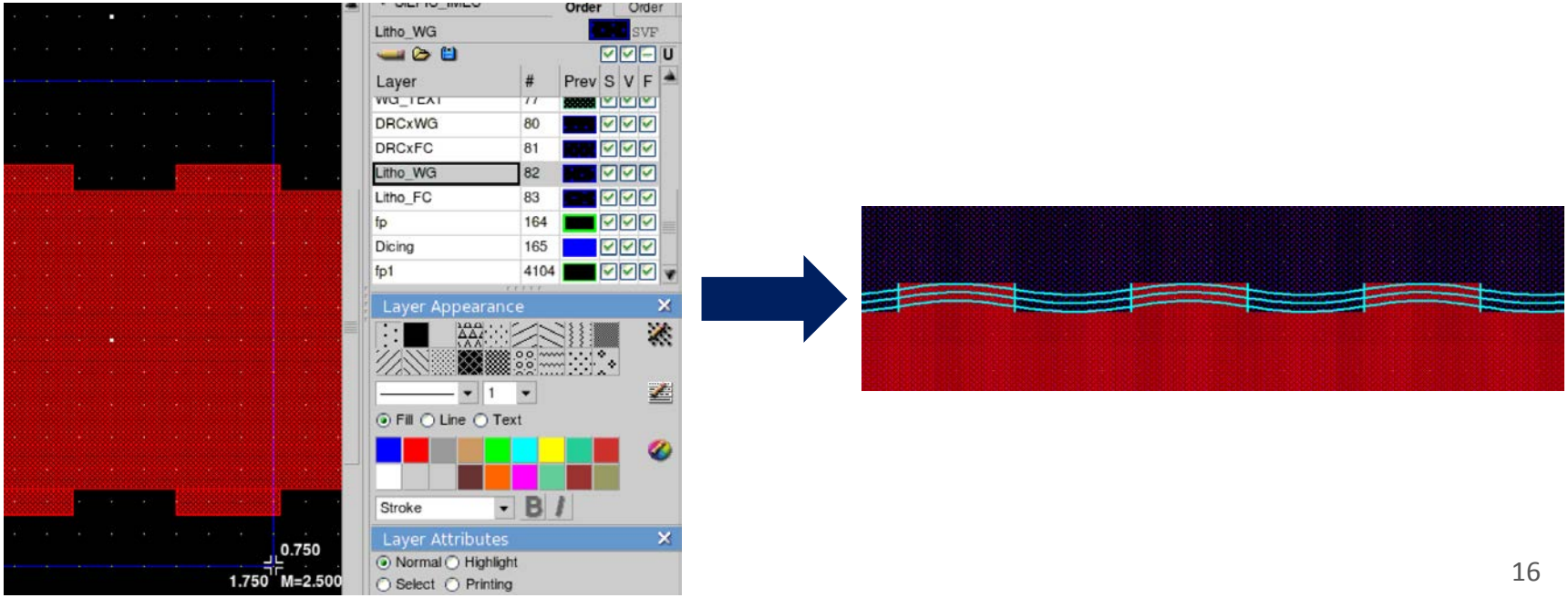
# Litho Impacts on Silicon Photonics

- **Optical Simulations Often do not Match Silicon Results**
  - **Litho simulation better captures ‘as manufactured’ structures**
- **Recommended Litho-Aware Device Characterization**
  - **Link to Lumerical FDTD improves device model parameters**
  - **Retargeting best practices to preserve intended topology**



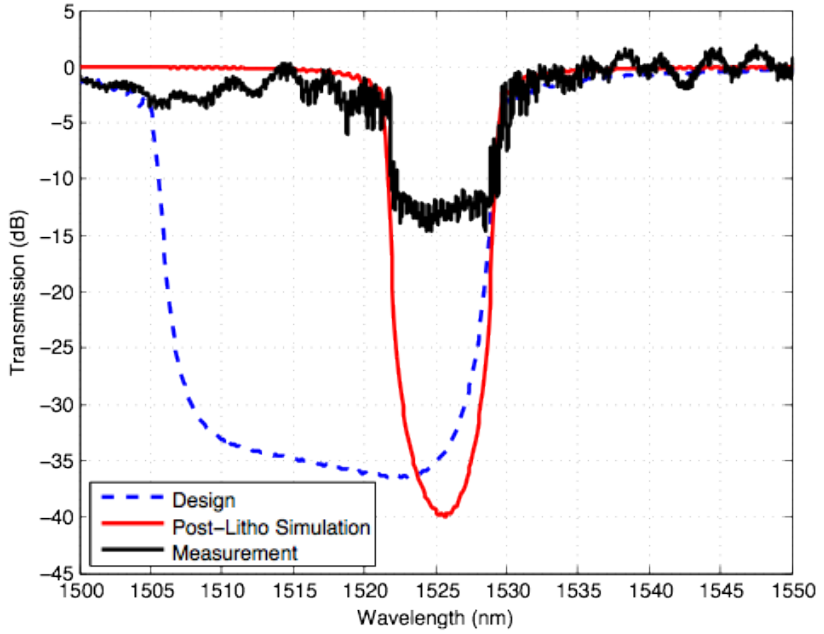
# Litho Impacts on Silicon Photonics

- **Waveguide Bragg Grating Example**
  - **Sharp edges of grating will smooth due to lithography resolution**
  - **This change in geometry will affect component attributes**
  - **Calibre LFD is used to simulate as manufactured geometric shapes**

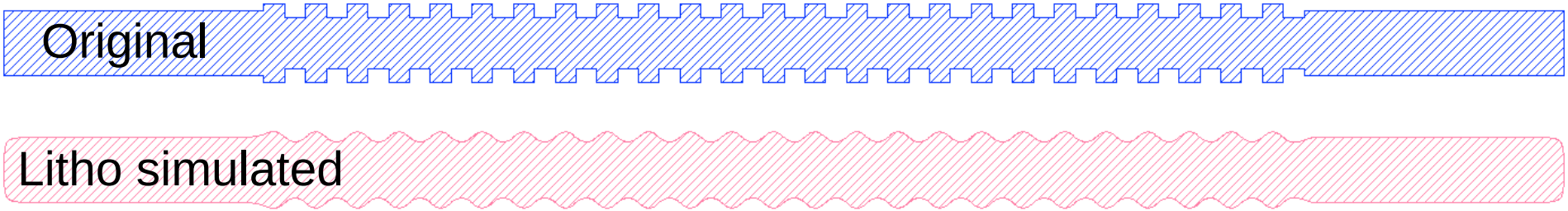


# Calibre Lithography Simulation: Waveguide Bragg Grating

- **Comparison of device designed with 40 nm square corrugations**
- **Litho Correction and FDTD Solutions simulations match experimental Bragg bandwidth**

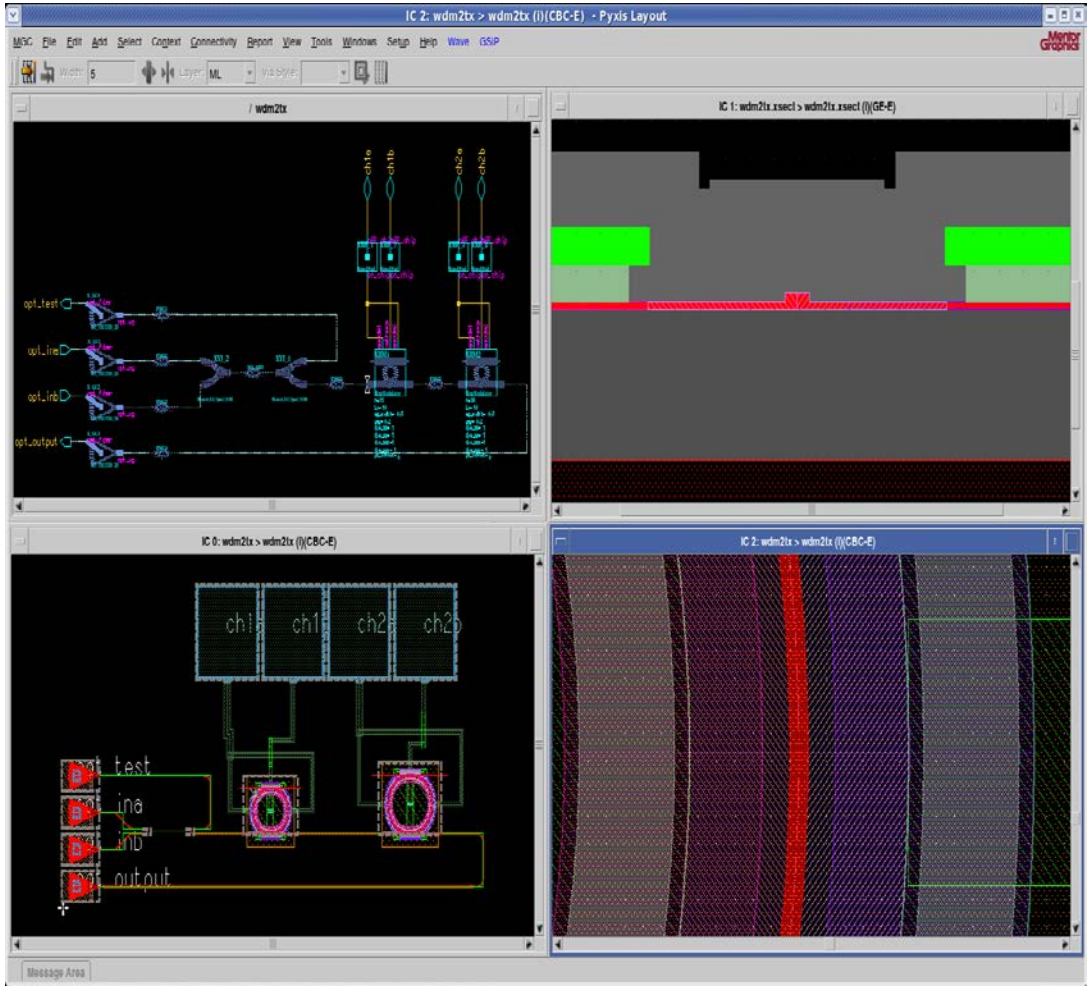



Xu Wang, et al., "**Lithography Simulation for the Fabrication of Silicon Photonic Devices with Deep-Ultraviolet Lithography**", *IEEE GFP*, 2012



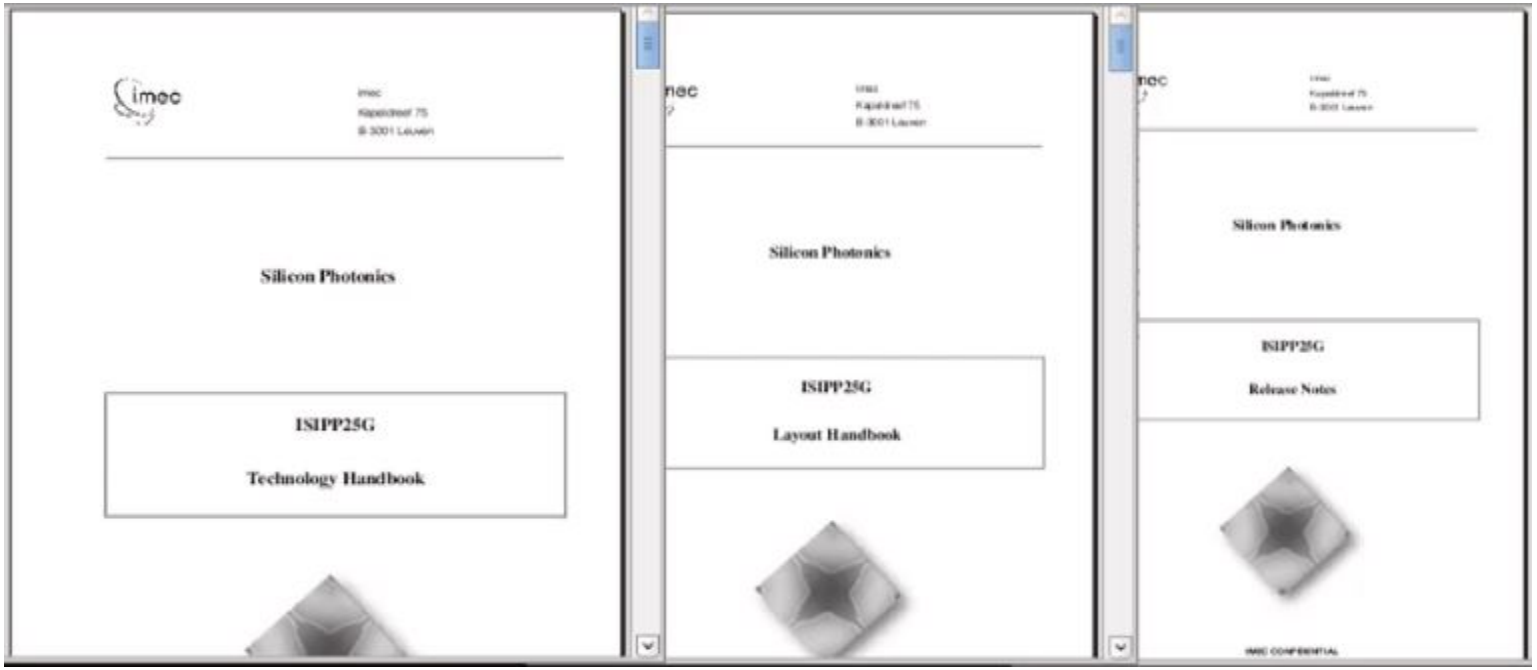
# Pyxis_GSiP Tutorial/Demo Available
# NDA neutral GSiP PDK with tutorial available from Mentor

- The Pyxis Wave reference packages provides extended features for Silicon Photonics PDK development
- Supports tiered custom PCell loading
- Waveguide routing enables full SDL flow
- Contains NDA neutral Silicon Photonics PDK created by University of British Columbia



# IMEC / SiEPIC / Mentor

- LVS – Layout versus schematic
  - LVS_v0.1 – waveguide connectivity and device recognition, Feb 2015
  - LVS_v0.2 – multiple cross-sections of waveguides and devices, Aug 2015
- Circuit Models
  - Circuit_models_V0.1 all passives and select actives, Aug 2015
- LFD – Lithography simulation support
  - LFD_v0.1 – Aug 2015



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