DATE 16
DESIGN, AUTOMATION & TEST IN EUROPE
14 – 18 March, 2016 · ICC · Dresden · Germany
The European Event for Electronic System Design & Test

Fabrication Non-Uniformity in Silicon Photonic Interconnects

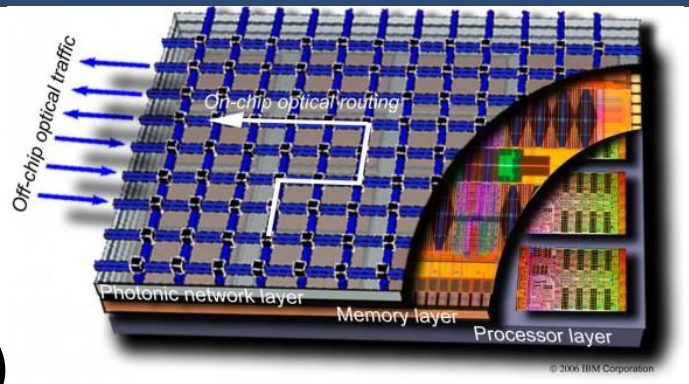
Mahdi Nikdast[1], Gabriela Nicolescu[1], Jelena Trajkovic[2], and Odile Liboiron-Ladouceur[3]

[1]Polytechnique Montréal, Montréal, Canada
[2]Concordia University, Montréal, Canada
[3]McGill University, Montréal, Canada

McGill
POLYTECHNIQUE MONTRÉAL
LE GÉNIE EN PREMIÈRE CLASSE
Concordia UNIVERSITY
NSERC CRSNG
Si-EPIC
RESMIQ
Regroupement Stratégique en Microsystèmes du Québec

Silicon Photonic Interconnects

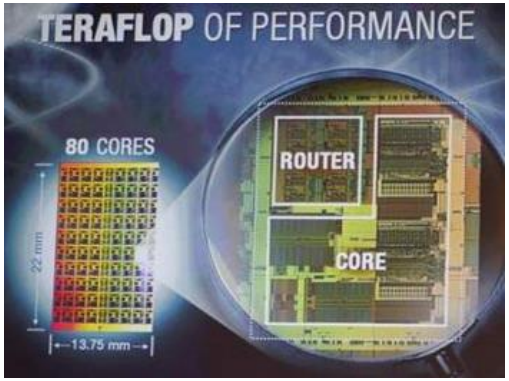
- Number of processor cores
- Metallic interconnects limitations
- Let there be light
- Wavelength Division Multiplexing (WDM)
- Challenges (Designed ≠ Fabricated)
  - Fabrication non-uniformity



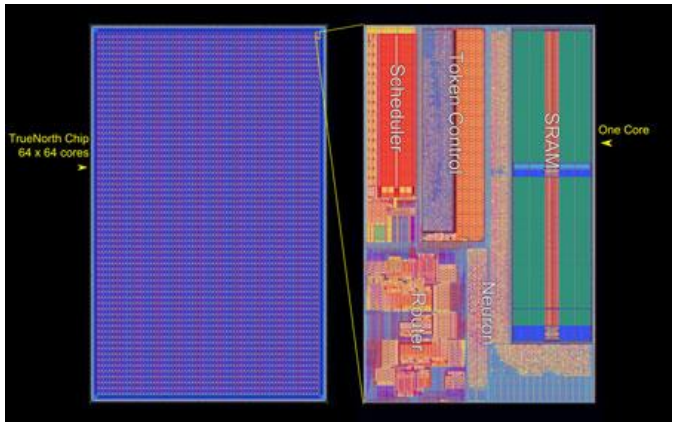
IBM ICON (Intra-Chip Optical Network)
3D-integated chip consists of several layers
(2006)

2006

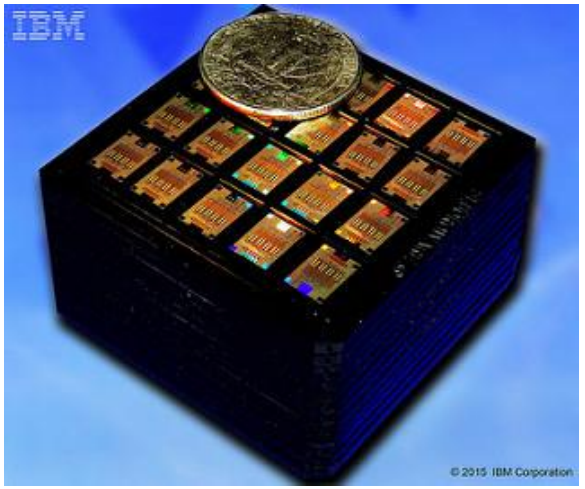
2015



Intel's Polaris chip: 8x10 mesh
(2007)



IBM's TrueNorth: 4096 cores
(2011~2014)



IBM's fully integrated wavelength multiplexed CMOS silicon photonics chip
(2015)

Outline

- **Fabrication non-uniformity in silicon photonics**
- **Proposed bottom-up approach**
- **Quantitative simulation results**
- **Fabrication**
- **Conclusion**

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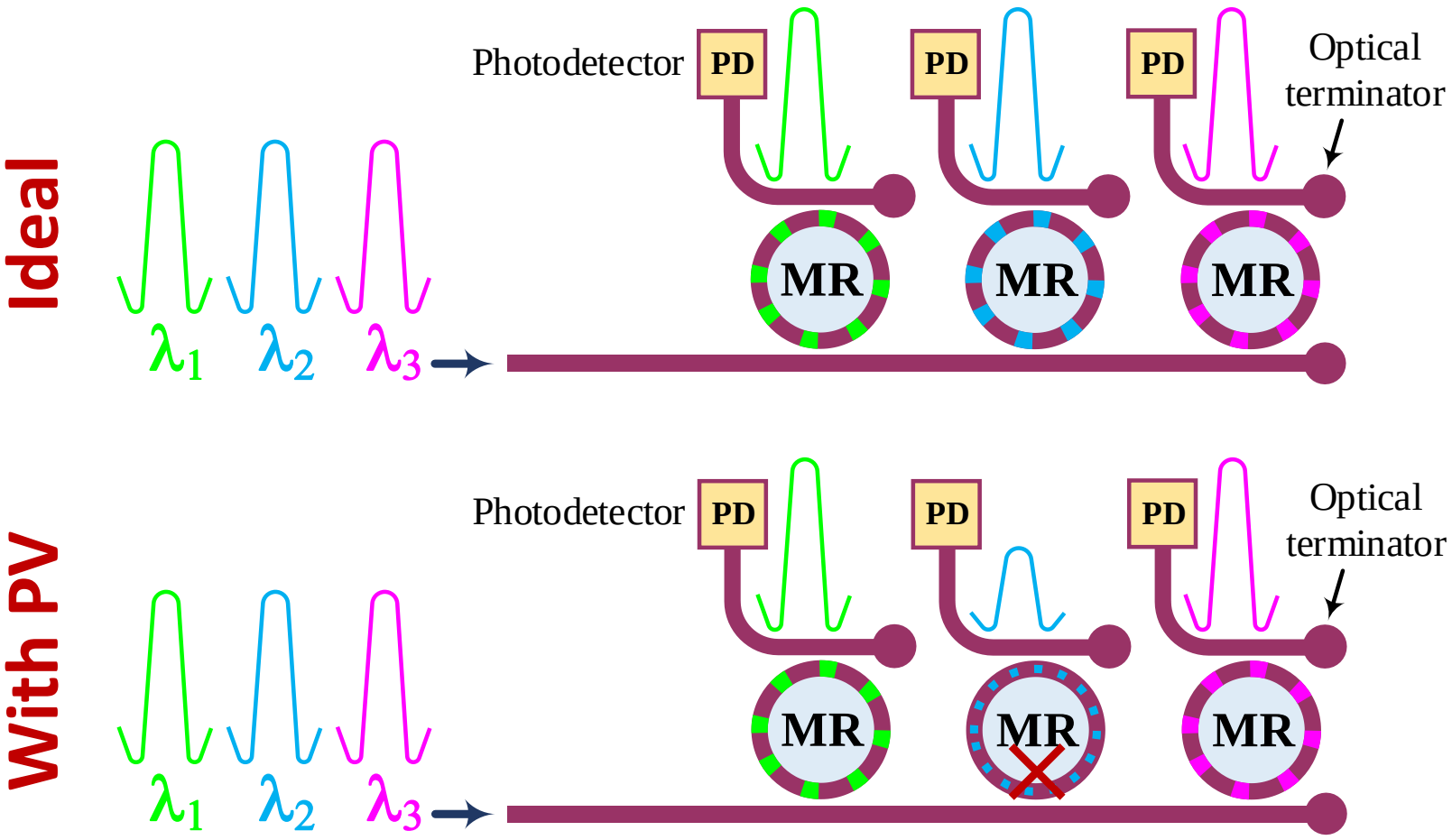
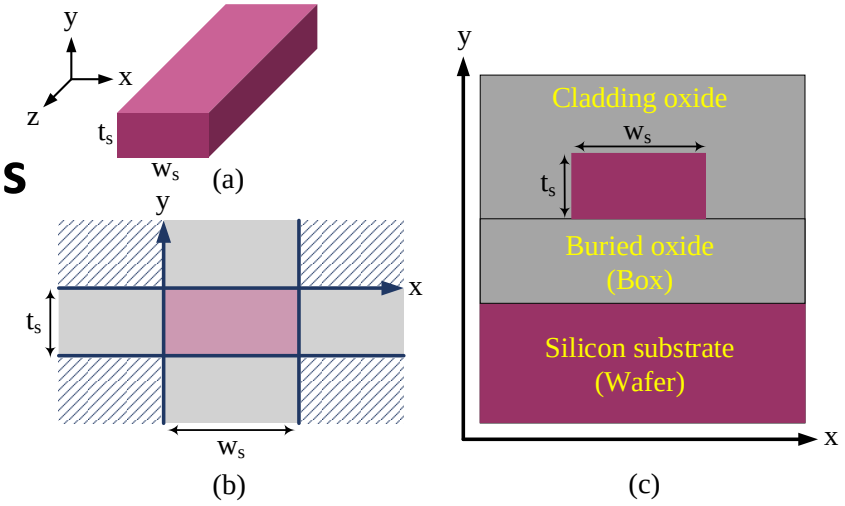
Fabrication Non-Uniformity

- **Fabrication-induced Process Variation (PV)**



Why Does It Happen?

- Optical lithography process imperfection
  - Resist sensitivity
  - Resist age or thickness
  - Exposure change
  - Etching
- Primary concerns
  - Waveguide width variations
  - Top silicon thickness variations



Different Perspectives

- No detailed analytical study on process variations
- Lack of tools
- Difficult problem to study
- Expensive problem
- Interaction between the two communities

- Characterize several identically designed devices
- Understand variations
- Lack of system perspective
- Consider process variation as an issue
- Corner analysis
  - Numerical simulations (e.g., FDTD)
  - Moderate computation cost

- Design solutions (e.g., channel relocation) (e.g., reliable design)
- Ignore/manage process variations
- Lack of device perspective
- Corner analysis
  - No tool available
  - Not feasible

Our Contribution

- A **computationally efficient and accurate** method
  - Explore different variations at both levels
  - PV study in large-scale photonic interconnects
  - Corner analysis at the system level

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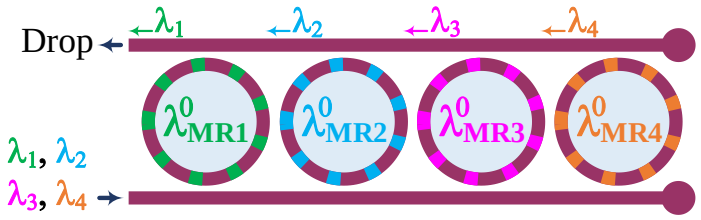
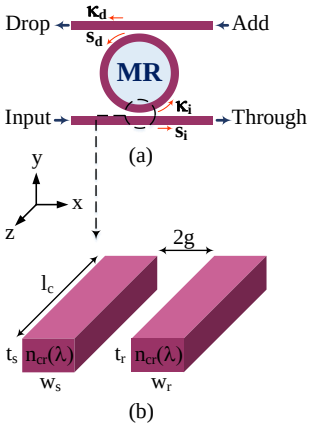
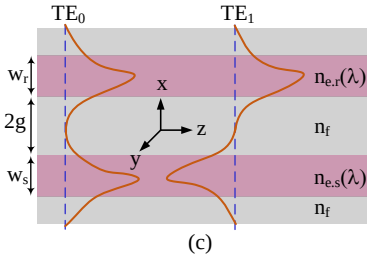
Methodology Overview

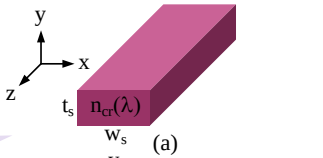
Supermode theory

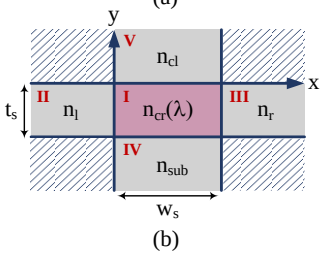
Marcatili's approach

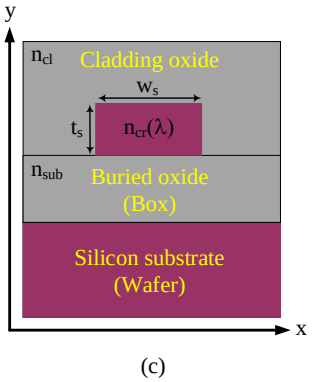


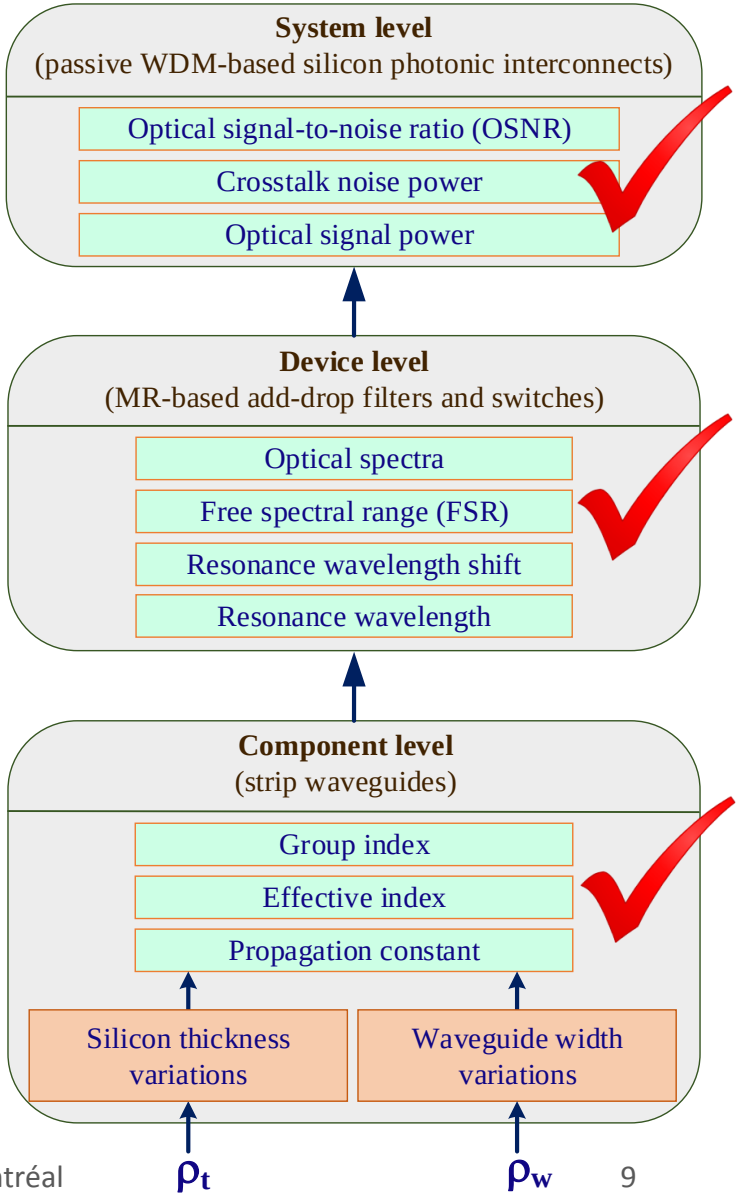












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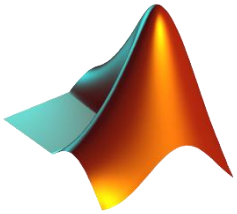
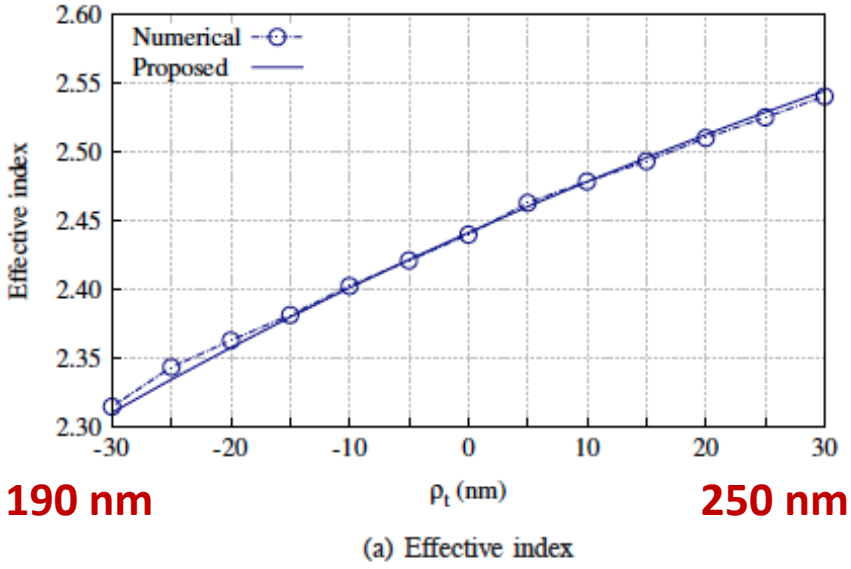
Quantitative Simulations



- Numerical simulator (use for evaluations)
  - MODE (Lumerical)
- MATLAB implementation
- Strip waveguides original dimensions
  - Width: 500 nm
  - Thickness: 220 nm
- Simulation parameters
  - Arbitrary variation range: [-30 , 30] nm
  - Central laser wavelength: 1550 nm
  - Gap (input/drop waveguide and MR): 200 nm
- Fundamental TE mode

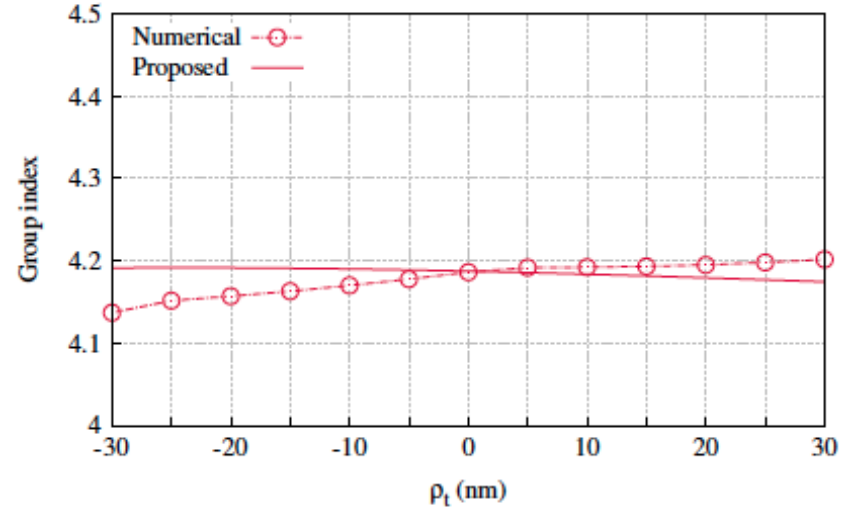
Effective and Group Indices

Thickness



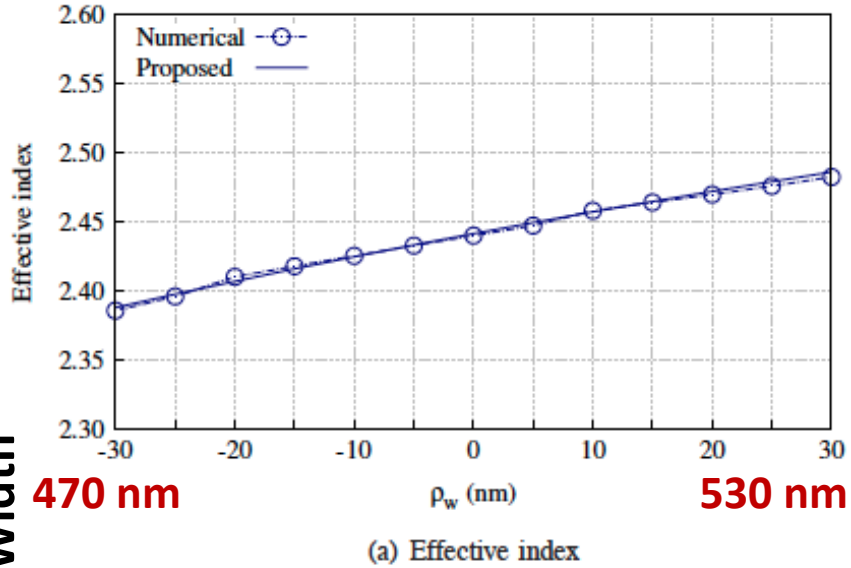
190 nm 250 nm

(a) Effective index



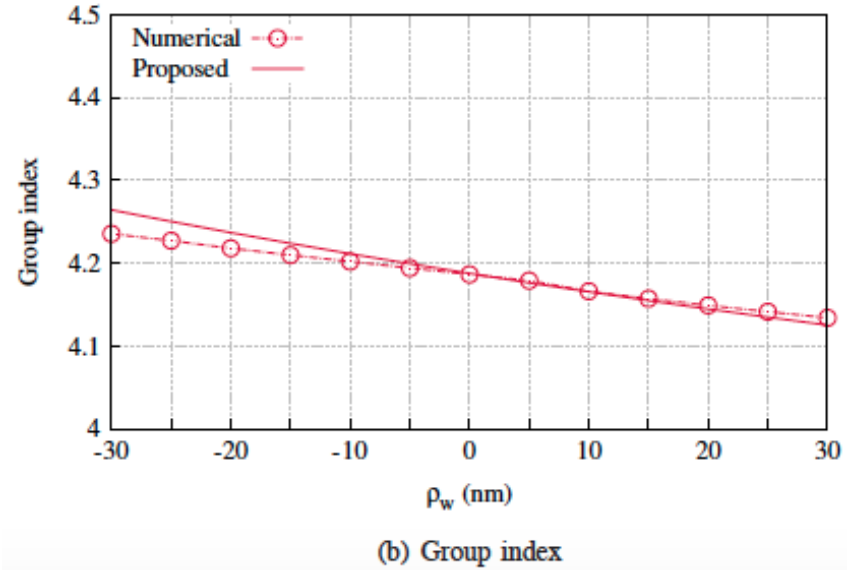
(b) Group index

Width



470 nm 530 nm

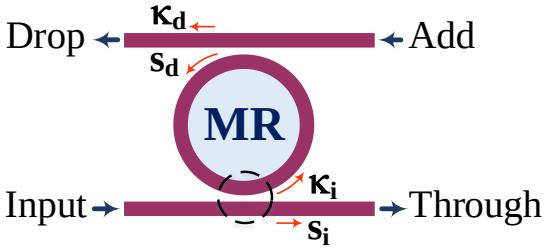
(a) Effective index



(b) Group index

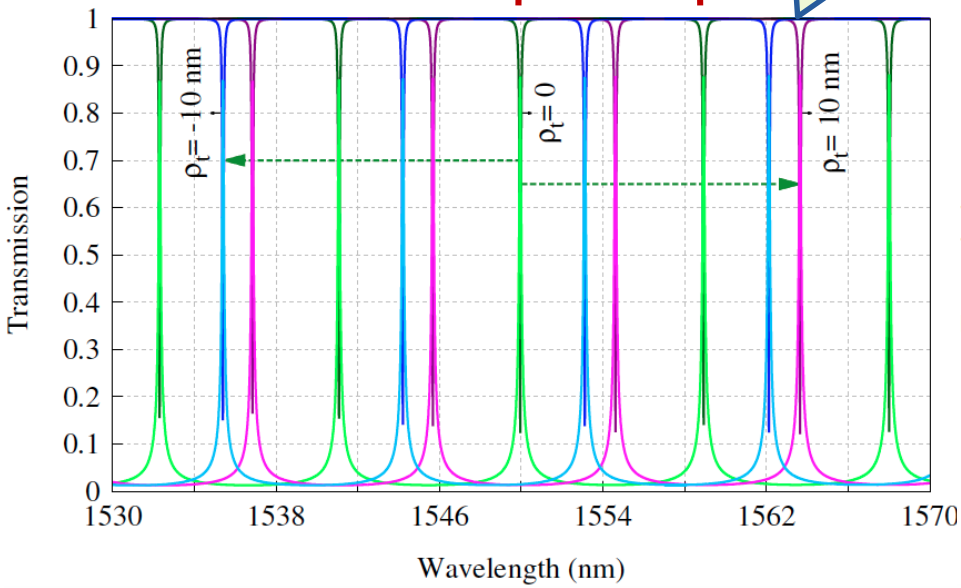
Optical Spectrum of an Add-Drop Filter

- radius r = 9 µm, coupler length l_c = 4 µm, gap 2g = 200 nm
- FSR≈ 9 nm

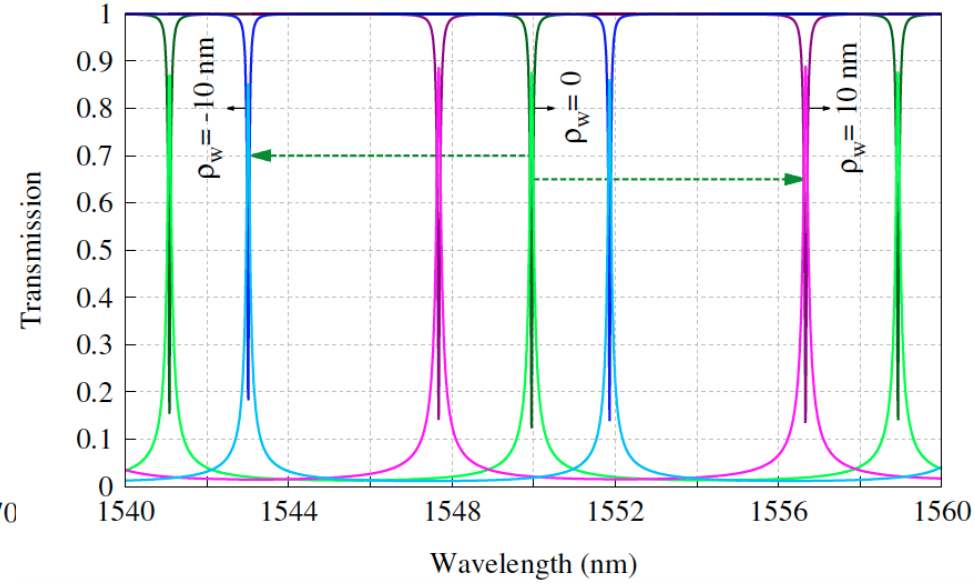


Free-Spectral Range (FSR)

$\Delta\lambda_{MR} > FSR$



Silicon thickness variations (±10 nm)



Waveguide width variations (±10 nm)

Complexity Comparison and Evaluation

- Proposed method vs. numerical simulation (MODE)
- Same computation platform
- All the results up to the system level

Method	Computation time	Average error rate
Numerical (MODE)	128 minutes	-
Proposed	54 seconds	1 %

- Speed-up: greater than 100x
- Average error rate 1%

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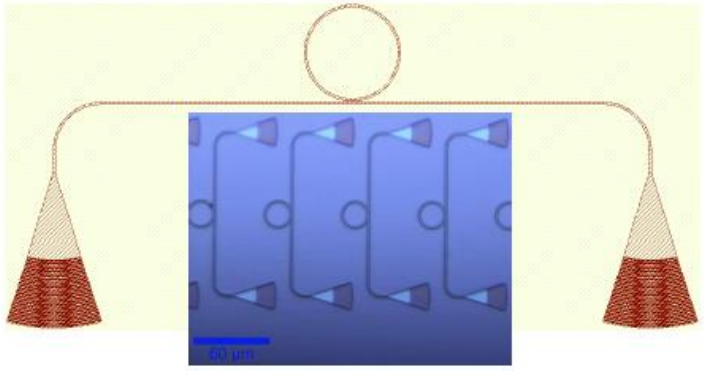
Fabrication Details

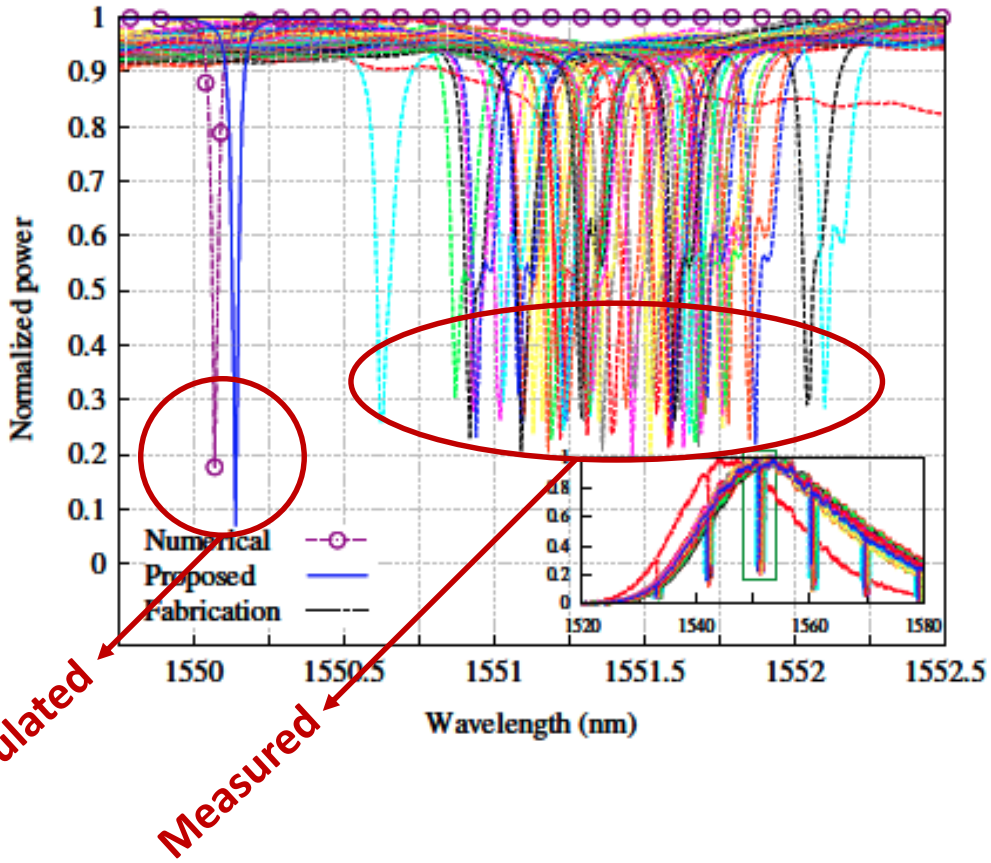
- 220 nm thick SOI strip waveguide with a 500 nm width
- TE polarization racetrack resonators
  - Radius= 10 µm
  - Coupler length≈ 1 µm
  - Gap= 200 nm
  - FSR≈ 9 nm



- Chip
  - Fabrication: Ebeam (U of Washington) (2 nm resolution)
  - Measurements: UBC (automatic probe station)
  - 2.1×4.5 mm^2
  - Sixty identical copies
  - Placed between 60 µm and 4.2 mm
- Within-die variations are studied

Resonance Wavelength Shift

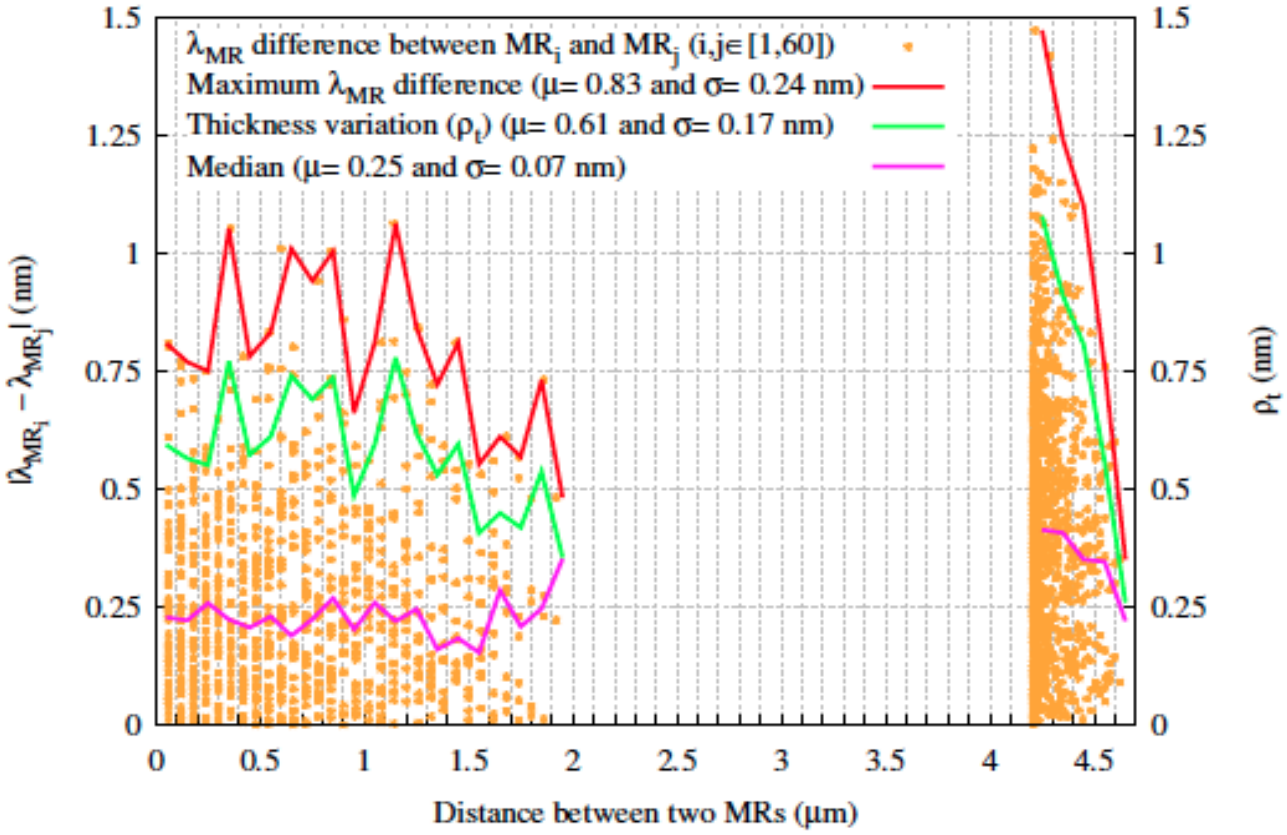
- 2.1 nm (worst-case) and 0.6 nm (best-case)
- Process variation
- No thermal variation
- Negligible width variations
- Thickness variations
  - 2 nm (worst-case)



Mahdi Nikdast, Gabriela Nicolescu, Jelena Trajkovic, and Odile Liboiron-Ladouceur, "Photonic Integrated Circuits: a Study on Process Variations," Optical Fiber Communication Conference and Exhibition (OFC), Anaheim, California, USA, March 2016.

Resonance Wavelength shift vs. Physical Distance

- **Compared each pair of MRs: $\binom{60}{2}$=1770**



Resonance wavelength difference vs physical distance

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Conclusion

- **Fabrication non-uniformity is an issue both at the Physical Level Design and System Level Design**
- **Proposed a computationally efficient and accurate method to study fabrication process variations in large-scale systems (100x, 1%)**
- **Corner analysis at physical level and system level**
- **Need MORE silicon photonics fabrications**

Thank You!

Mahdi Nikdast
E-mail: mahdi.nikdast@{polymtl/mcgill}.ca
Webpage: http://nikdast.com