Modelling and Analysis of Off-Chip Optical and Electrical Interconnect and Interface

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OPTICS Lab

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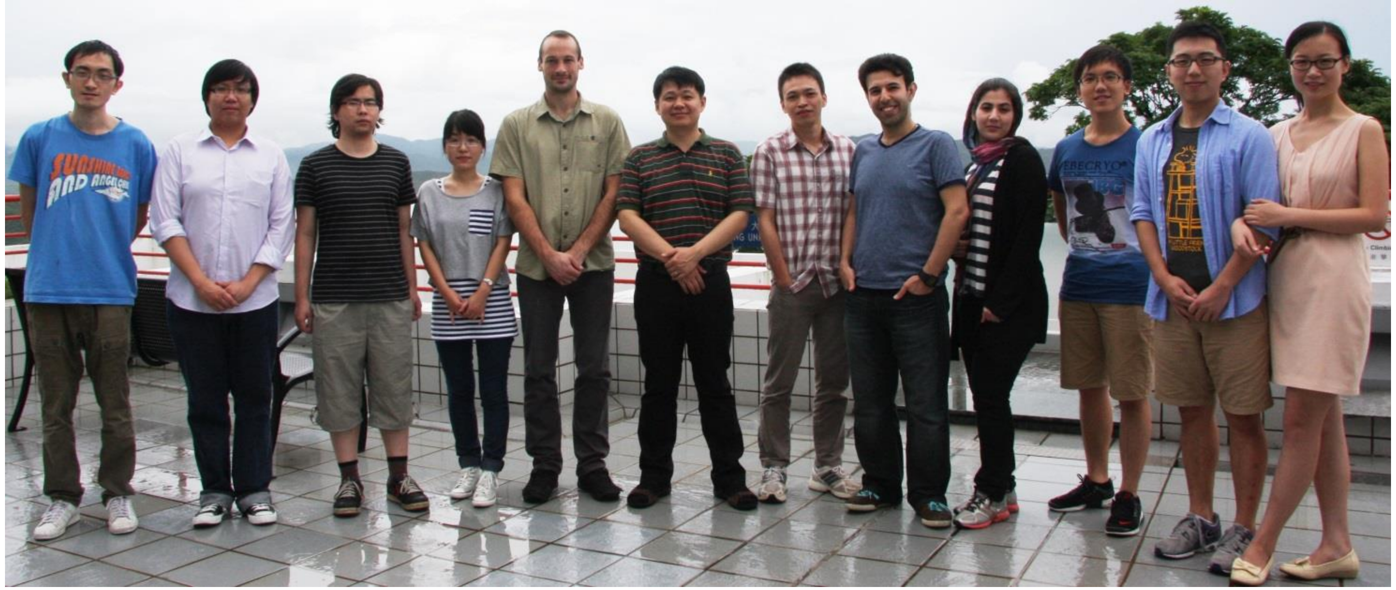

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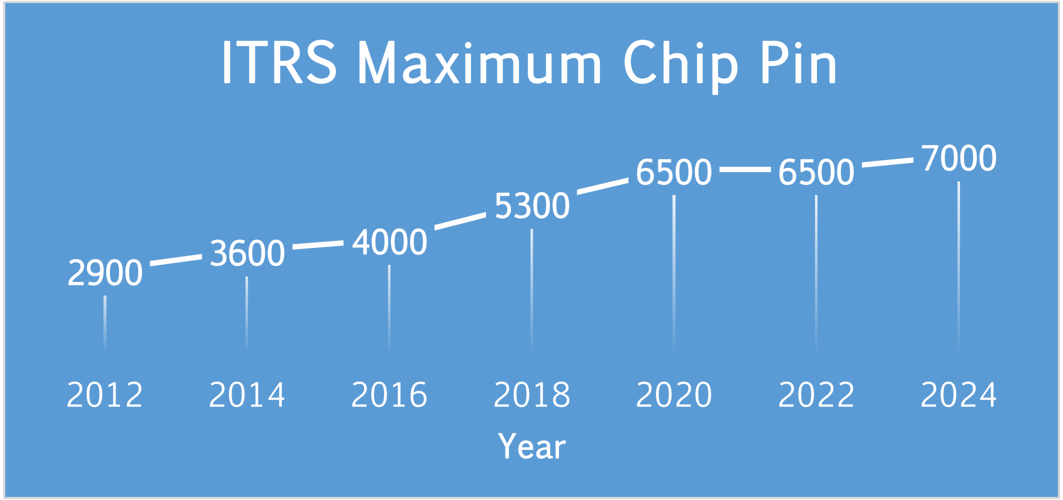
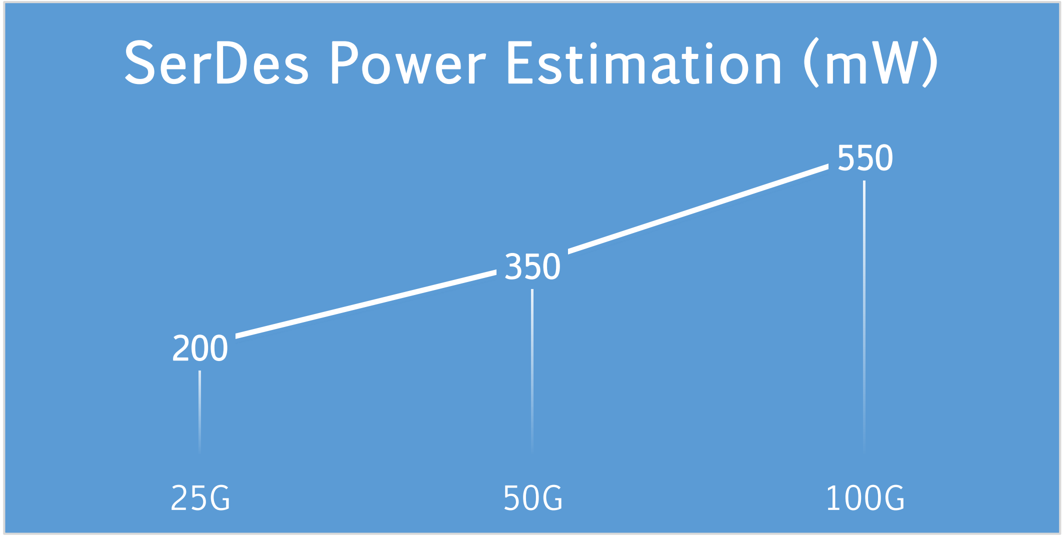
Challenges of Inter/Intra-Chip Electrical Interconnect

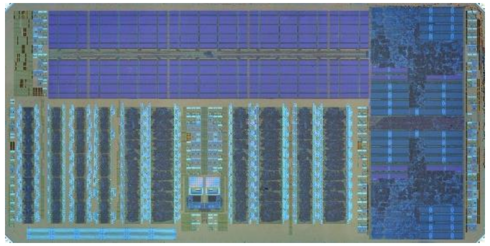
- More communications from more cores
  - Cisco QuantumFlow (40), Intel Phi (72), Tilera Tile (72), PicoChip (300) ...
  - Blade server, micro server, disaggregated server ...
- Tighter I/O bandwidth
  - Maximum pin count of package grows slow
  - Higher packaging and PCB cost
- Larger latency
  - Multiple clock cycles are required to cross a chip
- Higher energy consumption and loss
  - Dynamic and leakage power of drivers and buffers
  - ~35dB/m @12.5G on high-quality PCB
- SerDes energy and performance bottleneck
  - ~5pJ/bit @ 100G





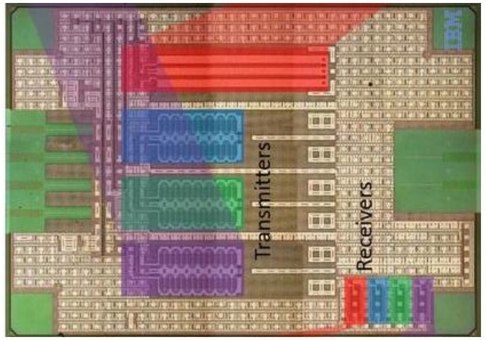
Optical Interconnect

- Photonic technologies have been successfully used in WAN and LAN
  - Showed strengths in multicomputer systems and Internet core routers
- Benefit from more matured silicon-based technologies
  - Micron-scale devices working at picosecond-level are widely demonstrated
- Commercialization efforts
  - IBM, Intel (Omni-Path), HP (Machine), Oracle (UNIC), STMicro, NTT, NEC, Fujitsu (PECST), Huawei …
  - Startups: Luxtera-STMicro, Lightwire/Cisco, Kotura/Mellanox, Caliopa/Huawei, Aurrion, OneChip, Skorpios …
  - EDA: Cadence-PhoeniX-Lumerical, Mentor Graphics-Lumerical, RSoft/Synopsys …
- Questions remain: What? How? & Why?



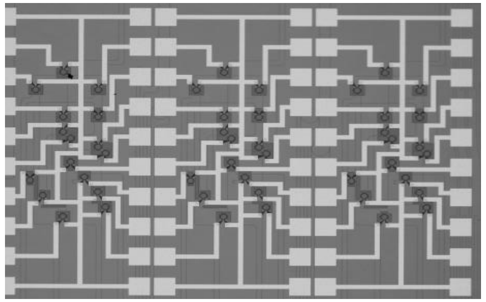
Integrated OE Interfaces & Processor

C. Sun *et al.*, “Single-chip microprocessor that communicates directly using light”, Nature 2015



Integrated OE Interfaces

D.M. Gill, *et al.*, “Demonstration of Error Free Operation Up To 32 Gb/s From a CMOS Integrated Monolithic Nano-Photonic Transmitter”, CLEO 2015

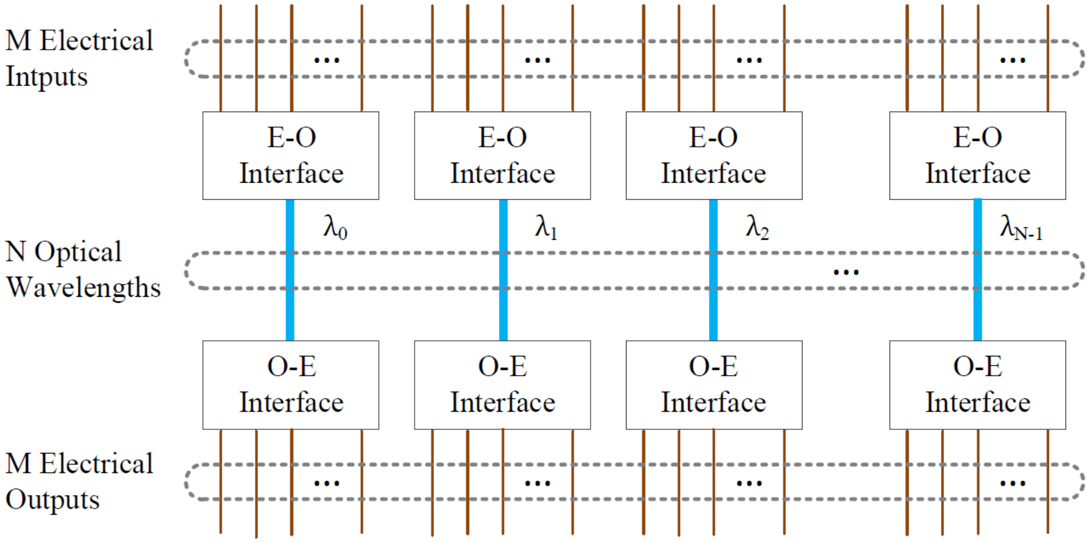


Integrated Optical Switches

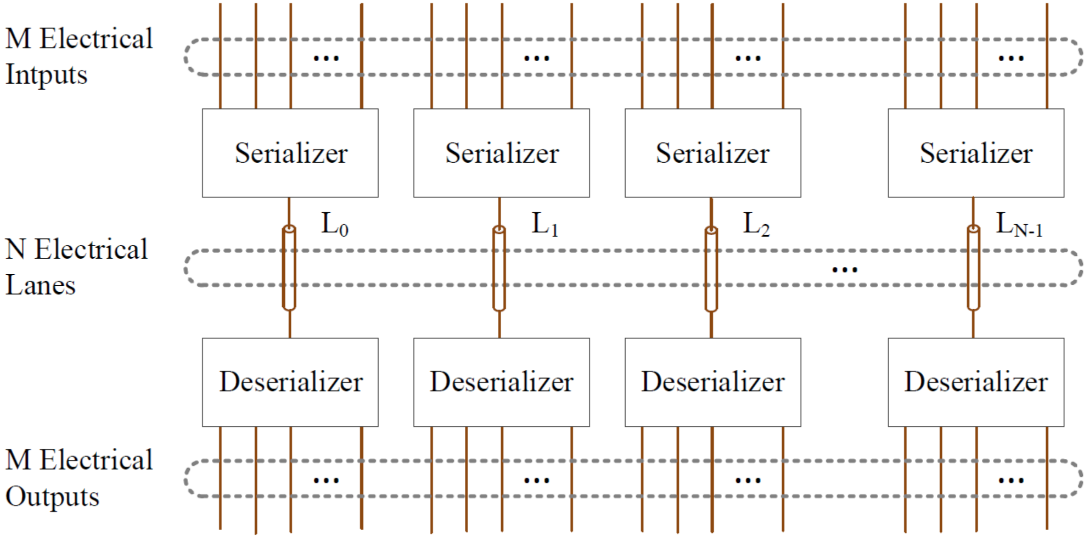
R. Ji, J. Xu, L. Yang, “Five-Port Optical Router Based on Microring Switches for Photonic Networks-on-Chip”, IEEE Photonics Technology Letters, March, 2013

Off-Chip Interconnect Overview

- Optical interconnect OI(M,N) include
  - M electrical inputs
  - M electrical outputs
  - N optical wavelengths



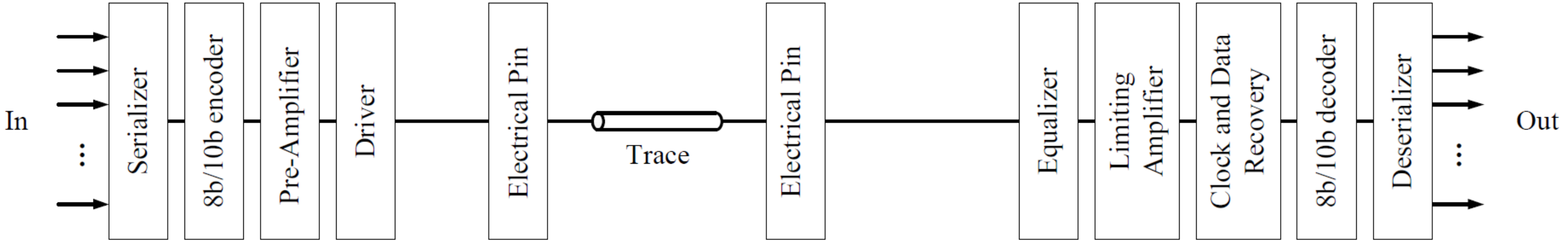
- Electrical interconnect EI(M,N) include
  - M electrical inputs
  - M electrical outputs
  - N electrical lanes



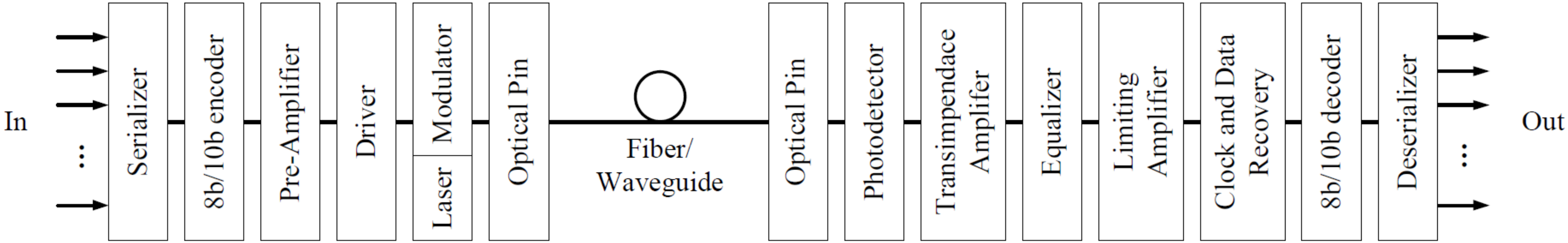
* Zhehui Wang, Jiang Xu, *et al*, “A Holistic Modelling and Analysis of Optical-Electrical Interfaces for Inter/Intra-chip Interconnects,” IEEE TVLSI 2016
* Zhehui Wang, Jiang Xu, *et al*, “Improve Chip Pin Performance Using Optical Interconnects,” IEEE TVLSI 2015

Off-Chip Interconnect Structure Examples

- Electrical off-chip Interconnect



- Optical off-chip Interconnect



Holistic Models and Comparisons

- Optical interconnects vs. electrical Interconnects
  - Bandwidth
  - Area and linear bandwidth density
  - Latency
  - Energy efficiency
  - Signal integrity
  - Area
- OE interfaces
- SerDes designs
- Packaging options
- Different structures

Outline

- Introduction
- Modelling off-chip interconnects and interfaces
  - Electrical Interconnects
  - Optical Interconnects
  - SerDes and O-E interface
- A new O-E interface
- Quantitative analysis and comparisons
- Conclusions

Basic Design Parameters

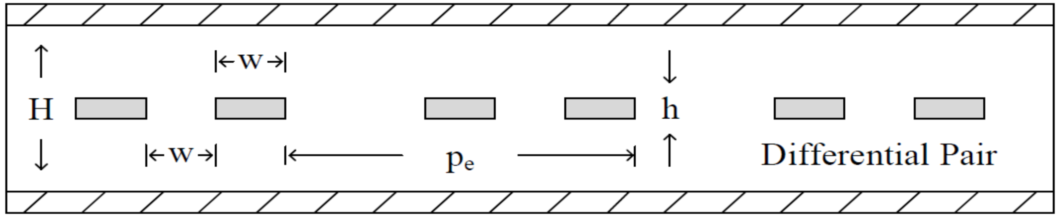
	Saraswat	Chen	Esener	OEIL
1 Energy Efficiency			✓	✓
1.1 Power Consumption	✓	✓	✓	✓
1.1.1 Transmitter Power	✓	*	✓	✓
1.1.1.1 Crosstalk Noise				✓
1.1.1.1.1 Number of Wavelengths				✓
1.1.1.1.2 Wavelength Spacing				✓
1.1.1.1.3 MR Characteristics				✓
1.1.1.2 Optical Power Loss			✓	✓
1.1.1.2.1 Coupler Loss				✓
1.1.1.2.2 Waveguide Attenuation				✓
1.1.1.2.3 Interconnect Length				✓
1.1.1.2.4 MR Characteristics	✓			✓
1.1.1.3 Receiver Sensitivity	✓			✓
1.1.1.3.1 Photodetector Responsively	*			✓
1.1.1.3.2 Signal to Noise Ratio	*			✓
1.1.1.3.3 Modulation Frequency	*			✓
1.1.1.3.4 TIA Transimpedance				✓
1.1.1.3.5 Limiting Amplifier Sensitivity				✓
1.1.1.4 Laser & Modulator Parameters	✓	*	*	✓
1.1.1.4.1 Threshold Current			*	✓
1.1.1.4.2 Slope Efficiency	✓		✓	✓
1.1.1.4.3 Power Extinction Ratio	✓	*	✓	✓

	Saraswat	Chen	Esener	OEIL
1.1.2 Receiver Power	*	✓	✓	✓
1.1.2.1 TIA Power	*	✓	✓	✓
1.1.2.1.1 Photodetector Capacitance	*		✓	✓
1.1.2.1.2 Signal Frequency	*			✓
1.1.2.1.3 TIA Supply Voltage		✓	✓	✓
1.1.2.2 LA Power	*	✓	✓	✓
1.1.2.2.1 LA Supply Current		✓	✓	✓
1.1.2.2.2 LA Supply Voltage		✓	✓	✓
1.2 Data Rate	*			✓
2 Bandwidth Density		*		✓
2.1 Data Rate per Wavelength		*		✓
2.2 Number of Wavelengths		*		✓
2.2.1 MR Characteristics				✓
2.2.2 Wavelength Spacing				✓
2.3 Optical Pin Pitch				✓
2.4 Waveguide Pitch		✓		✓
3 Latency		✓		✓
3.1 RC Delay		✓		✓
3.2 Propagation Delay		*		✓
3.2.1 Interconnect Length				✓
3.2.2 Signal Propagation Speed		*		✓

* Mentioned but without an exact model

Electrical Crosstalk Noise

- Top/bottom layer for power/ground and inner layer for signal
- The differential traces on PCB board has the following parameters:
  - *H* height between two panels
  - *w* width of a trace
  - *h* height of a trace
  - P_e pitch of differential traces:



- *C(d)* is the crosstalk noise coefficient of two traces with distance *d*

$$c(d) = H^2/(4d^2 + H^2)$$

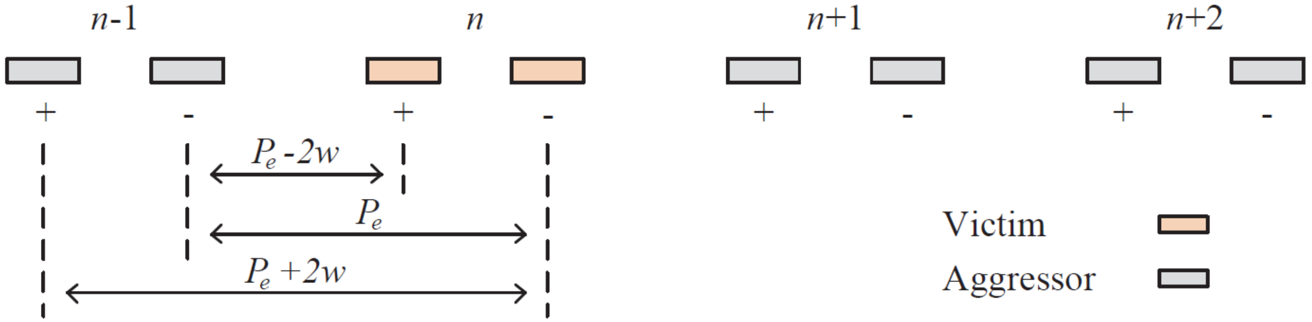
Electrical Crosstalk Noise

- $N_d(i)$ is the crosstalk noise coefficient between two differential pair n and pair $n+i$

$$N_d(i) = c(|i|p_e - 2w) - 2c(|i|p_e) + c(|i|p_e + 2w)$$

- The total crosstalk noise coefficient is the summation of coefficients from neighboring pairs

$$\varepsilon_e = \ldots + N_d(-1) + N_d(1) + N_d(2) + \ldots$$



Electrical Interconnect Attenuation

- The attenuation factor of PCB trace has two terms, which are skin effect loss and dielectric loss
  - R_{dc} direct current resistance
  - Z_0 characteristic impedance
  - f_s frequency of half skin depth
  - C_0 the capacitance per unit length
  - $tan\delta_D$ loss tangent in dielectric material

$$\alpha_e = \underbrace{\frac{R_{dc}(w+h)}{2Z_0 w}\left(\frac{f}{f_s}\right)^{0.5}}_{\text{Skin effect loss}} + \underbrace{\pi f C_0 tan\delta_D Z_0}_{\text{Dielectric loss}}$$

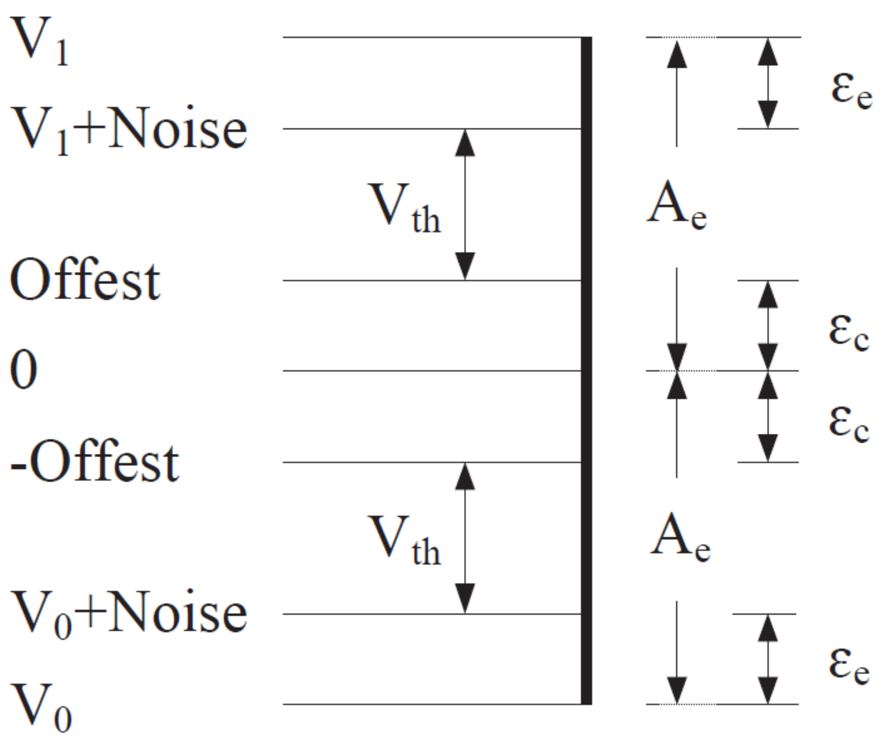
- The total attenuation of electrical interconnects
  - η_e coupling loss of electrical pin
  - f working frequency
  - L interconnect length

$$A_e = \underbrace{\eta_e^2}_{\text{Coupling loss}} \underbrace{e^{-\alpha_e L}}_{\text{Propagation loss}}$$

Electrical Interconnect Sensitivity

- Only when this voltage difference is grater than $|V_{th}|$ of the limiting amplifier, signals can be detected
  - A_e attenuation (0~1)
  - ε_e crosstalk noise coefficient
  - ε_o receiver offset coefficient:
- The supply current of driver
  - V_{th} threshold voltage
  - Z_d differential impendence

$$I_0 = \frac{2V_{th}}{(A_e - \epsilon_e - \epsilon_0) \cdot Z_d}$$

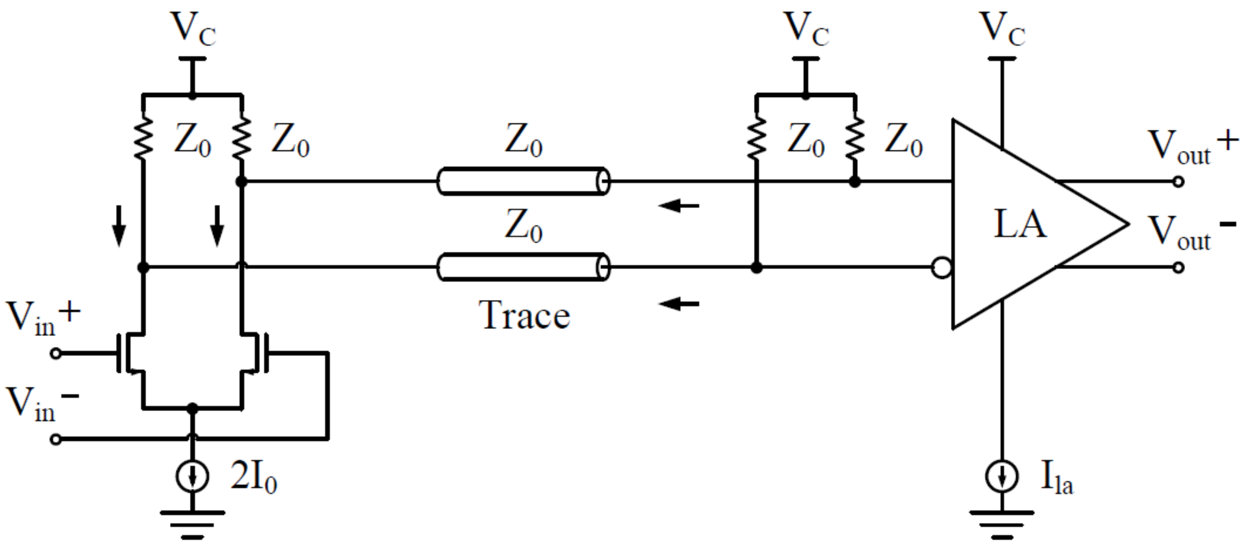


Ratio= $A - \varepsilon_e - \varepsilon_c = \Delta\varepsilon > 0$

Electrical Interconnect Power Consumption

- In electrical interconnect, power consumption includes the power of driver, receiver and SerDes
  - P_{sd} power of SerDes
  - V_c supply voltage
  - I_{la} supply current of limiting amplifier

$$P_e = P_{sd} + (2I_0 + I_{la})V_c$$



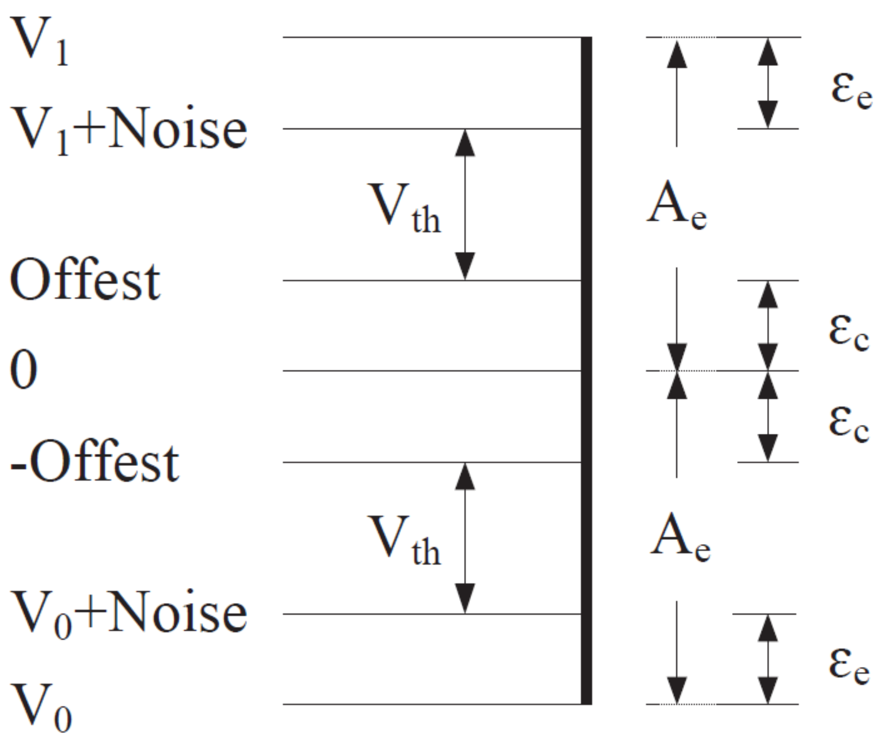
Electrical Interconnect Bandwidth

- If the signal frequency or the interconnect length is increased, trace attenuation is increased. The ratio Δε of the receiver amplitude over transmitter amplitude, will be decreased

$$A - \varepsilon_e - \varepsilon_c = \Delta\varepsilon$$

- The maximum bandwidth of electrical interconnect

$$\mathrm{B}_e = 2\mathcal{A}^{-1}(-\frac{\ln(\varepsilon_e + \varepsilon_c + \Delta\varepsilon)}{L})$$

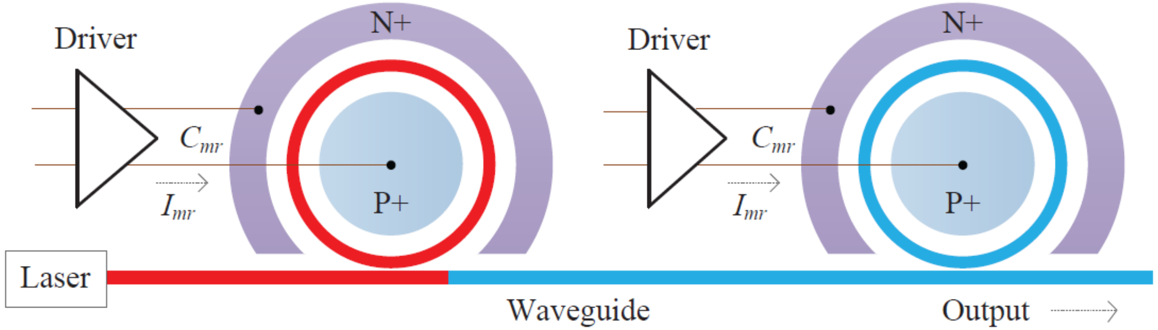


Microresonator

- Power of driver P_d: each time the voltage level of the PN junction is reversed, it is charged or discharged by the driver
  - C_m input capacitance
  - V_m supply voltage
- Power of microresonator P_m: when the voltage level of the PN junction is high, it is forward biased
  - I_m static current

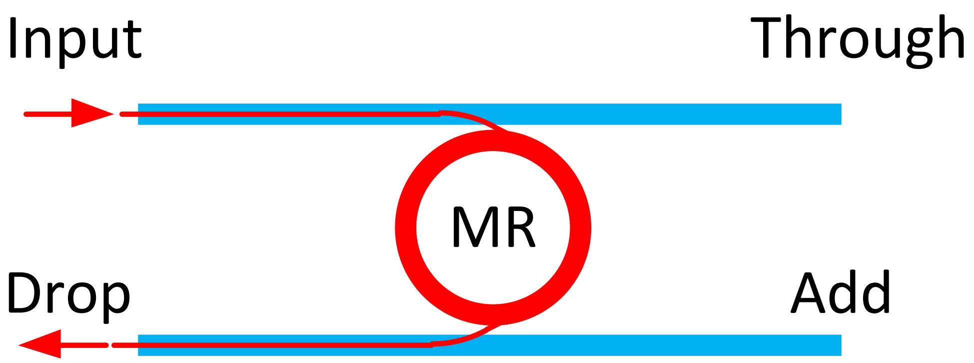
$$P_d = f \cdot C_m \cdot V_m^2$$

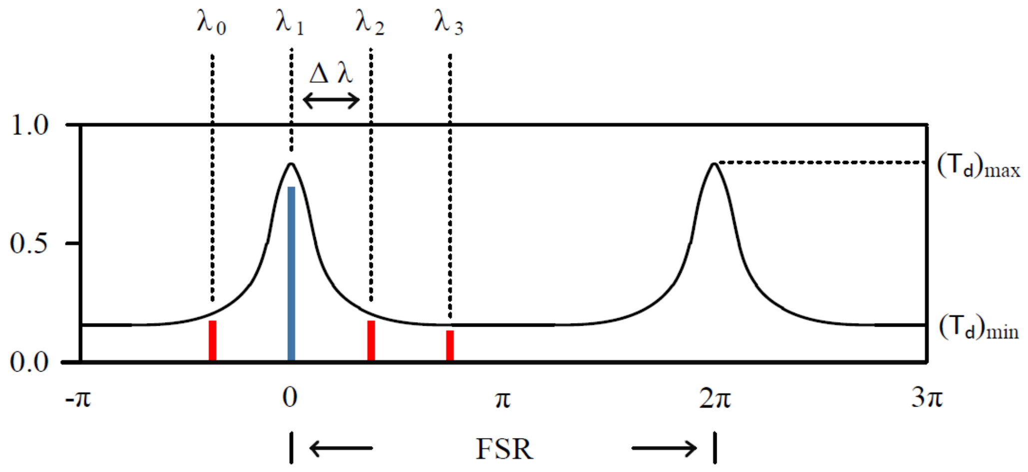
$$P_m = I_m \cdot V_m$$



Optical Crosstalk Noise

- At the receiver side, there are multiple optical signals in different wavelengths
  - λ_0 , λ_1 , λ_2 .... λ_n
- Part of the signal power in wavelength λ_0 , λ_2 and λ_3 will also appear on the drop port





Optical Crosstalk Noise

- In micro-resonator with working wavelength λ_1, the drop port transfer function is
  - $cos\theta(\lambda)$ function of working frequency λ
  - r power splitting ratio
  - a round trip attenuation

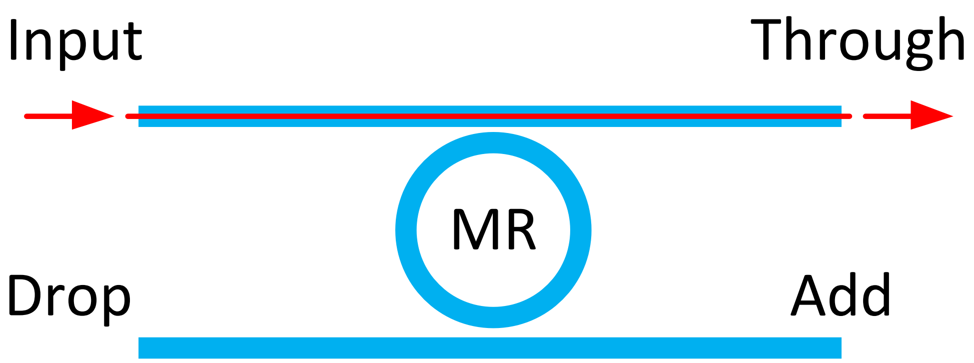
$$T_d(\lambda) = \frac{(1-r^2)^2 a}{1 - 2r^2 a \cos\theta(\lambda) + r^4 a^2}$$

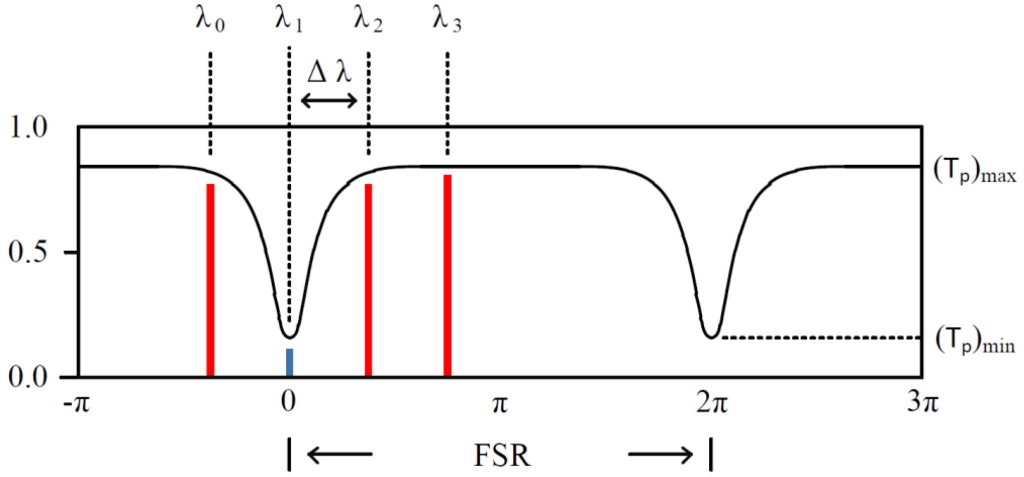
- The optical crosstalk noise coefficient is the summation of unwanted signals whose wavelength is not λ_1
  - m_o number of wavelengths in optical interconnect
  - $\Delta\lambda$ wavelength spacing

$$\varepsilon_o = 2 \sum_{i=1}^{\lfloor m_o/2 \rfloor} T_d^N(\lambda_1 + i\Delta\lambda)$$

Optical Interconnect Attenuation

- Before λ_0 reaches the filter, it will pass by other micro-resonators with working wavelength
  - λ_1 , λ_2 .... λ_n
- The attenuation of optical path is the product of:
  - Coupler efficiency
  - Propagation attenuation
  - Passing-by loss of MR
  - Insertion loss of MR





Optical Interconnect Attenuation

- In microresonator with working frequency λ_1, the through port transfer function is

$$T_p(\lambda) = \frac{r^2a^2 - 2r^2acos\theta + r^2}{1 - 2r^2a\cos\theta(\lambda) + r^4a^2}$$

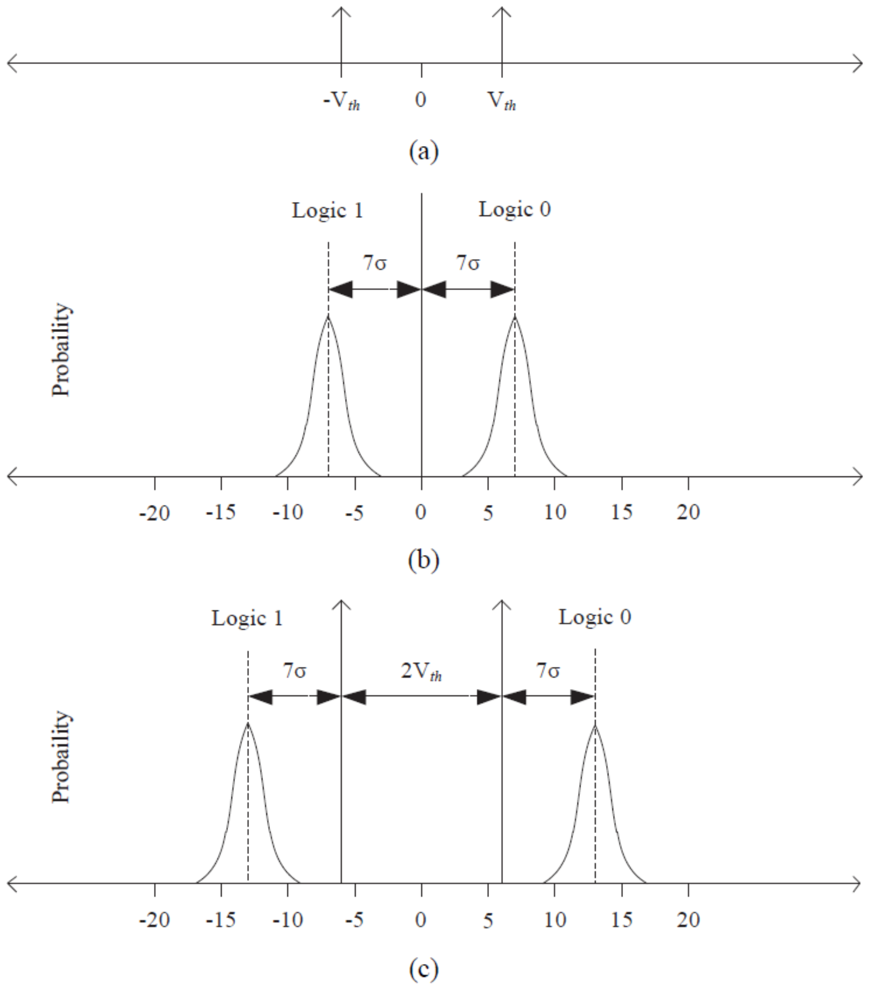
- The attenuation of optical path is the product of four terms
  - η_o coupling efficiency of optical pin
  - a_o attenuation of waveguide

$$A_o = \underbrace{\eta_o^2}_{\text{Coupler loss}}\underbrace{e^{-\alpha_o L}}_{\text{Propagation loss}}\underbrace{L_p(m_o - 1)}_{\text{Passing loss}}\underbrace{T_d^2(\lambda_n)}_{\text{Insertion loss}}$$

Optical Interconnect Sensitivity

- In optical interconnect, the sensitivity OMA is the difference between two optical power levels P_1 and P_0
  - *BER* bit error rate
  - *SNR* signal to noise ratio
  - i_n input referred RMS noise density
  - Z_{tia} transimpedance of TIA
  - ρ responsivity of photodetector

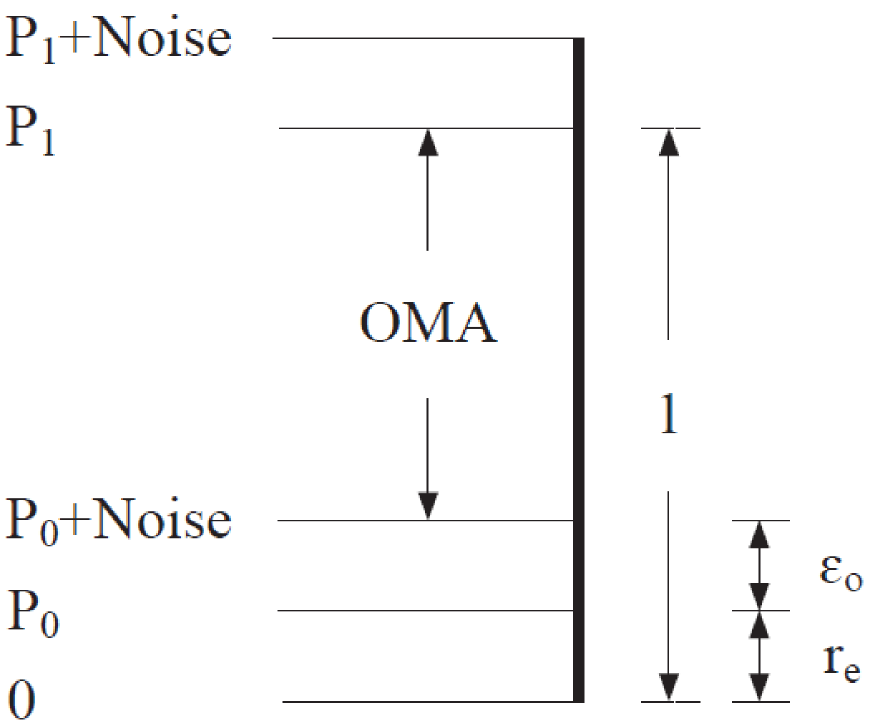
$$\text{OMA} = \frac{i_n f^{0.5} \cdot \text{SNR} + 2V_{th} Z_{tia}^{-1}}{\rho}$$



Optical Interconnect Sensitivity

- Only when this voltage difference is grater than OMA, signals can be detected by the limiting amplifier
  - ε_o crosstalk noise coefficient
  - r_e extinction ratio P_1/P_0
  - η_s slope efficiency of laser
  - I_{th} threshold current of laser

$$I_{mod} + I_{bias} = \frac{\text{OMA}}{A_o(1 - \varepsilon_o - r_e)\eta_s} + I_{th}$$



Ratio= $1 - \varepsilon_o - r_e > 0$

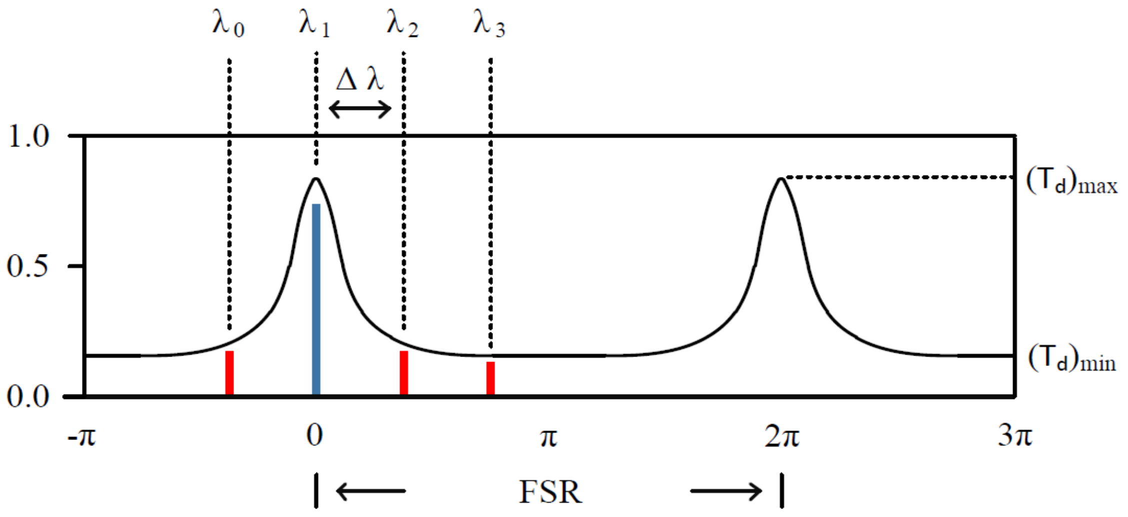
Optical Interconnect Bandwidth

- FSR is the spacing between two successive resonance peaks in spectrum
  - n_e MR effective refractive index
  - R MR radius of ring

$$\text{FSR} = \frac{\lambda^2}{2\pi n_e R}$$

- $\Delta\lambda$ is the wavelength spacing between two neighboring wavelengths

$$\text{B}_o = 2\lfloor\frac{\text{FSR}}{\Delta\lambda}\rfloor f$$



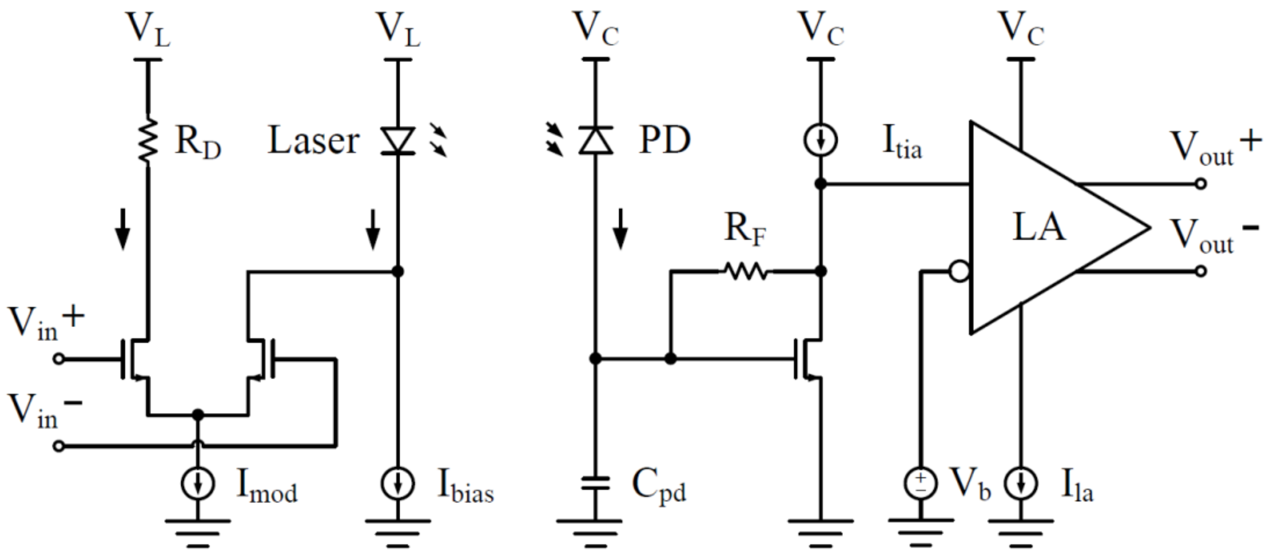
Optical Interconnect Power Consumption

- In optical interconnect, power consumption includes the power of laser sources, receiver, SerDes and modulator
  - V_l laser supply voltage
  - I_{tia} TIA supply current
  - Direct modulation

$$P_o = P_{sd} + (I_{mod} + I_{bias})V_l + (I_{tia} + I_{la})V_c$$

  - Indirect modulation

$$P_o = P_{sd} + (I_{mod} + I_{bias})V_l + (I_{tia} + I_{la})V_c + P_m + P_d$$



Optical Interconnect Power Consumption and Area

- The power consumptions of the electrical funneling interface and optical weaving interface

$$P_{feo} = 5log_2 R P_e + P_c + \frac{1}{4} P_d + \frac{1}{2} P_m + P_t + \frac{P_o}{L_i}$$

$$P_{weo} = P_e + P_c + \frac{1}{2} P_d + R P_m + R P_t + \frac{P_o}{L_i^R}$$

- The areas of the electrical funneling interface and optical weaving interface

$$S_{feo} = 5log_2 R S_e + S_c + S_m + S_l$$

$$S_{weo} = \frac{M}{2N} S_e + S_c + \frac{M}{N} S_m + S_l$$

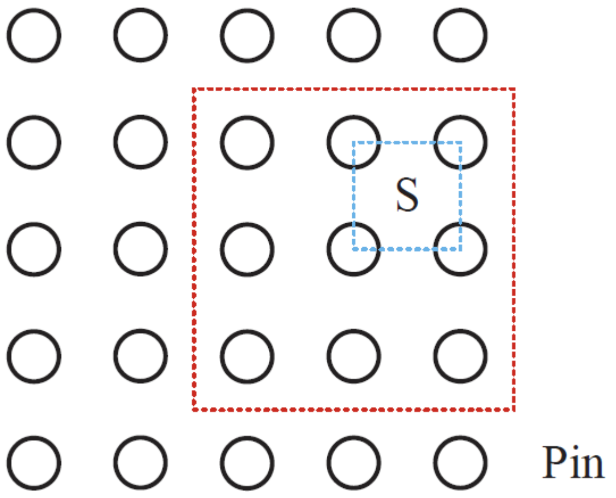
Area and Linear Bandwidth Density

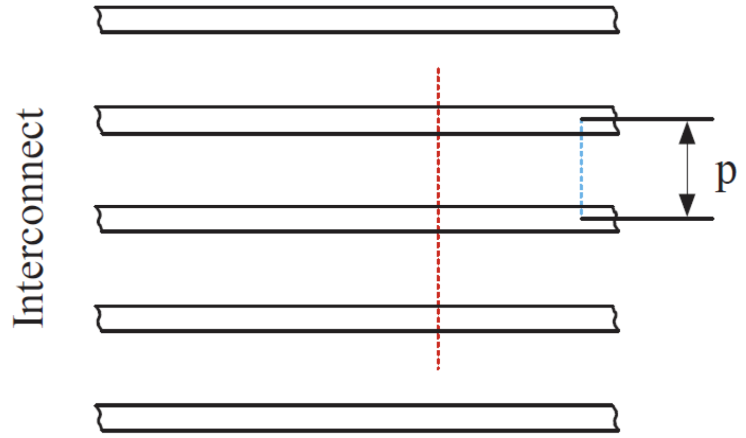
- Area bandwidth density
  - Bandwidth in a unit area
  - Important to package pin, socket *etc.*

$$\text{Area Density} = \frac{\text{Bandwidth } B}{\text{Area } S}$$

- Linear bandwidth density
  - Bandwidth in a unit width
  - Important to PCB, substrate, interposer *etc.*

$$\text{Linear Density} = \frac{\text{Bandwidth } B}{\text{Pitch } p}$$





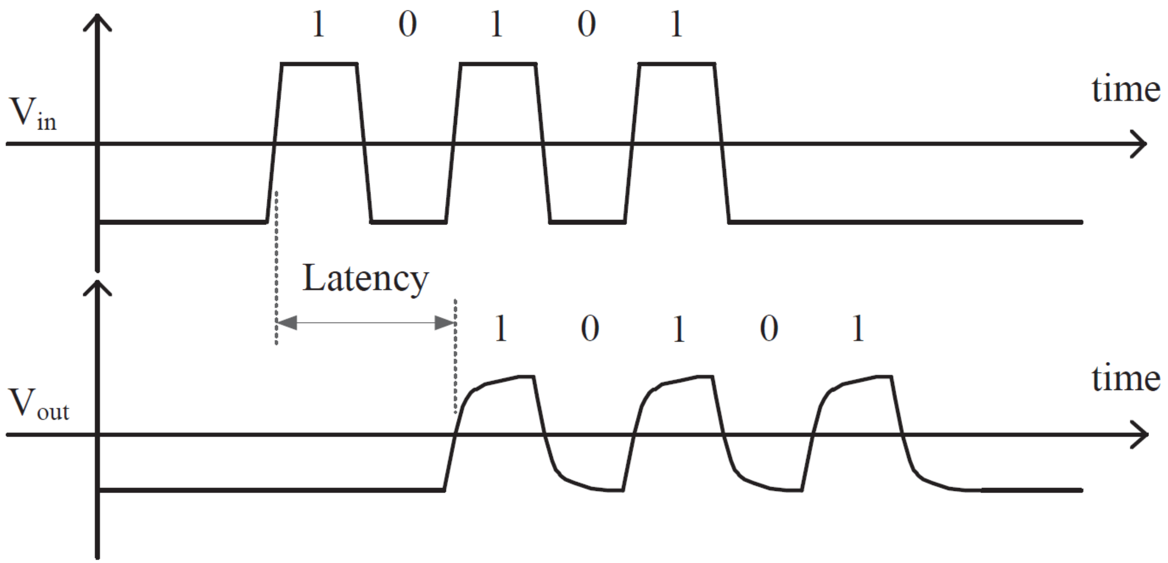
Electrical and Optical Interconnect Latency

- Propagation delay is proportional to the interconnect length, and inverse proportional to the propagation speed
  - V_e speed in electrical interconnect
  - ϵ_r relative dielectric constant

$$v_e = \frac{c}{\sqrt{\epsilon_r}}$$

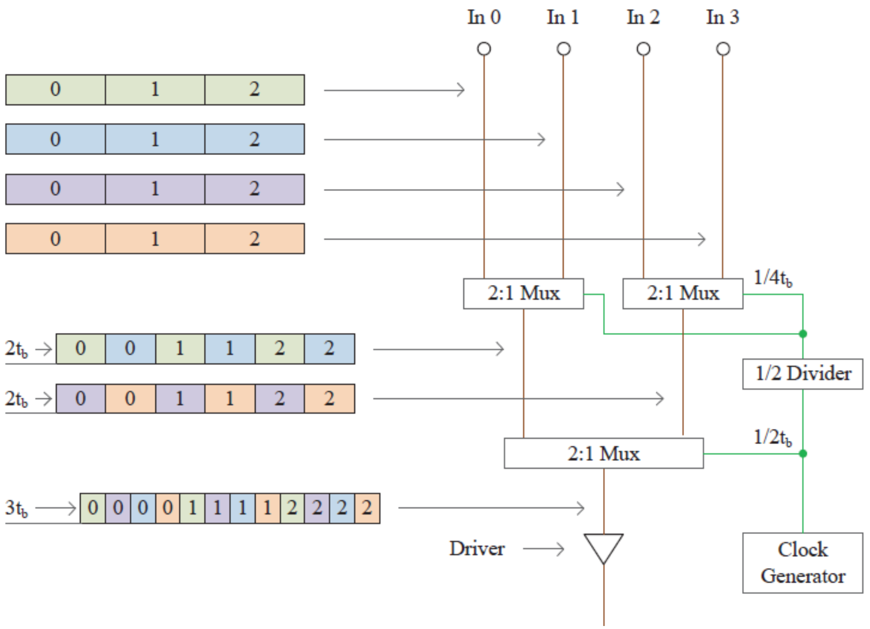
  - V_c speed in optical interconnect
  - n_g group reflection index

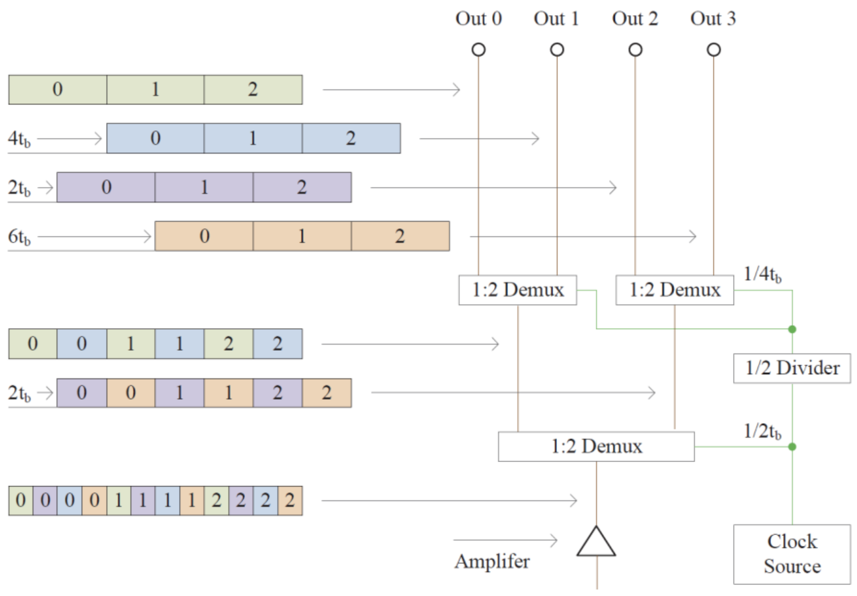
$$v_o = \frac{c}{n_g}$$



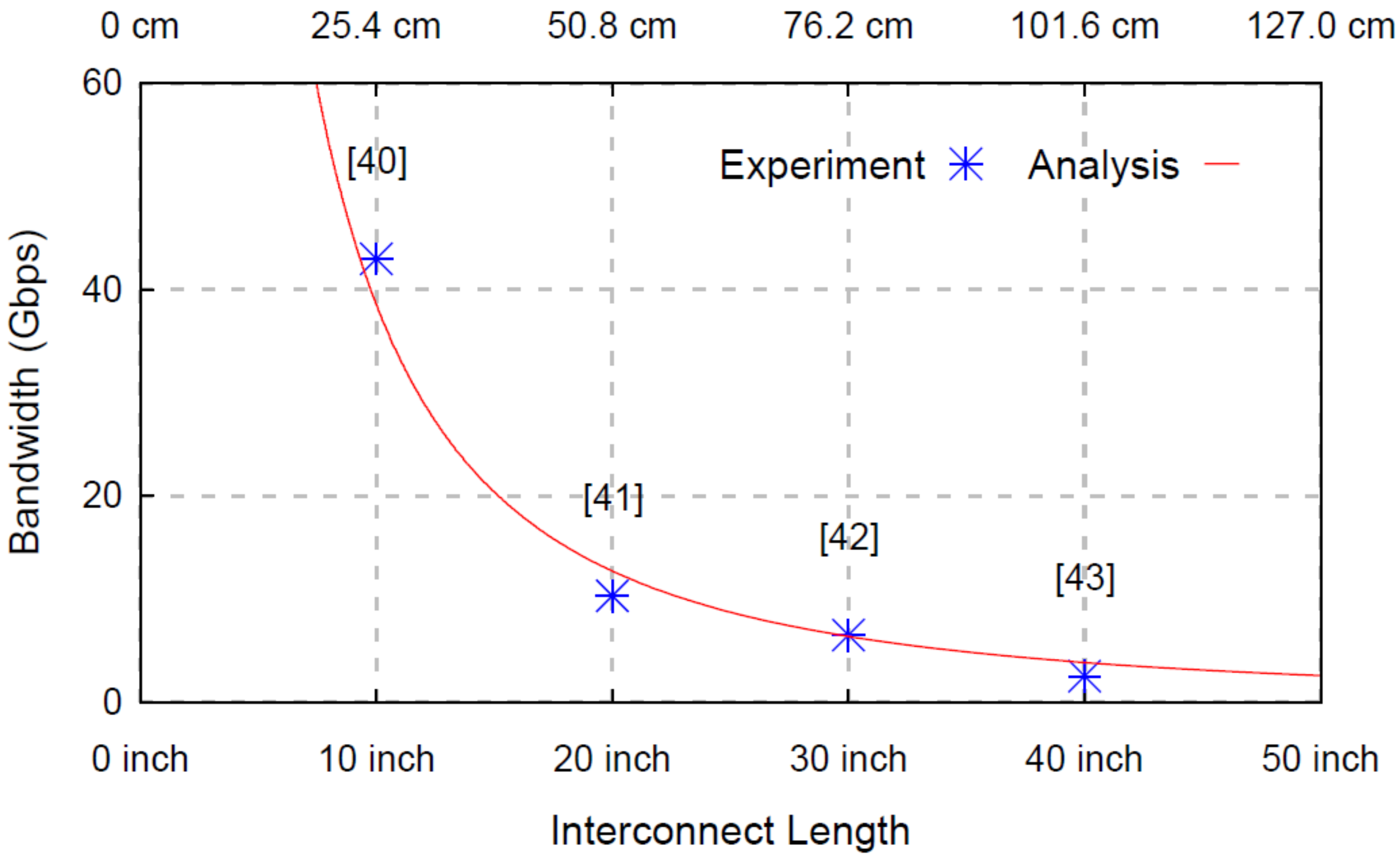
Serializer and Deserializer

- SerDes consist of multiple stages of multiplexers or demultiplexers
  - With a large number of latches
- A bottleneck in inter-chip interconnect
  - Large power consumption, large area, additional latency





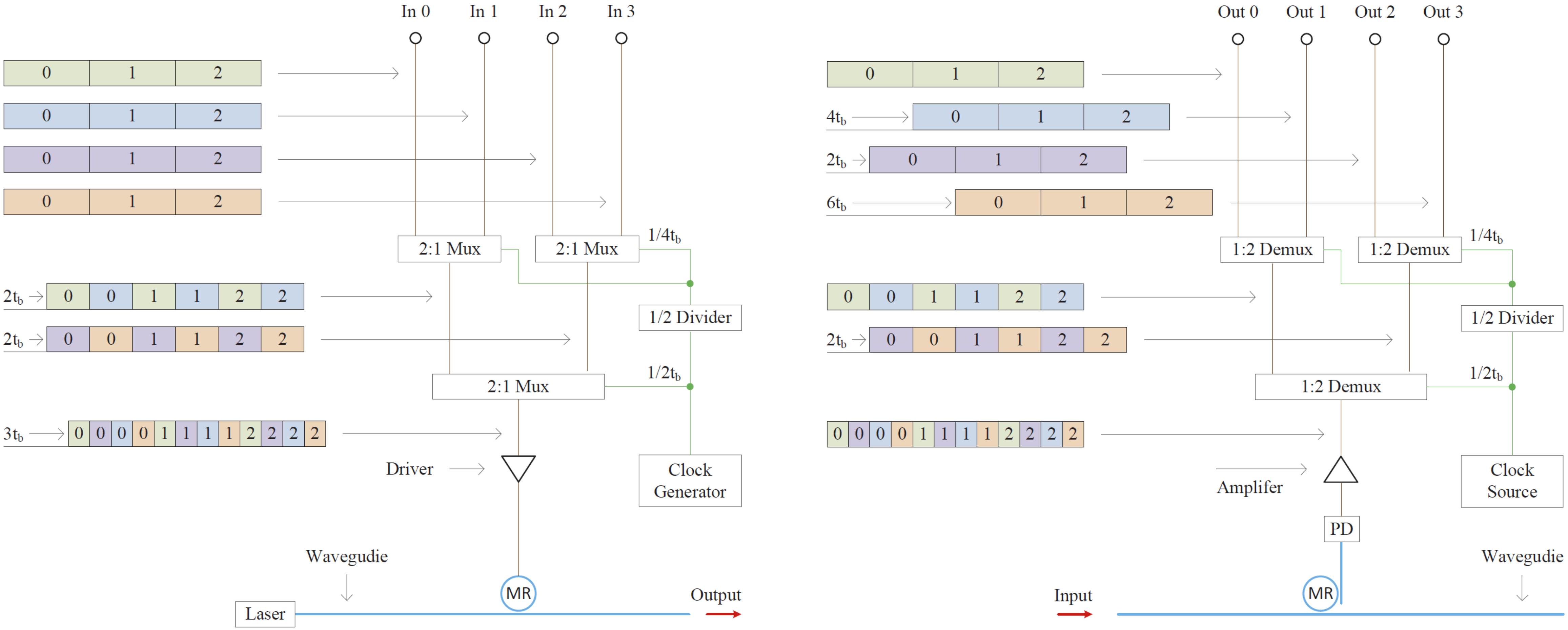
Electrical Interconnect Verification



- Our analytical models match experiment results well

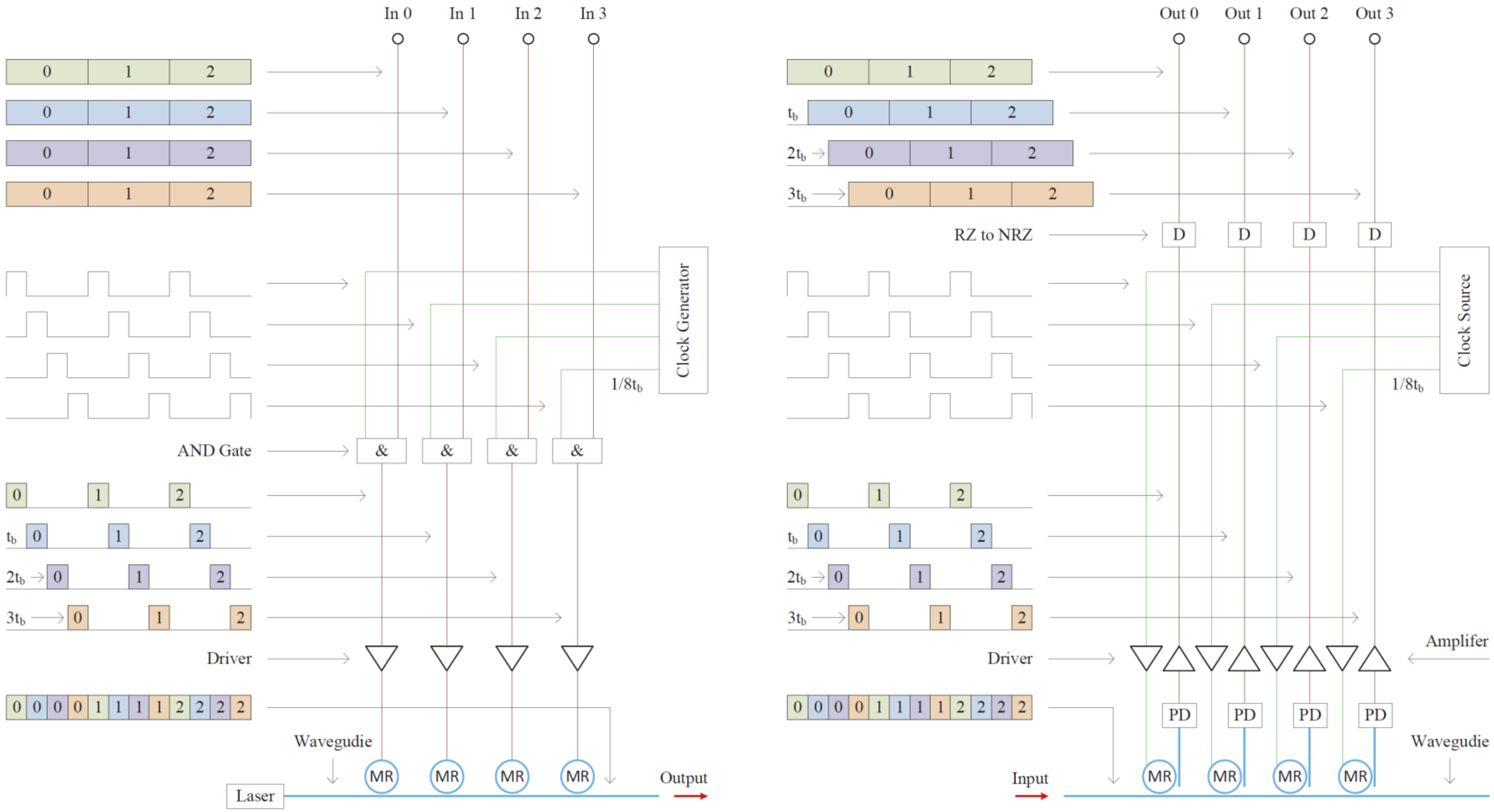
Traditional OE Interface: Electrical Funneling

- Electrical SerDes plus O-E conversion



New OE Interface: Optical Weaving

- Optical-electrical SerDes



Outline

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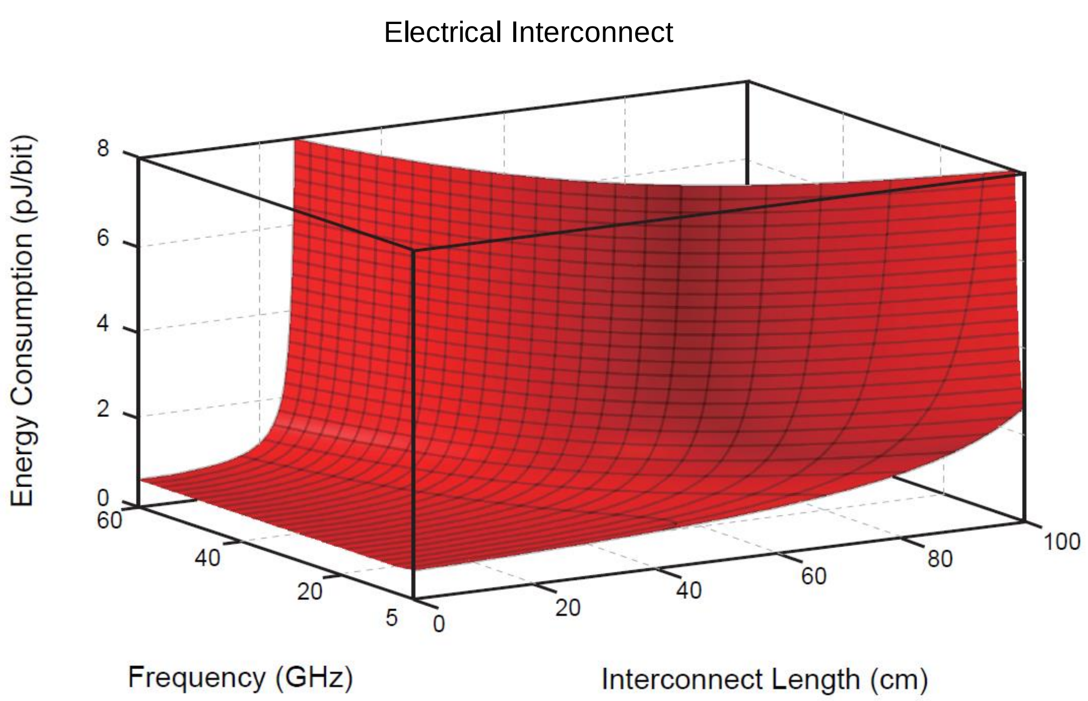
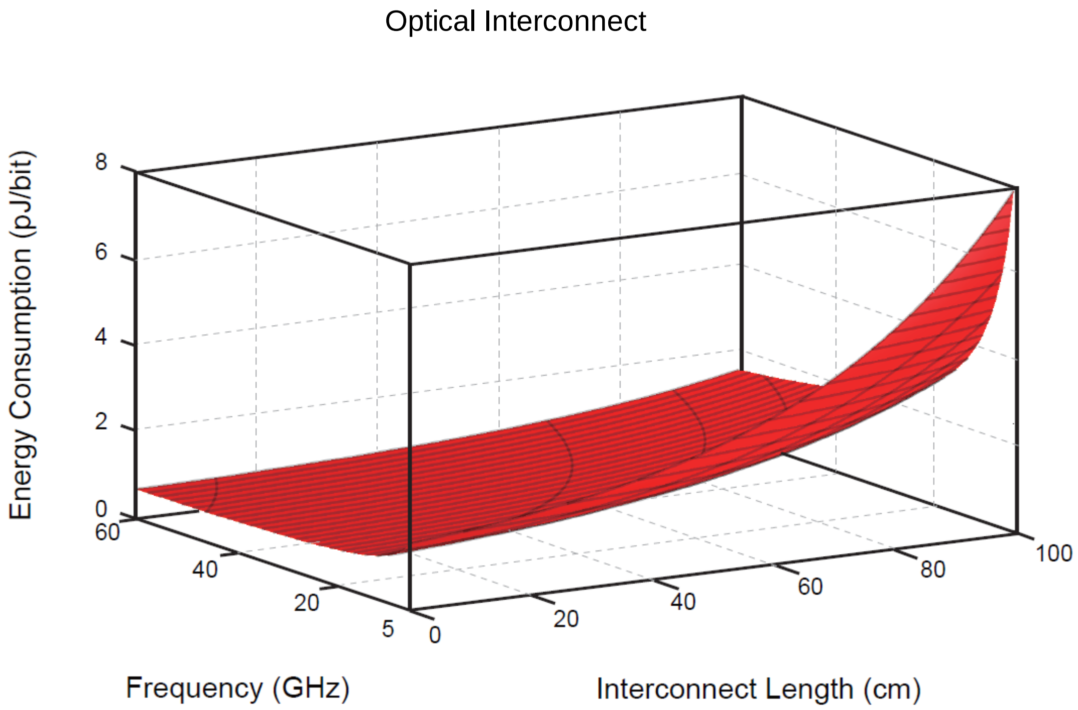
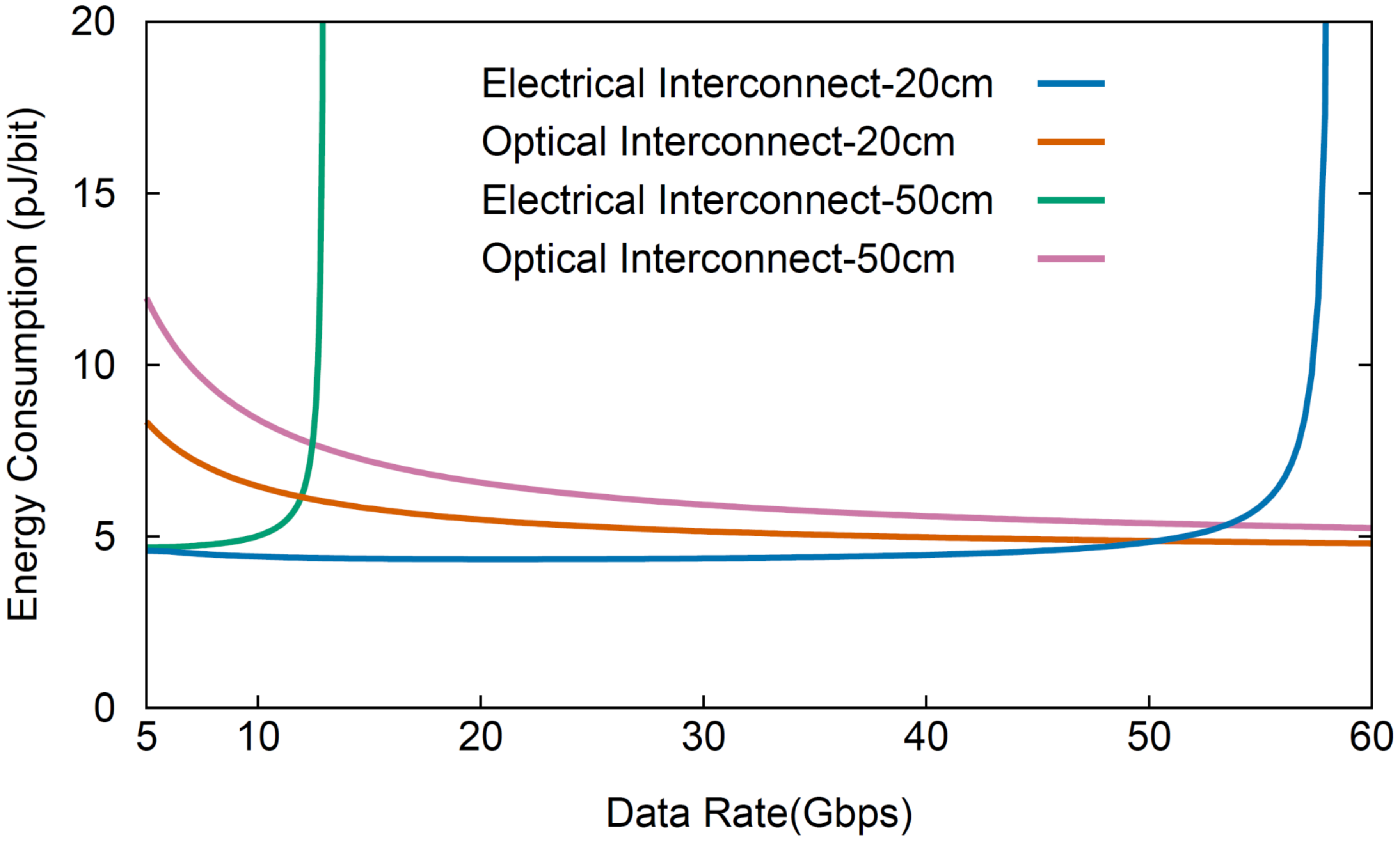
Optical vs. Electrical Interconnect: Energy Efficiency





- Electrical interconnect has an energy cliff
- Optical interconnect favorite high data rate

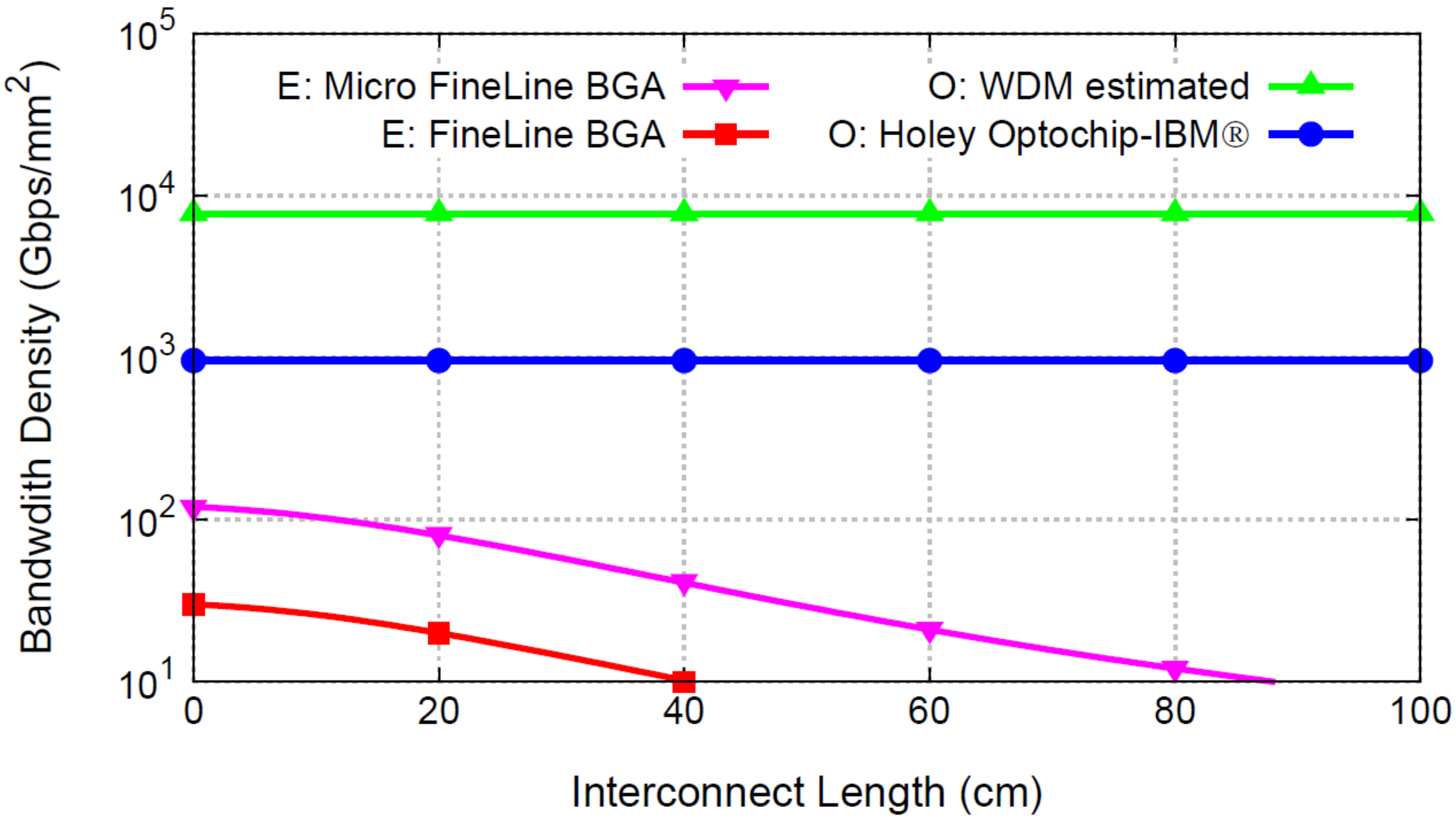
Optical vs. Electrical Interconnect: Energy Efficiency



- 8:1 SerDes
- Electrical funneling

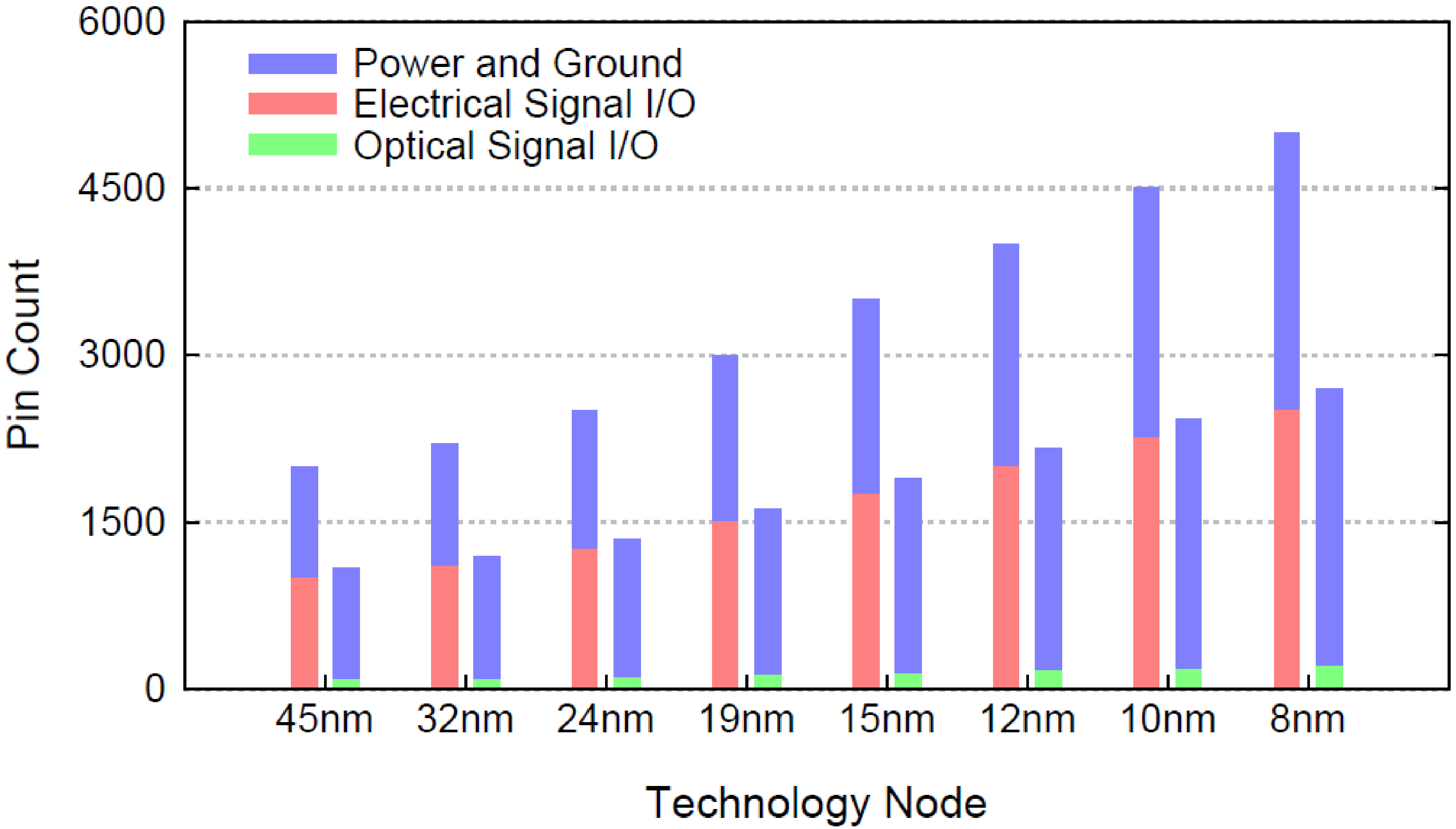
Optical vs. Electrical Interconnect: Area Bandwidth Density

- Two orders of magnitude higher than micro-FBGA package
- Three orders of magnitude higher than FBGA package

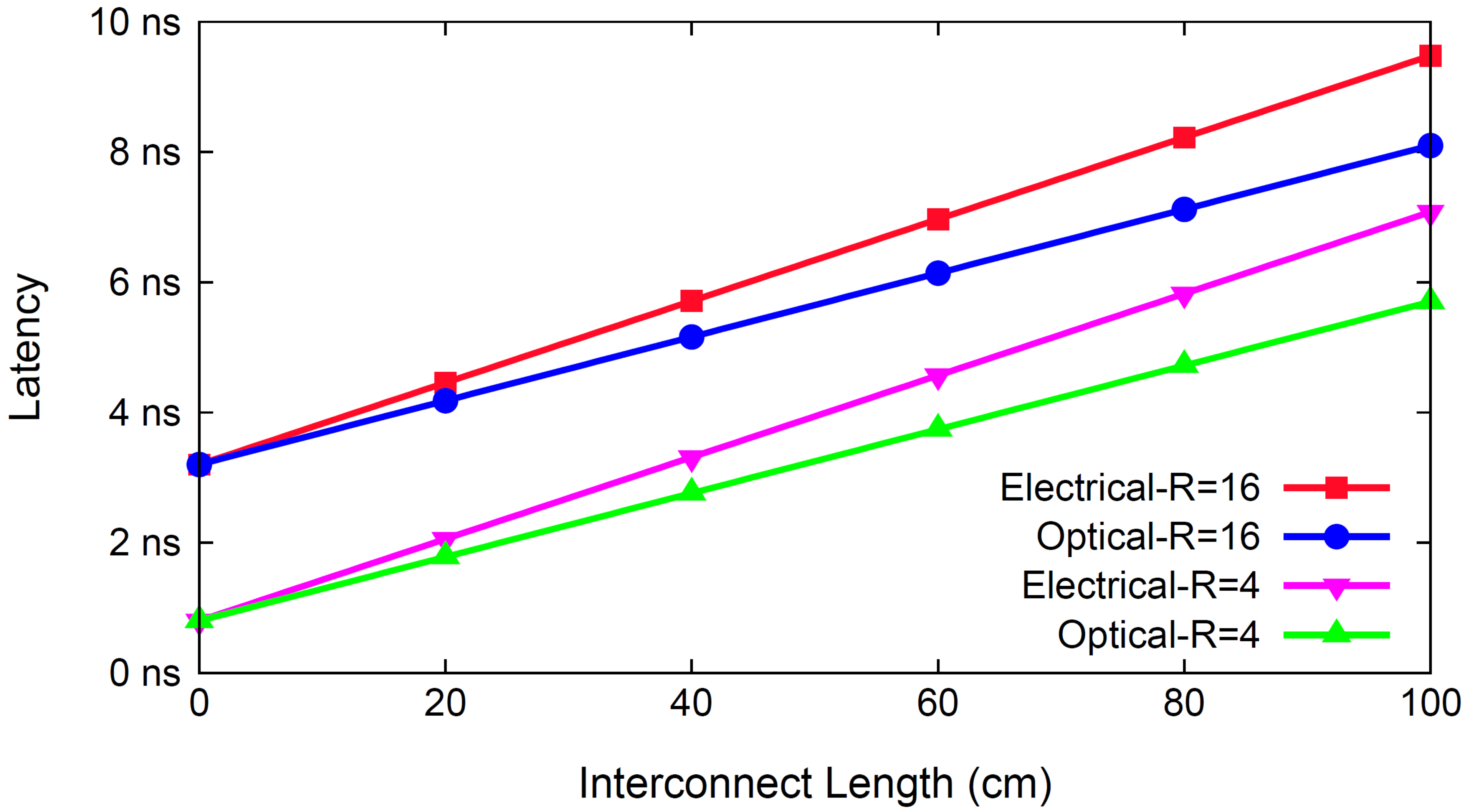


Optical vs. Electrical Interconnect: Pin Count

- Reduce >92% signal pins with 25cm interconnects
- Reduce >97% signal pins with 50cm interconnects

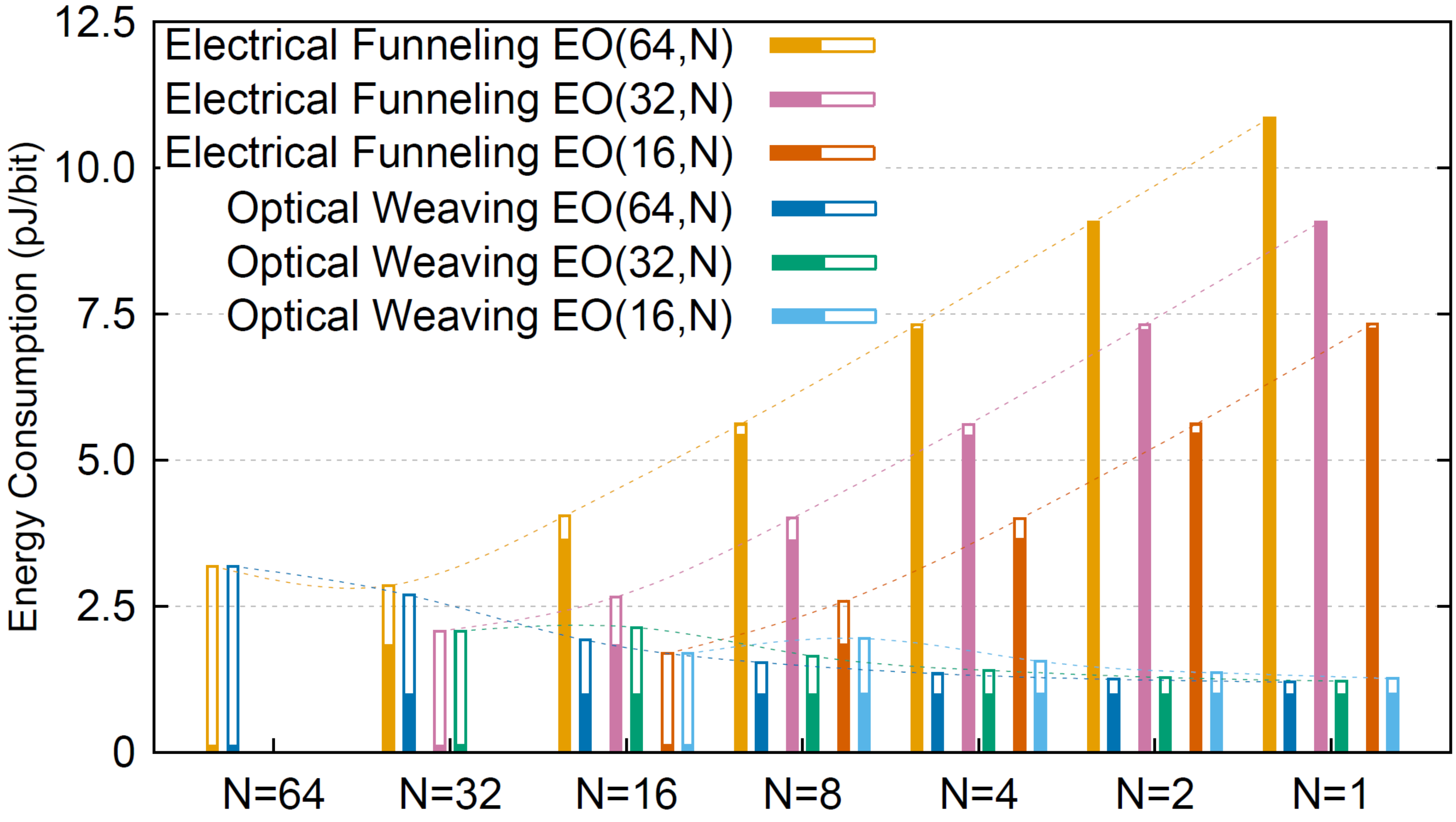


Optical vs. Electrical Interconnect: Latency



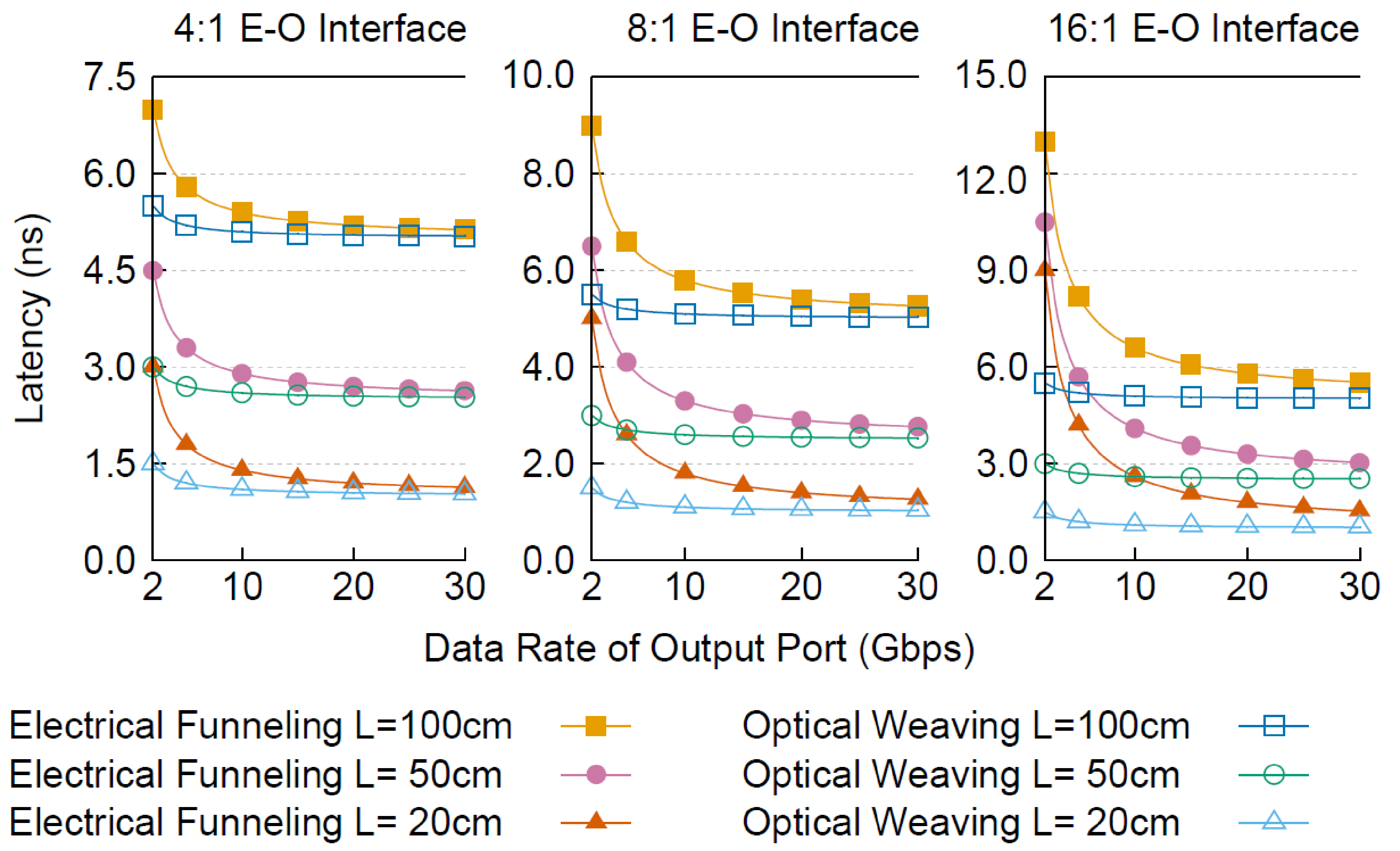
- 5Gbps
- Corning SMF-28 optical fiber
- Rogers RO4003
- Electrical funneling

Optical Weaving vs. Electrical Funneling: Energy Efficiency



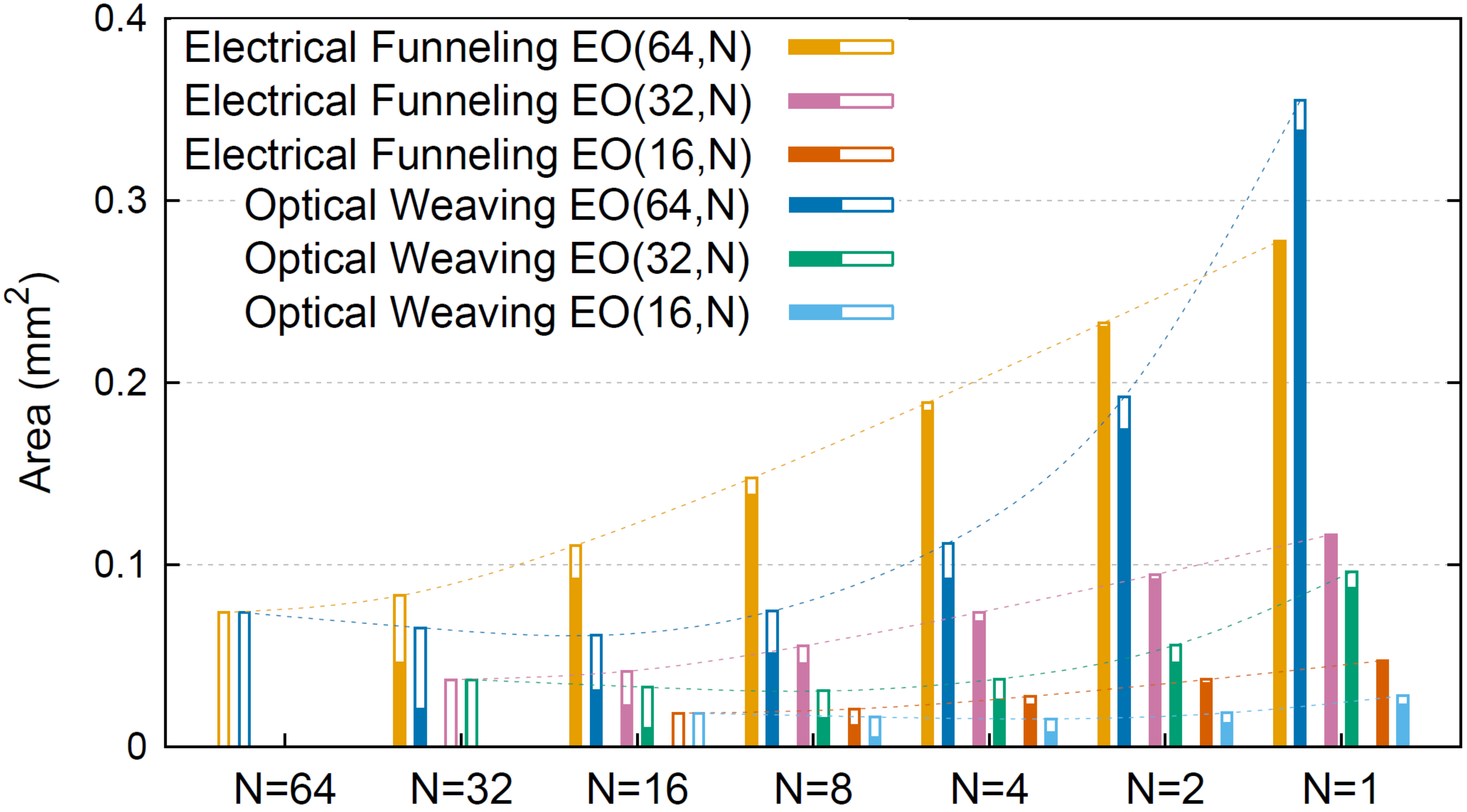
- 50cm long
- 2Gbp per input
- I_0=0.2mA/Gbps

Optical Weaving vs. Electrical Funneling: Latency



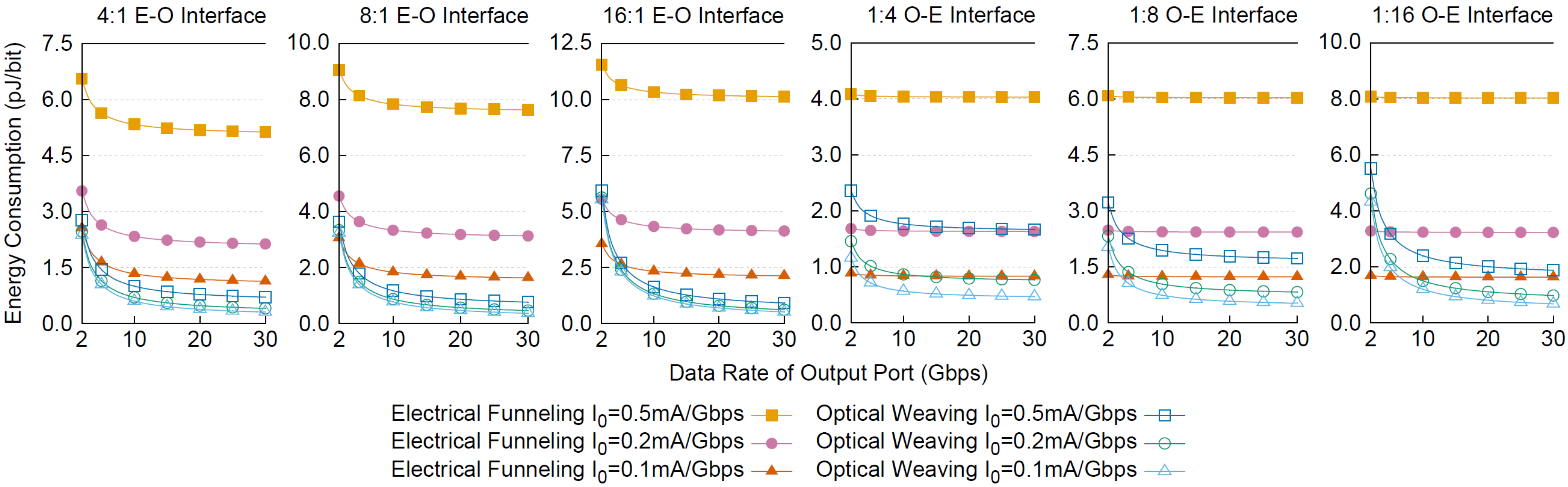
- I_0=0.2mA/Gbps

Optical Weaving vs. Electrical Funneling: Area



- 50cm long
- 2Gbp per input
- 22nm node

Optical Weaving vs. Electrical Funneling: Technology Dependency

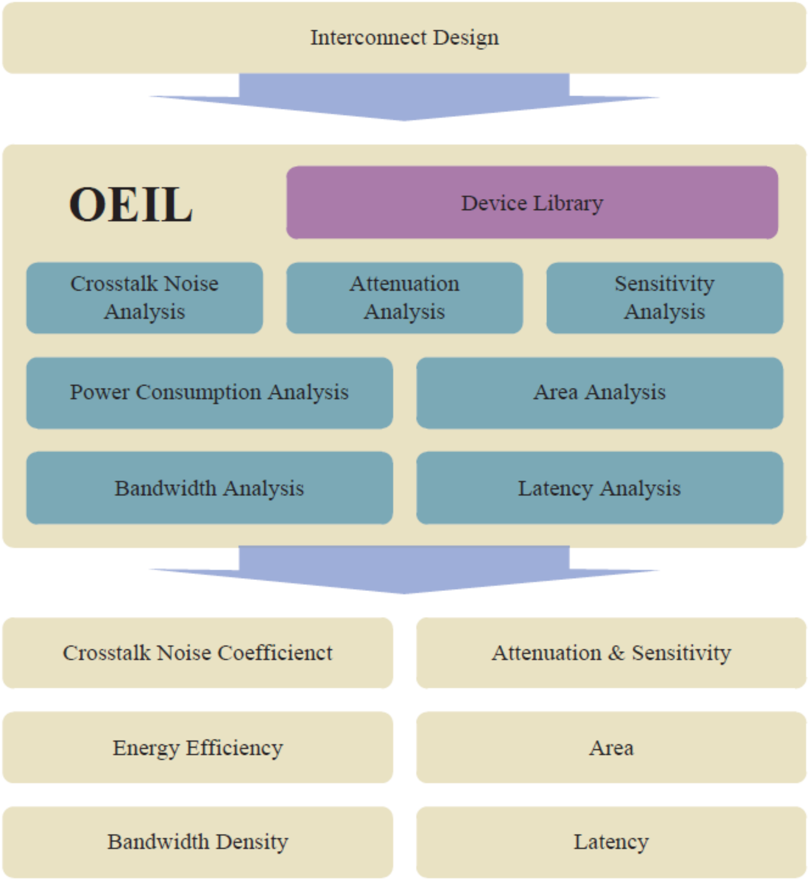


- Differences in circuit design details, technology nodes, and foundry processes are reflected by unit current I_0

OEIL: Optical and Electrical Interfaces and Links

- A comprehensive device library for off-chip interconnects
- Publicly released and available at

  www.ece.ust.hk/~eexu/OEIL.html



The flow chart of OEIL simulator

Conclusions

- Analytical models for optical and electrical interconnects and interfaces
- Holistic comparisons in terms of bandwidth, bandwidth density, latency, energy efficiency, signal integrity, and area
- Proposed a new O-E interface, optical weaving
- Publicly released a R&D tool, OEIL

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