Foton
CNRS UMR 6082

Fonctions Optiques pour les
Technologies de l'informatiON

Laser Integration challenges

For on-chip optical interconnects

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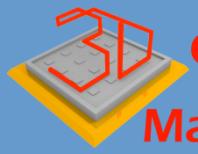
ComInLabs



Optical
Many Cores

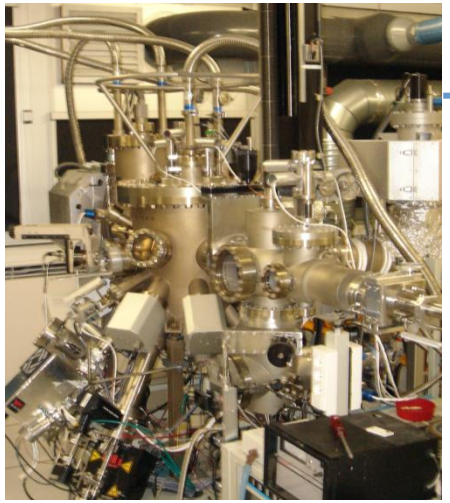
Who are we?

ENSSAT
LANNION

Optical communications & sensors

INSA INSTITUT NATIONAL DES SCIENCES APPLIQUÉES RENNES

Materials for photonics



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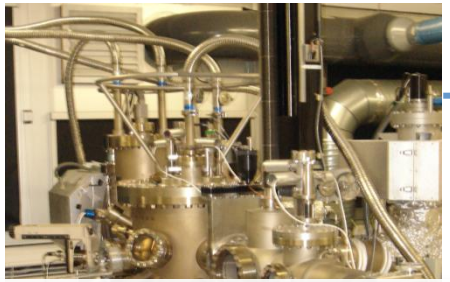
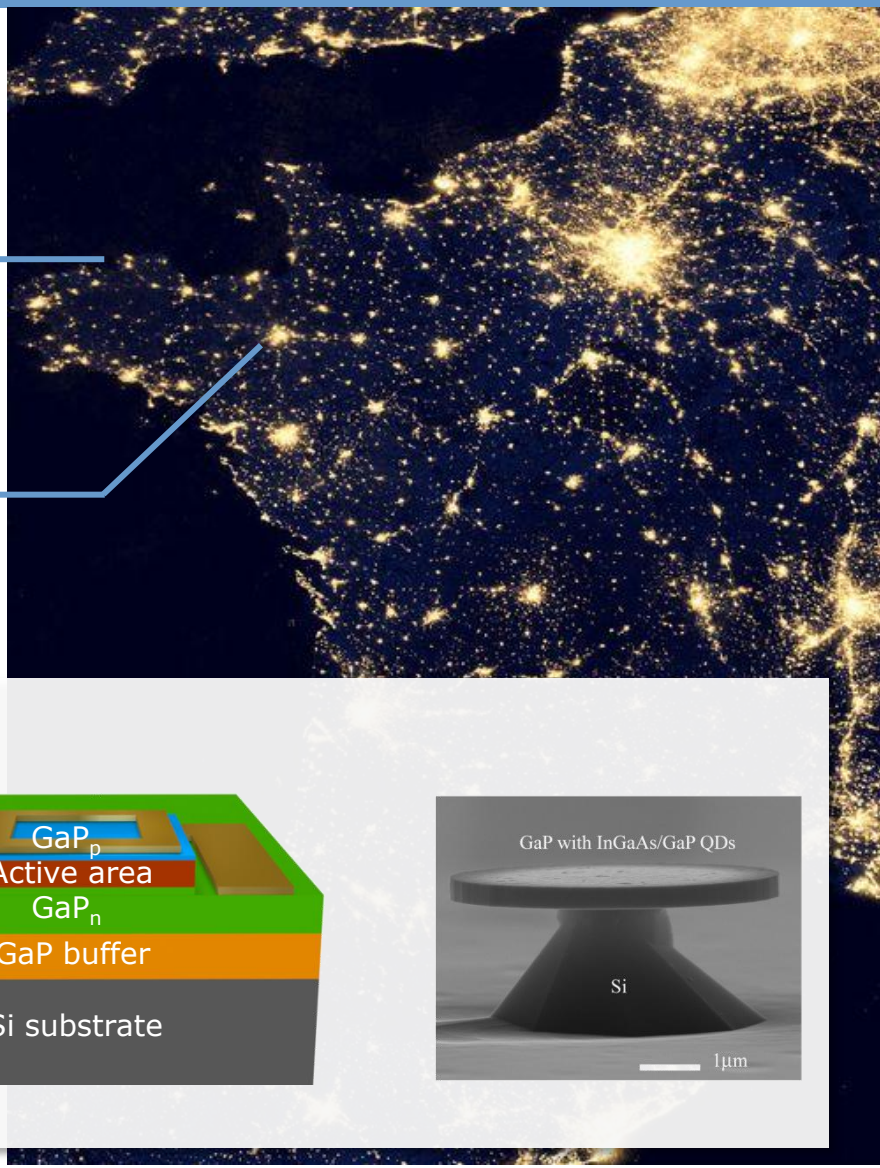
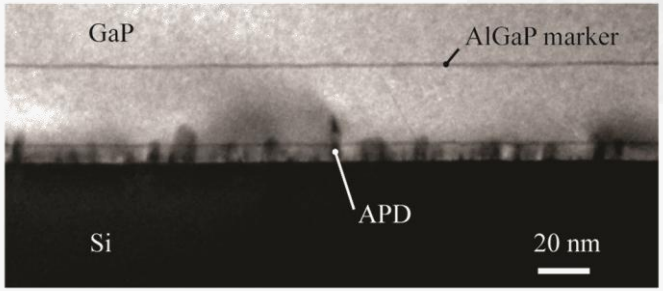




Monolithic silicon photonics



Integrating lasers in microprocessors

Where? The best place of the photonic layer in a microprocessor

How? The best integration approach of active photonic devices

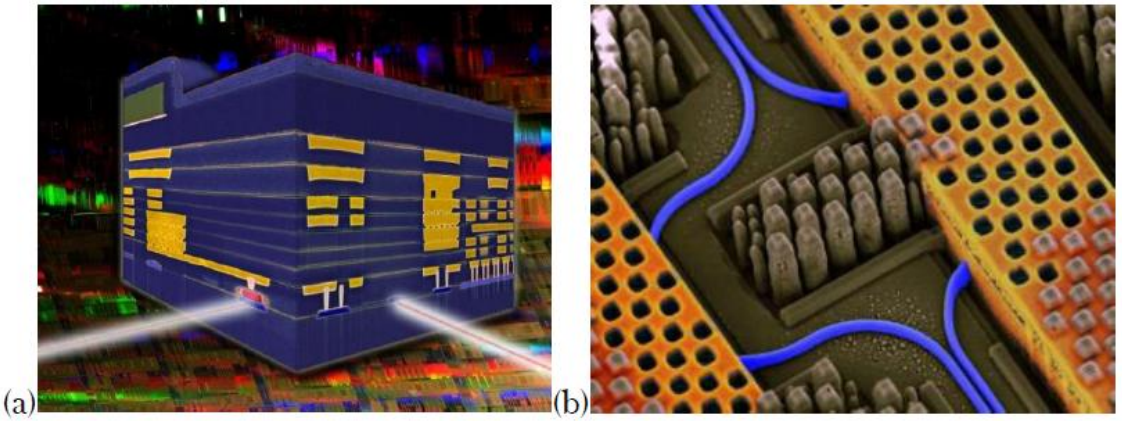
What? The best laser design for a given MP architecture

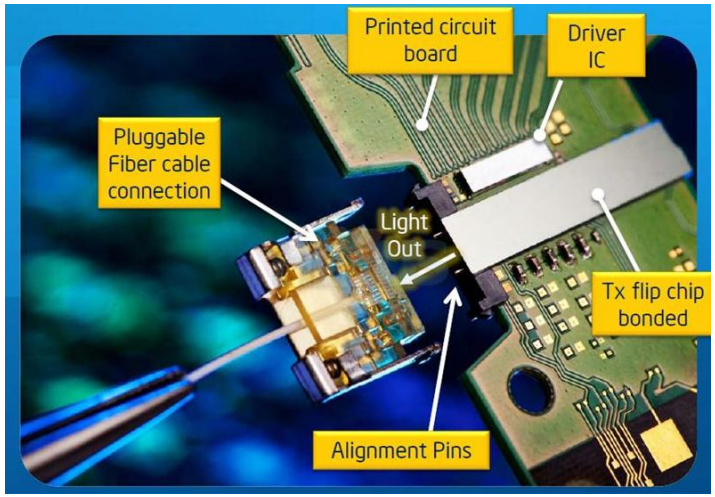
Very different approaches by the electronics giants

IBM:

Co-integration of CMOS and photonics

Combined front-end integration



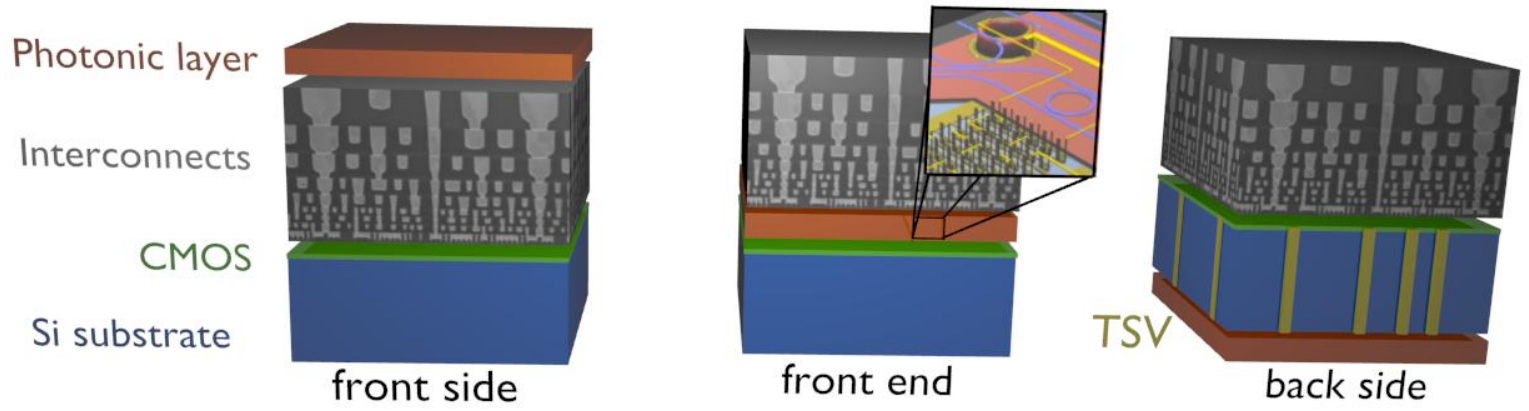


Intel:

Front side bonding of III-V lasers on Si

Where?

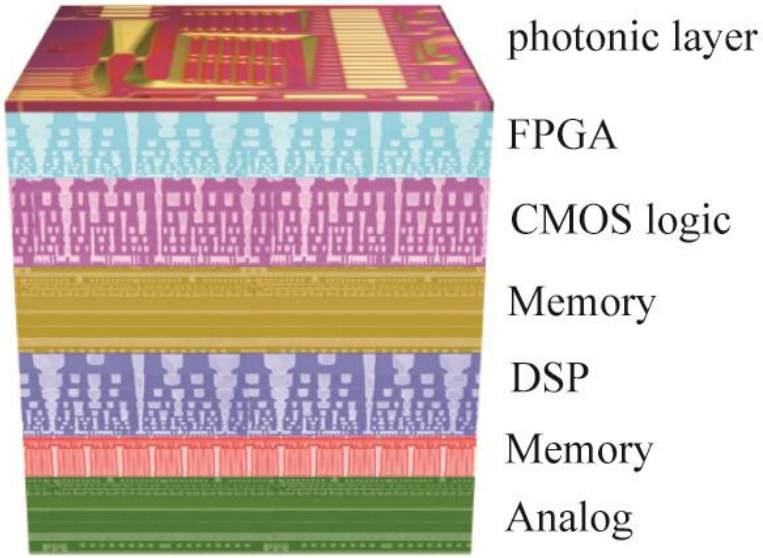
At the fab line level:



	front side	front end	back side
Thermal management	✗	✓	✓
Fast communication	✗	✓	✗
Process ease	✓	✗	✓
Off-chip communication	✓	✗	✓
Test costs	✗	✓	✗

Where?

In 3D architectures:

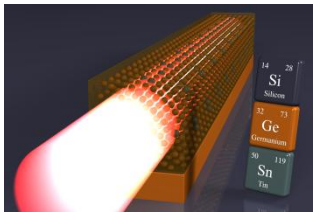


Inspired from N. Solomon patent US8136071 B2

- New issues for thermal management
- Is the previous classification still relevant?
  - Always production-line-related considerations
  - Consequences at different abstraction levels of the architecture design

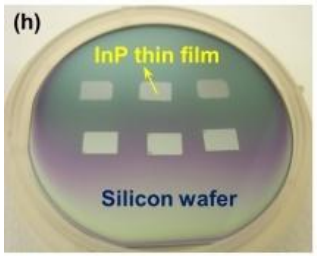
- Huge issues related to the integration method…

How?



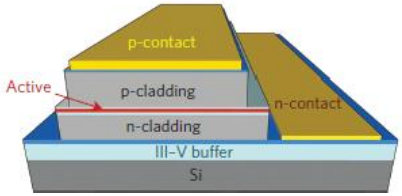
Nat. Phot. '15

- Group IV photonics (Si, Ge, GeSn)
  - CMOS compatibility
  - Laser electric drive
  - In some cases the wavelength



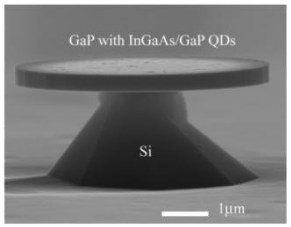
Gent Univ.

- Heterogeneous integration of III-V
  - Process and architecture
  - Best(?)yields
  - Flexibility
  - III-V wafer issue
  - (large scale integration, costs)



Nat. Phot. '16

- Metamorphic integration of III-V
  - Large scale integration
  - Good yields
  - Thermal management
  - Pseudo-substrate issue



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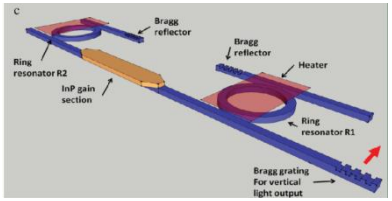
- Pseudomorphic integration of III-V
  - Large scale integration
  - Best choice for combined front-end
  - Thermal management
  - Optical property immaturity

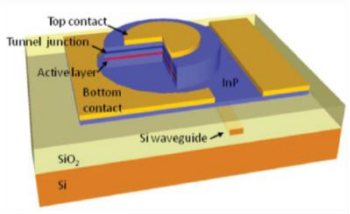
Four kinds of laser designs:

Ridge lasers



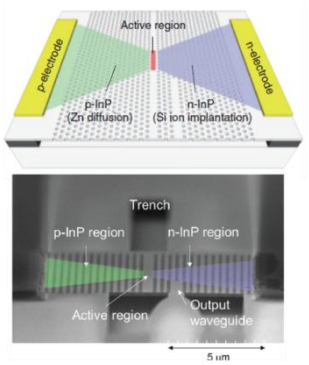
III-V lab

Microdisks/rings



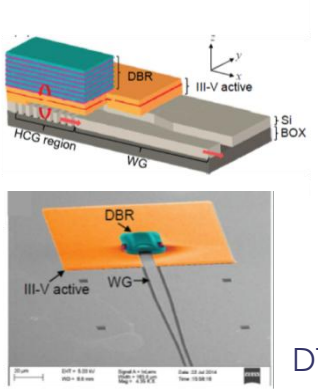
Gent - CEA

Ph. C. cavities



NTT

VCSELs



DTU

Different demands in PICs:

Corona archi.

-External optical drive

- high power laser (0.8W)
- WDM source
- no footprint issue

Chameleon archi.

-thousands of on-chip micro-lasers

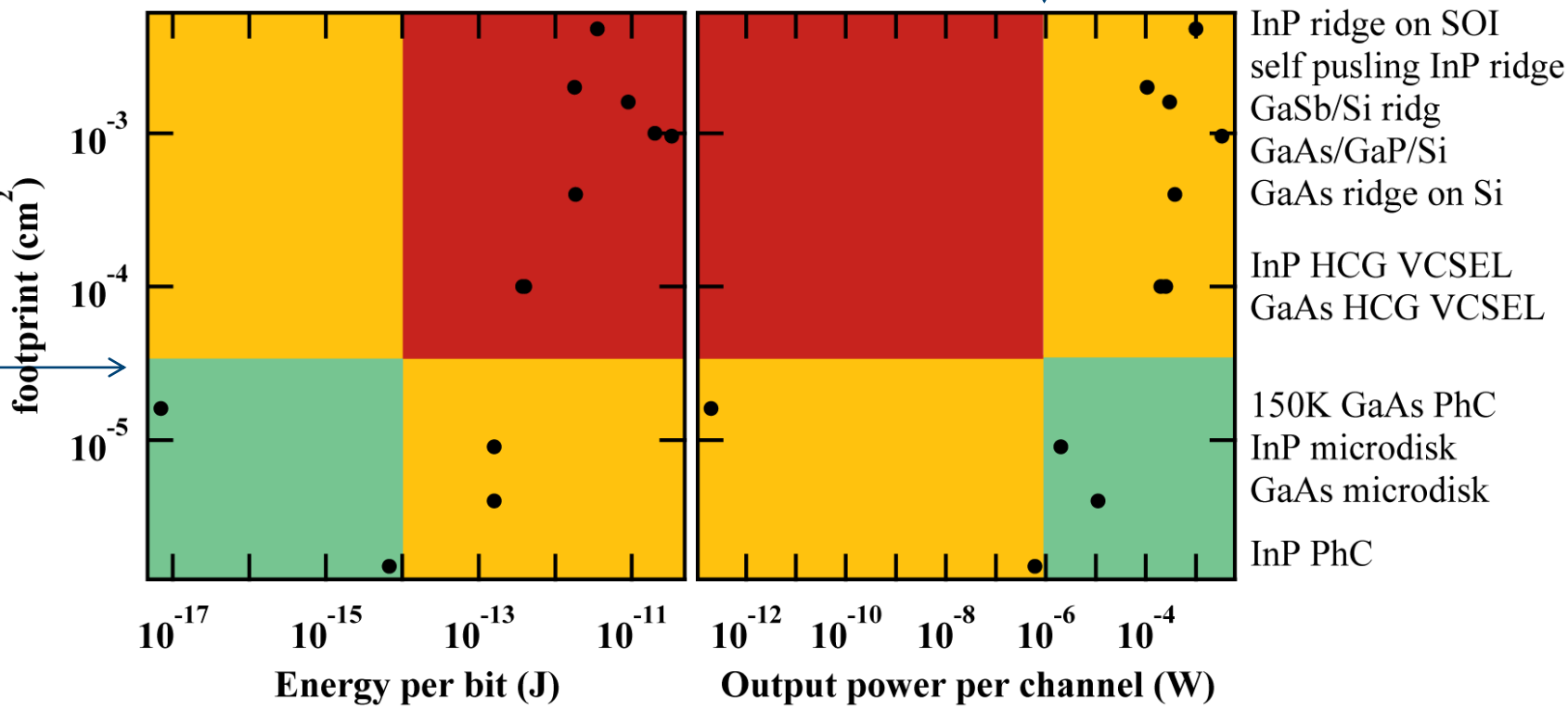
-Low power source

- tunability?
- huge footprint constraint

What?

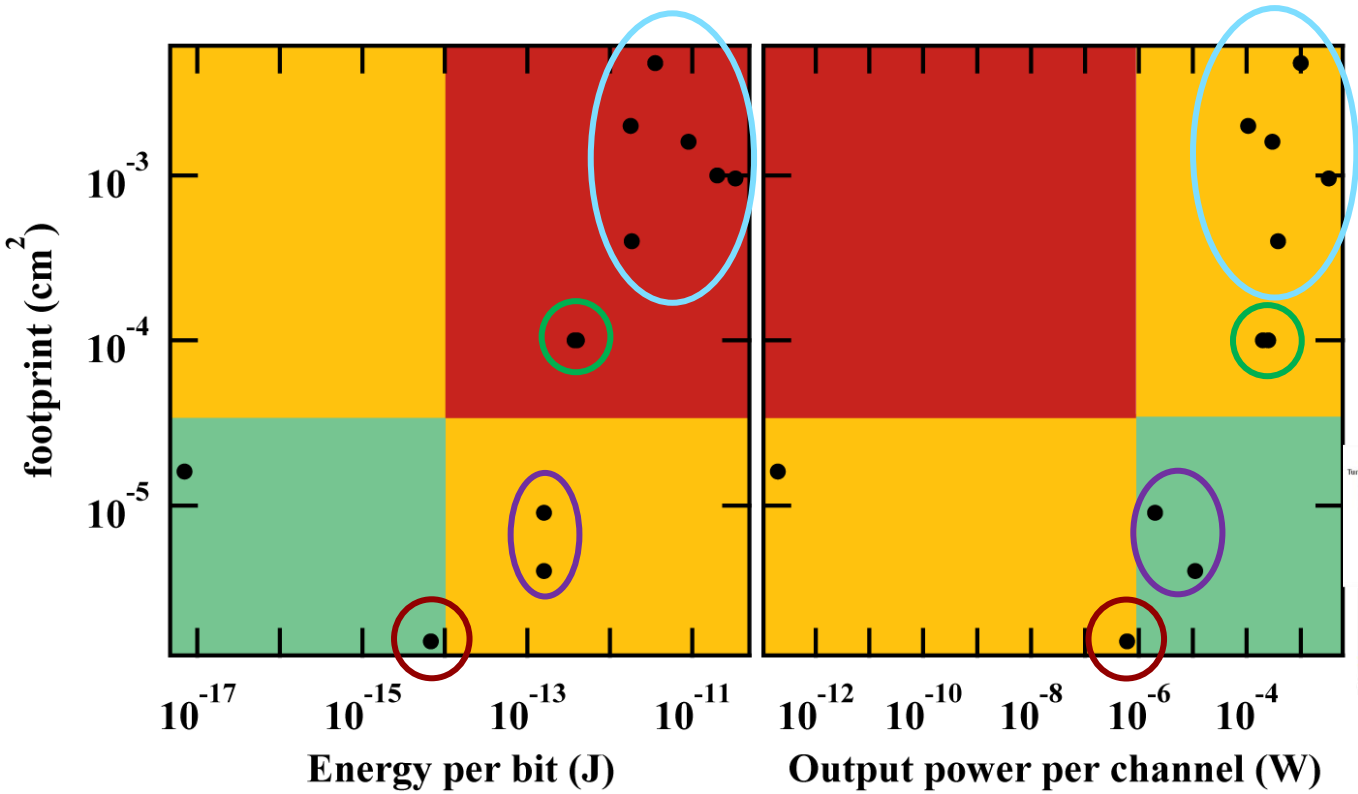
D.Miller, *Proc. IEEE*, **97**, 1166 (2009)

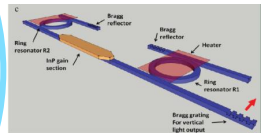
S. Le Beux *et al.*, ATD Europe (2014)



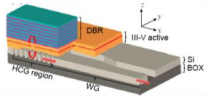
Calculated from Chameleon data.

What?

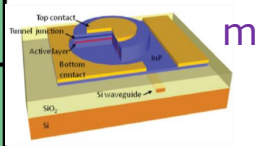




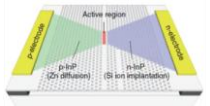
Ridges



VCSELs



microdisks



Ph. Cs

Any conclusion?

1) Integration issues at the chip scale
2) The ultimate monolithic integration might not be so unreachable
3) No laser solution so far : PhCs, microdisks or power sharing of ridges or VCSELs

All the issues, no solutions in …

Integrated lasers on Silicon

(C. Cornet, Y. Léger, C. Robert)

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