

Scalable Electro-optical Assembly Techniques for Silicon Photonics

Bert Jan Offrein, Tymon Barwicz, Paul Fortier



OIDA Workshop on Manufacturing Trends for Integrated Photonics

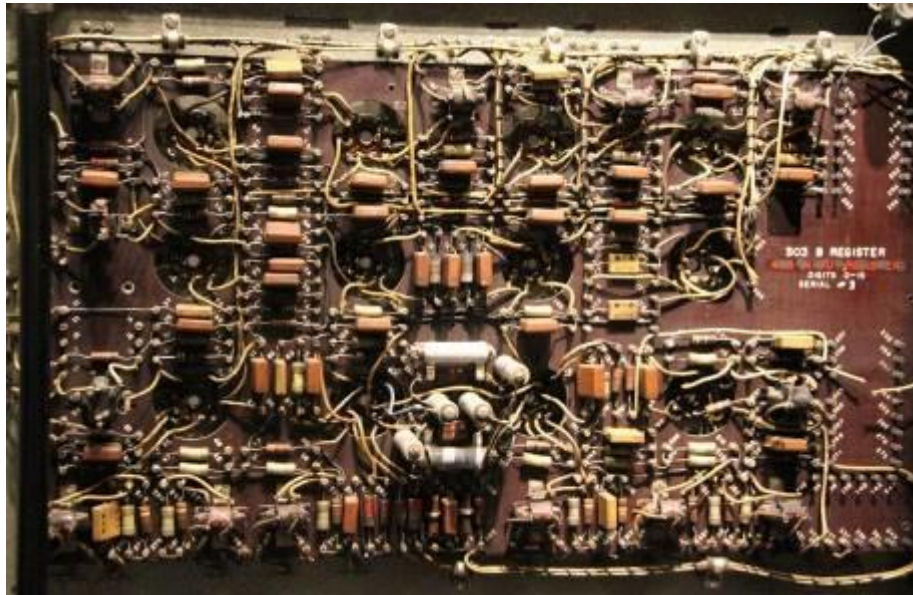
Outline

- Broadband large channel count electro-optical fiber-chip interfacing technique for silicon photonics
- Scalable and tolerant assembly techniques
- Summary

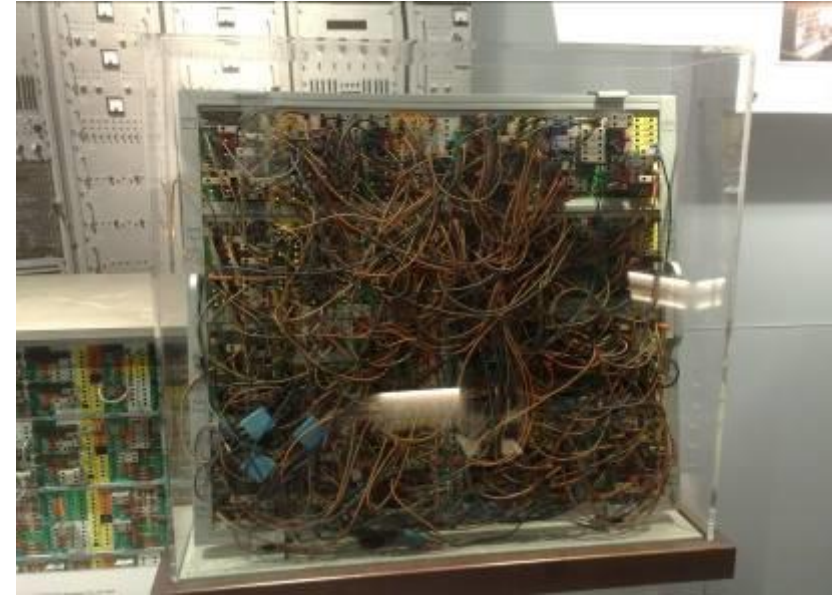
Why integration? Looking back, electronics



Pictures taken at:



Whirlwind, MIT, 1952



EAI 580 patch panel, Electronic Associates, 1968

Today's state of computing is based on:

- Integration and scaling of the logic functions (CMOS electronics)
- Integration and scaling of the interconnects (PCB technology & assembly)



For optical interconnects, this resembles:

- Electro-optical integration and scaling of transceiver technology
- **Integration of optical connectivity and signal distribution**

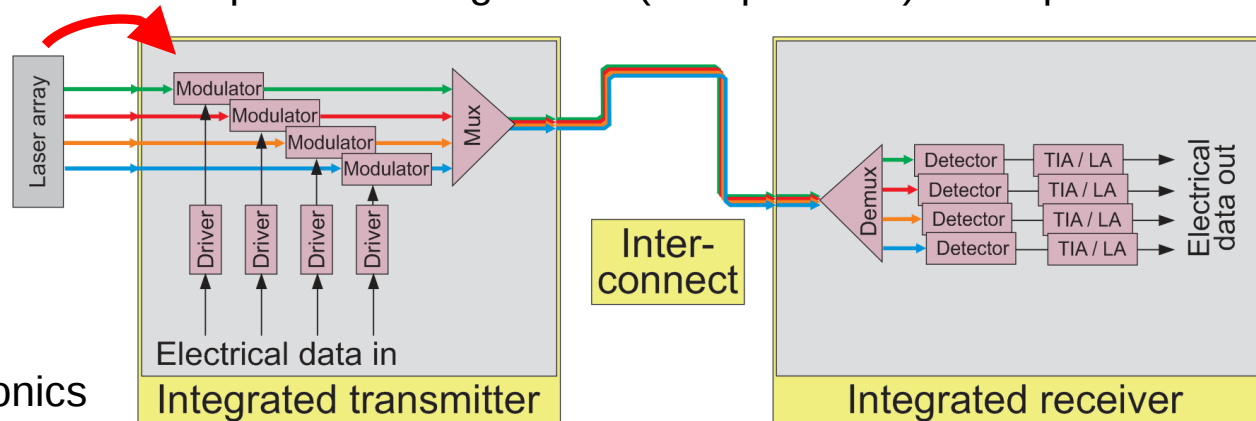
Photonics technologies for system-level integration

① Chip-level: CMOS silicon photonics + Active photonics devices

- Si photonics provides all required building blocks (except lasers) on chip-level:

- Modulators
- Drivers
- Detectors
- Amplifiers
- WDM filters

+ CMOS electronics



② System-level: Scalable chip-to-fiber connectivity

- One step mating of numerous optical interfaces
- Provide electrical and optical signal routing capability
- Enable a simultaneous interfacing of electrical and optical connections

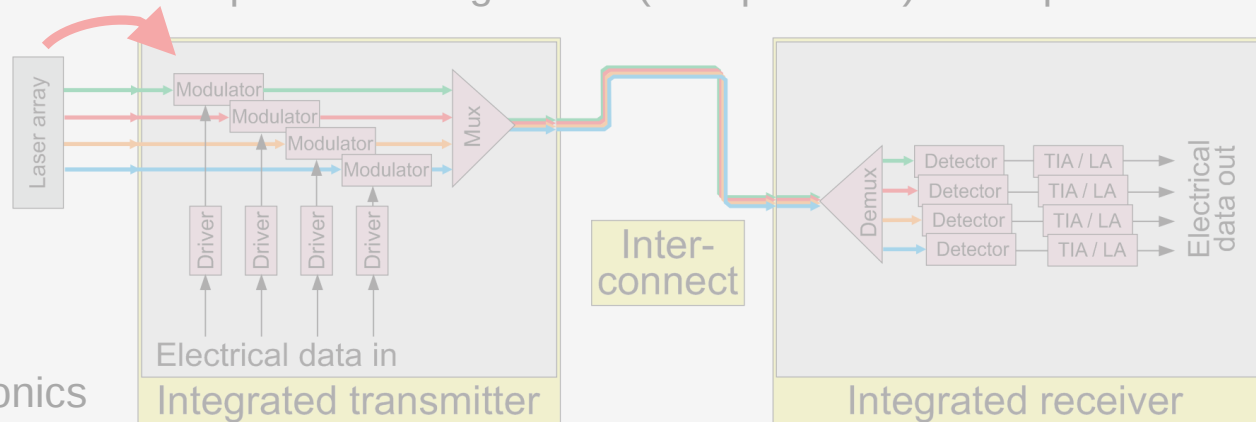
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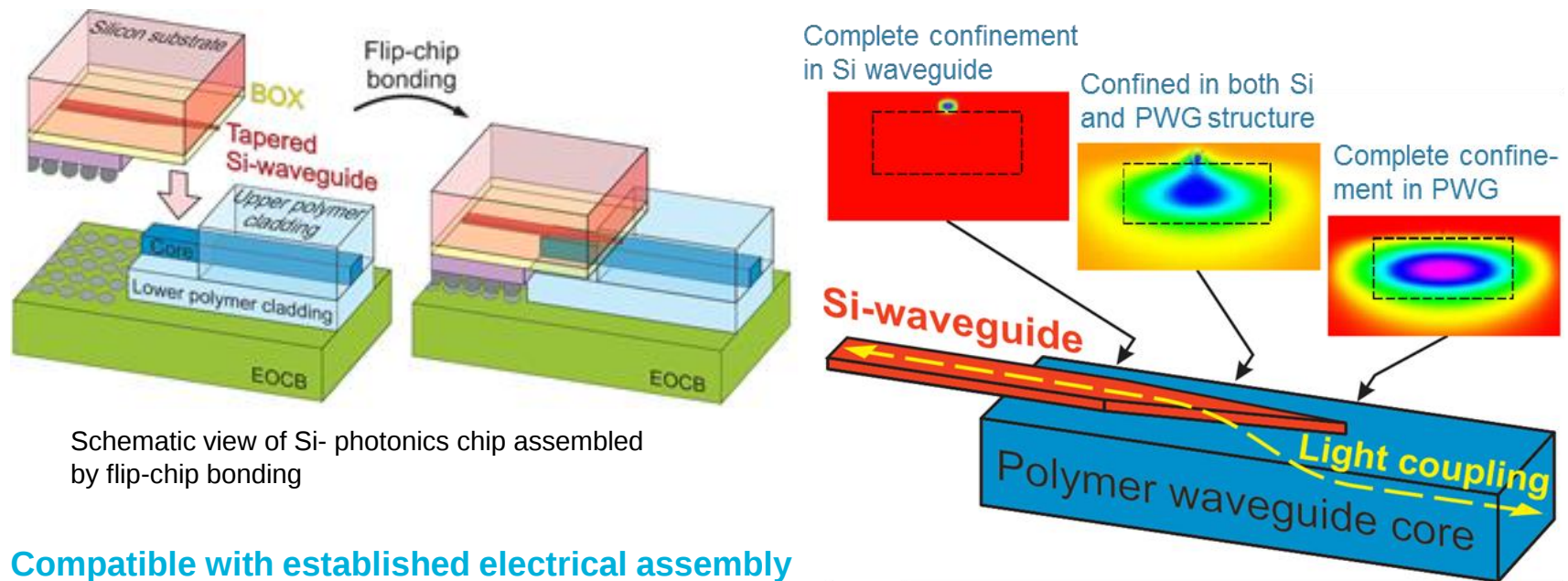
② System-level: Scalable chip-to-fiber connectivity

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Adiabatic optical coupling using polymer waveguides

Principle:

- Contact between the silicon waveguide taper and the polymer waveguide (PWG), achieved by flip-chip bonding, enables adiabatic optical coupling



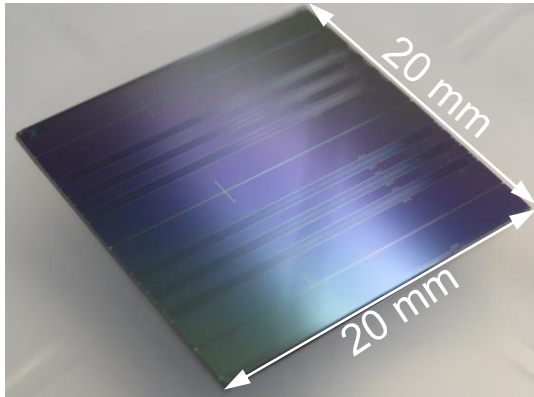
Schematic view of Si- photonics chip assembled by flip-chip bonding

- **Compatible with established electrical assembly**
- **Simultaneous E/O interfacing**
- **Scalable to many optical channels**

- J. Shu, et al. "Efficient coupler between chip-level and board-level optical waveguides." *Optics letters* 36.18 (2011): 3614-3616.
- I. M. Soganci, et al. "Flip-chip optical couplers with scalable I/O count for silicon photonics." *Optics express* 21.13 (2013): 16075-16085.
- T. Barwicz, et al. "Low-cost interfacing of fibers to nanophotonic waveguides: design for fabrication and assembly tolerances.", *Photonics Journal, IEEE* 6.4 (2014): 1-18.

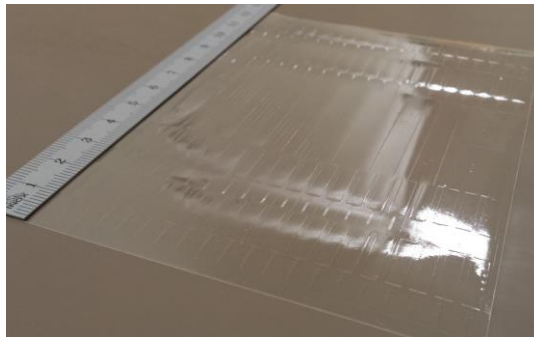
Single-mode polymer waveguide technology

SM polymer waveguides on **chips** (e.g. Si photonics chips)



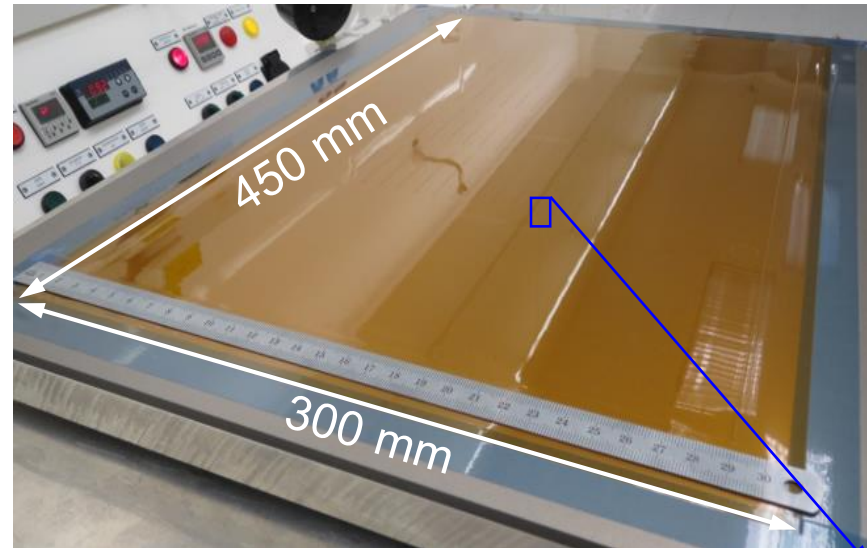
Chip-size

SM polymer waveguides on **wafer-size flexible** substrates

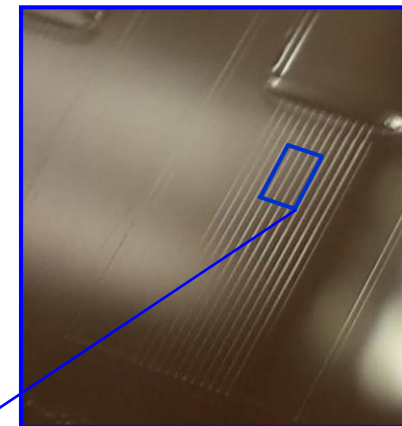
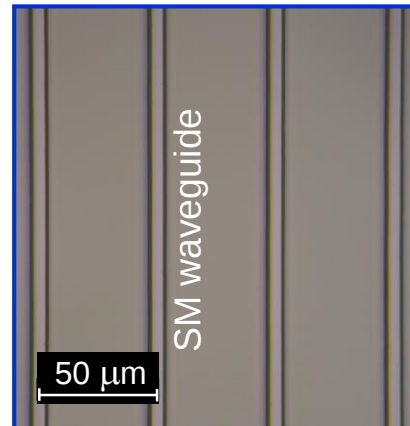


Wafer-size

SM polymer waveguides on **panel-size flexible** substrates



Panel-size

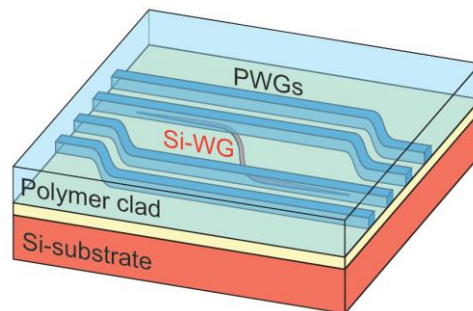
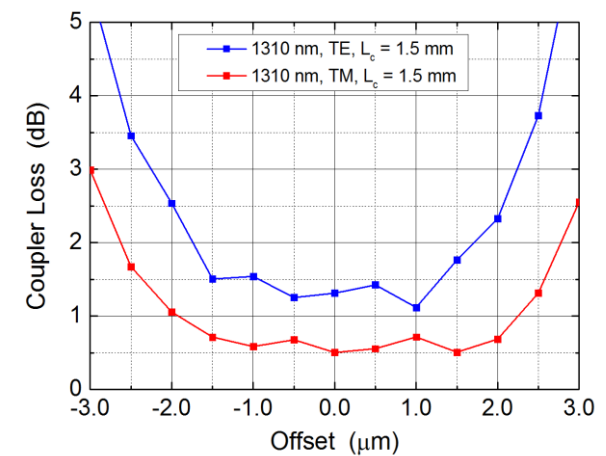
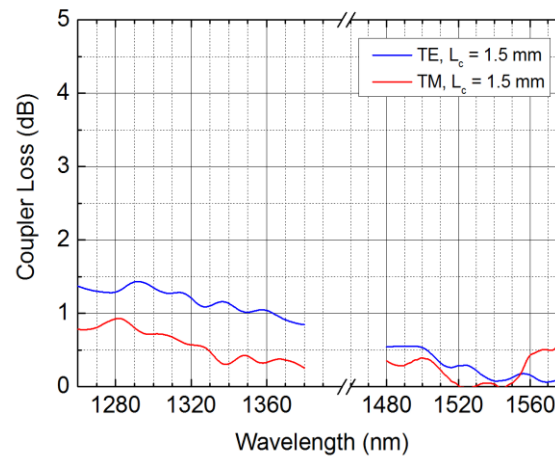
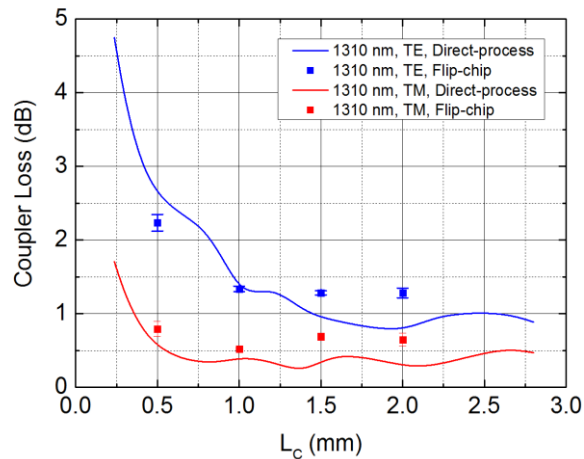


R. Dangel, et al. Optics Express, 2015

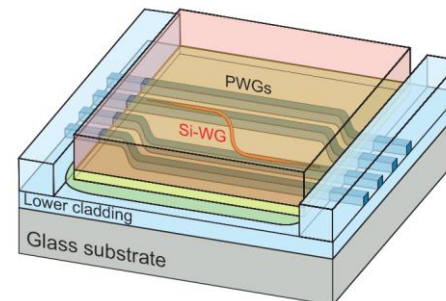
Adiabatic coupler loss characterization

Coupler loss measurement:

- Direct-process vs Flip-chip bonding approach
- For $L_c \geq 1.0$ mm: Coupler loss < 1.5 dB, PDL ≤ 0.7 dB
- Operating in the O and C-band



Polymer waveguides processed on chip



Polymer waveguides attached by flip-chip bonding

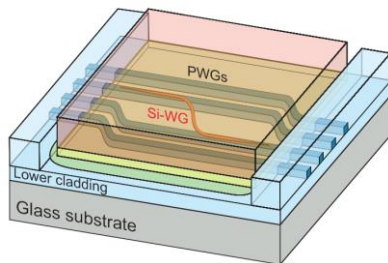
Insertion loss characterization (1)

Insertion loss measurement:

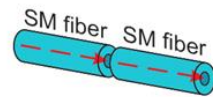
- Wavelength sweep over O-band
 - Full path vs ref. PWG path
- Wavelength dependency mainly in the PWG

Insertion loss per 2 facets

Measurement ①

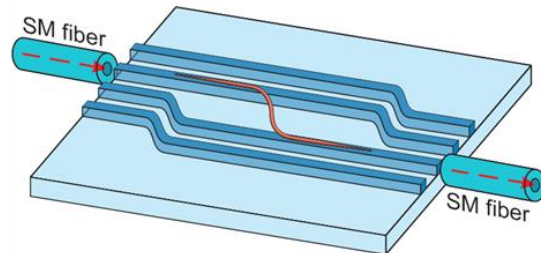


Schematic view of Si-photonics chip assembled by flip-chip bonding

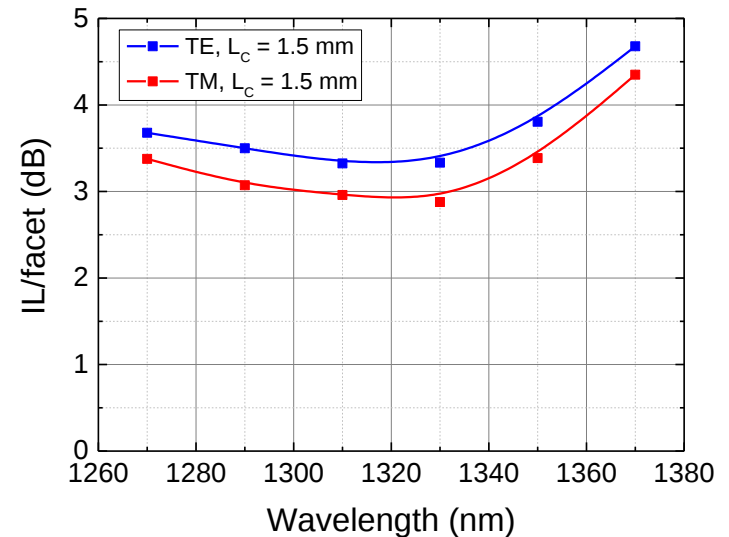
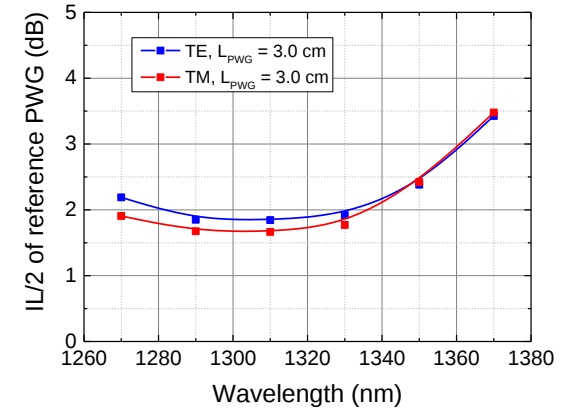


Fiber → Fiber

Measurement ②



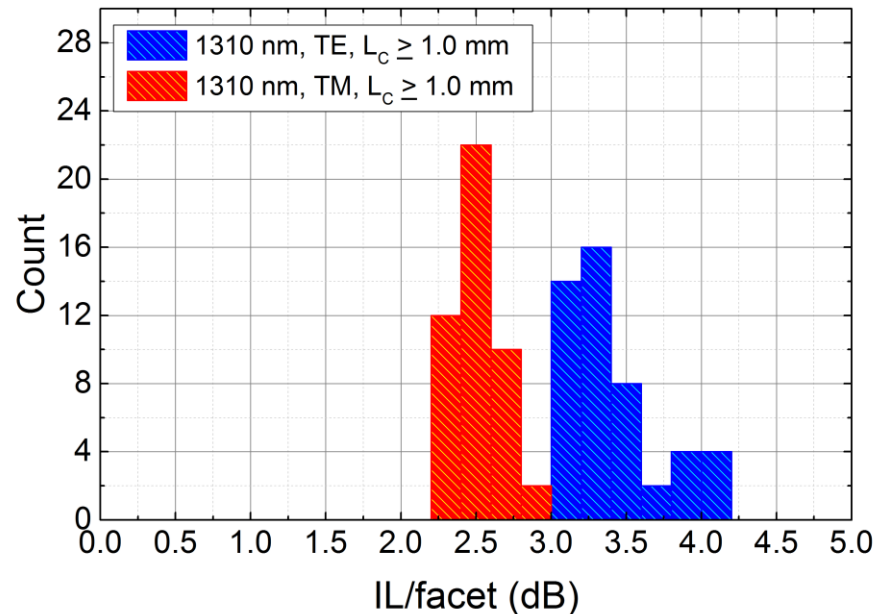
Fiber → PWG → SiWG → PWG → Fiber



Insertion loss characterization (2)

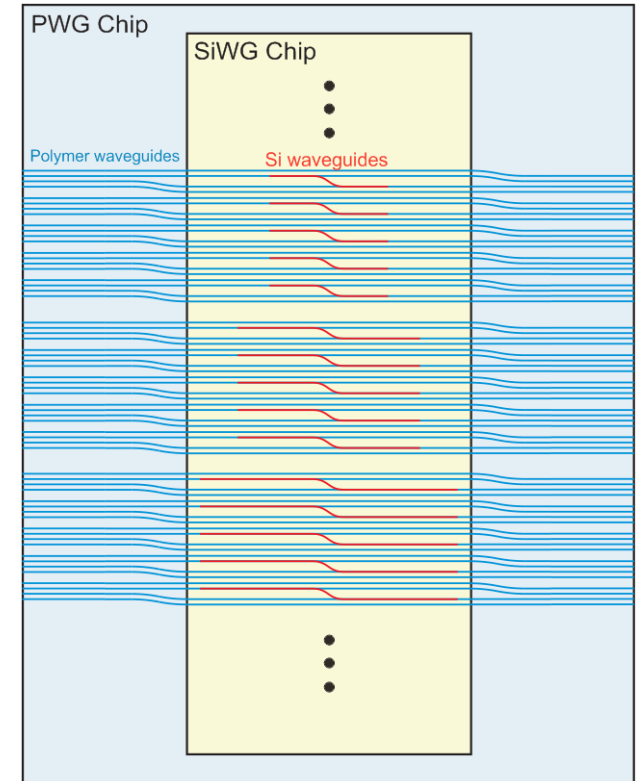
Insertion loss statistics:

- High number of optical interfaces: **152** per chip
 - 94 interfaces for silicon couplers
 - 58 interfaces for polymer waveguide references
- For $L_C = 0.5, 1.0 \text{ mm}, \dots, 3.0 \text{ mm}$



94 optical interfaces per chip, assembled simultaneously

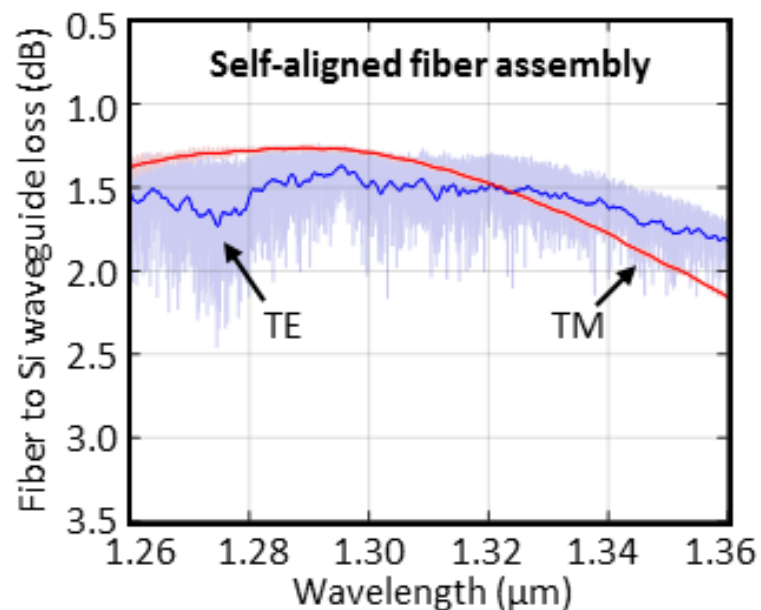
- 17 connections used for offset measurements (34 interfaces)
- 30 connections for coupler length variations (60 interfaces)
- 24 (48 interfaces) from 25 connections plotted above, only one connection not functional



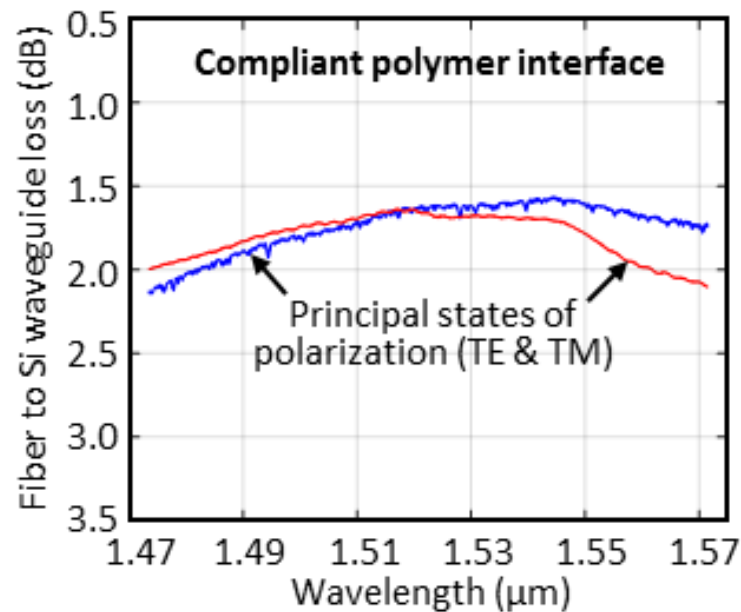
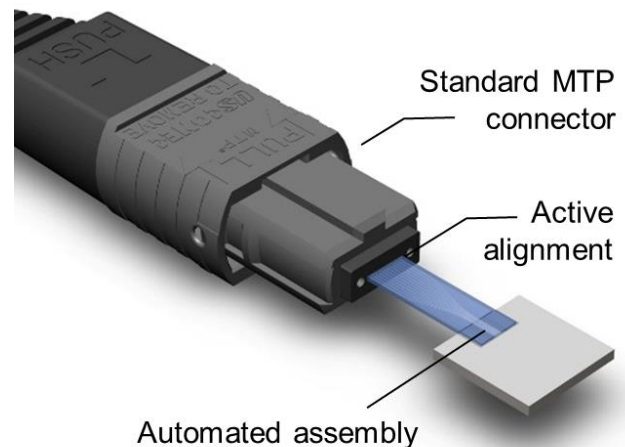
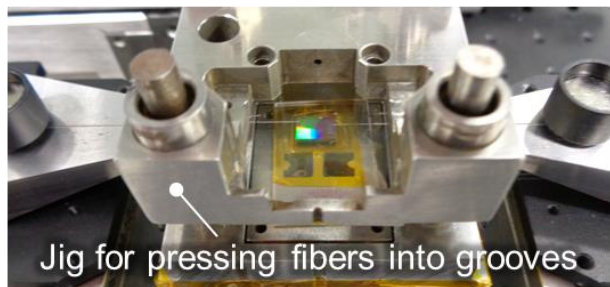
Top-view of Si-photonics chip assembled by flip-chip bonding

~100 functional assembled optical IO's per chip

Optical results for high throughput compatible approaches



Measurement setup



Barwicz *et al.*, OFC'17 Tu3K.4

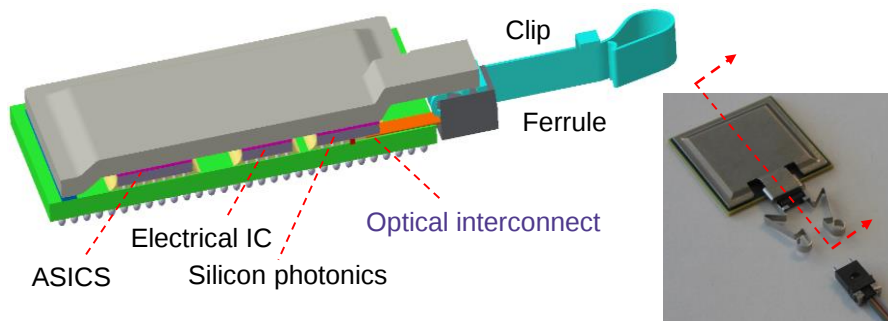
High throughput assembly strategy – Singlemode / Multi-connection

Development by IBM Assembly and Test Services (Bromont). Design concepts by IBM TJ Watson research.



Microelectronics assembly infrastructure

- Leverage std microelectronics assembly tools & processes.
- Passive self-alignment to reduce assembly time & cost
- Scalable volumes - High throughput automated assembly
- Scalable multi-channel connections



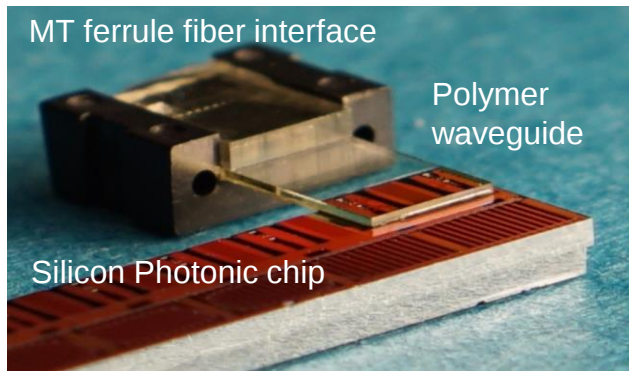
Sectional view of microelectronic module with integrated optics

- Optics integration with microelectronics
- Using microelectronics packaging knowhow

Low cost packaging / Scalable / Seamless integration of optics with microelectronics

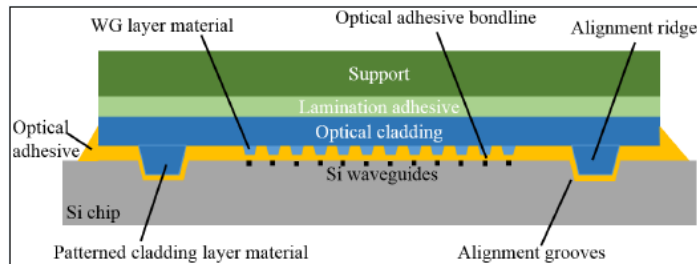
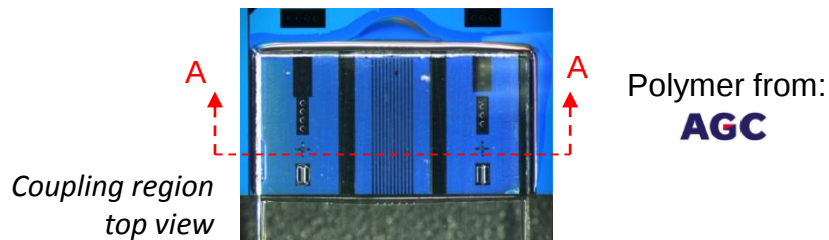
More details: Invited talk Tu3K.4 – Tymon Barwicz

Approach #1: Compliant polymer assembly



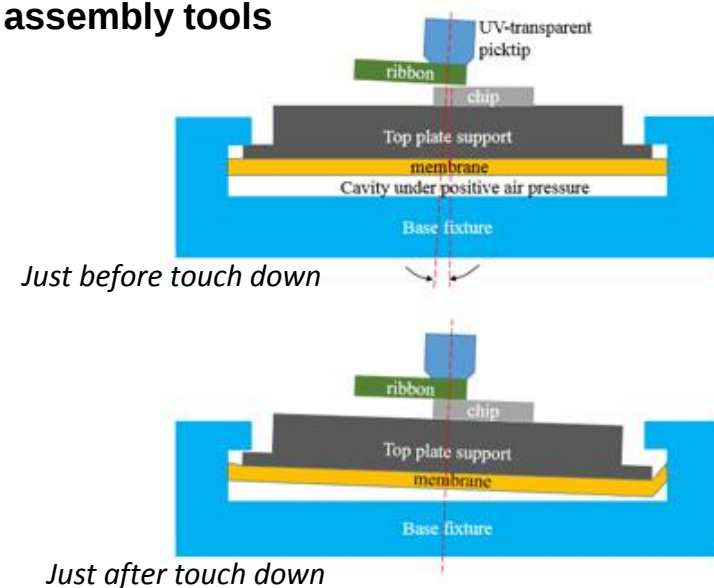
- Dense parallel channel array (50 μ m pitch)
- Wide spectral range (O,S,C,L bands)
- Polarization independent
- Compliant material for CPI risk mitigation
- Assembly using high throughput pick n place tools

Innovations to enable use of standard microelectronic assembly tools



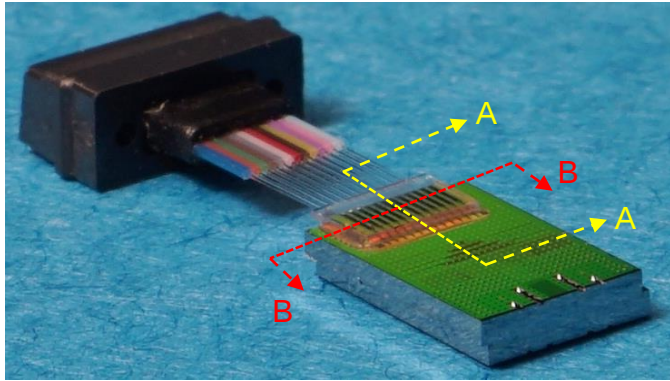
Section A-A

Passive self alignment using ridge / groove
Removes high precision placement requirement



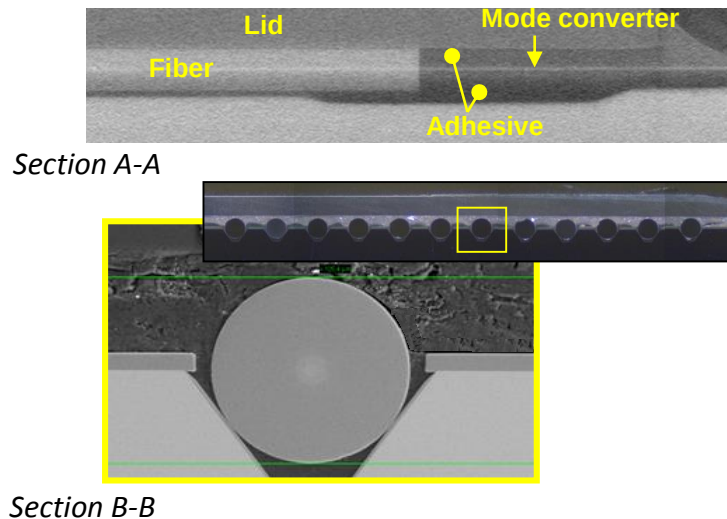
Dynamic parallelism adjustment using flexible membrane with pressure cavity

Approach #2: Fiber array assembly

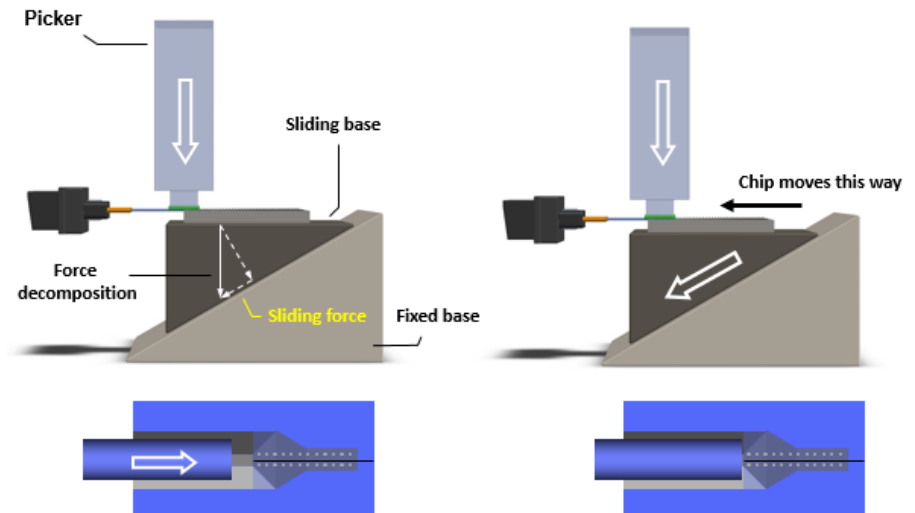


- Parallel channel array
- Wide spectral range (O,S,C,L bands)
- Polarization independent
- Assembly using high throughput pick n place tools

Innovations to enable use of standard microelectronic assembly tools



Passive self alignment using V-grooves
Removes high precision placement requirement



Sliding plane base for fiber butting
Convert vertical placement force to horizontal sliding

Acknowledgements

- Collaborators in IBM
 - Folkert Horst, Daniel Jubin, Norbert Meier, Roger Dangel, Antonio La Porta, Jonas Weiss
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- Co-funded by the European Union Horizon 2020 Programme

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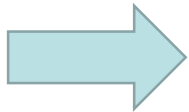


Agreement No 688572



Summary

- Adiabatic optical coupling enables efficient, broadband and polarization independent silicon photonics chip-to-fiber interfacing
 - Demonstrated simultaneous interfacing of up to 152 channels per chip
 - Fiber-to-chip insertion loss < 4 dB, PDL < 0.7 dB
- Low cost / High throughput single-mode optical interconnect assembly techniques leveraging existing microelectronic packaging infrastructure



Path towards high level of electro-optical integration & scalability

Thank you for your attention

- Bert Jan Offrein, ofb@zurich.ibm.com
- Tymon Barwicz, tymon@us.ibm.com
- Paul Fortier, pfortier@ca.ibm.com