



DESIGN, AUTOMATION & TEST IN EUROPE

27 – 31 March, 2017 · STCC · Lausanne · Switzerland

The European Event for Electronic
System Design & Test

Silicon Photonics Scalable Design Framework: From Design Concept to Physical Verification

Hossam Sarhan

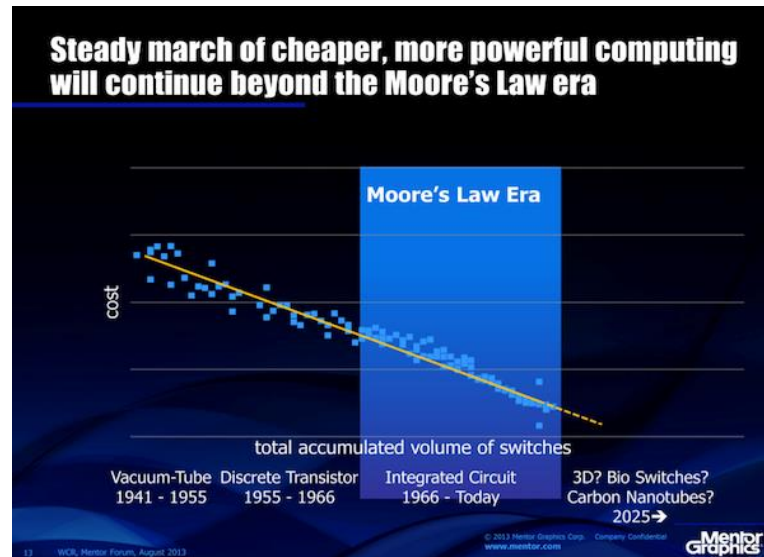
Technical Marketing Engineer

hossam_sarhan@mentor.com



Objective: Scalable Photonics Design Infrastructure

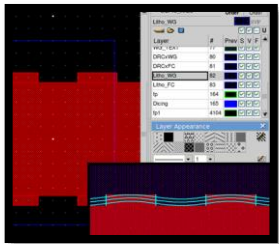
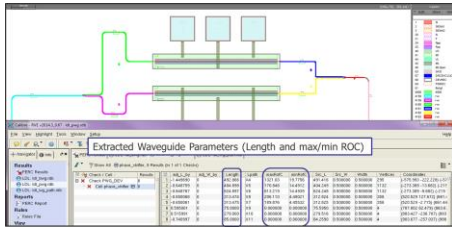
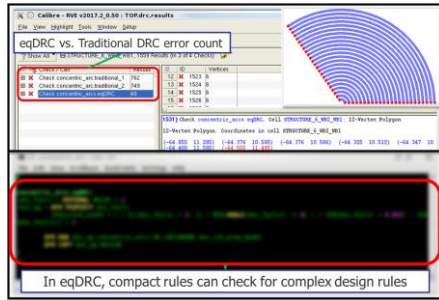
- The electronic IC market has benefitted greatly from the scalability attributed to Moore's Law
- Meanwhile the photonic market remains limited to relatively small circuits
 - Design differentiation still focused on device physics as opposed to novel device and sub-circuit re-use.



What is Required to Move Forward?

- **Scalable Design Tools**
 - Large scale optical simulation based on compact models
 - Automated/semi-automated layout
 - Physical verification and DFM
- **Dedicated Process Development Kits (PDKs)**
 - Pre-characterized compact models
 - Pre-characterized device pcells
 - Process specific PV and DFM decks
 - Validated tool settings
- **Reference Flows**
 - Validated design flows
 - Device characterization procedures
 - Test and measurement methodologies
- **Validated Re-Usable IP?**

Partnering to provide IoT Solutions



Photonic ICs

Physical Verification

Analog RF

Parasitic Extraction

3D/2.5D IC

Lithography Impacts

MEMS

Mask Data Preparation

Tanner
EDA

Calibre

Partners in
Photonics

LUCEDA
PHOTONICS



Phoenix Software
Solutions for Micro and Nano Technologies



Partners in MEMS



SoftMEMS
Bringing MEMS to the Mainstream

Mentor's Custom IC Design Tools

Joint support for Pyxis and Tanner EDA Products

- **Both utilize common PDK development utilities**
 - Supports Python based PCells
 - Supports OA based PDK development
- **Both support interface to Mentors “enterprise level” simulation and verification tools**
 - Full support for Calibre® Physical Verification tools
 - Full support for Eldo Platform with Verilog-A support
- **Tanner EDA will be fully OA native this year**
 - L-Edit is Open Access native
 - S-Edit will be Open Access native in 17.2 release



Mentor's Photonic IC Design Flow

Calibre's Scalability with Tanner EDA platform

Native Open Access Design Environment

Design Capture

Tanner S-Edit

- Upcoming OA Native support in v17.2
- Photonic SDL support
- Supports Pre/Post-layout simulation

Layout Implementation

Tanner L-Edit

- Advanced Curves
- X-Section
- Photonic SDL Support

Luceda IPKISS

- Photonic PCells
- Waveguide generation
- Layout direct simulation

Comprehensive Open Access PDK Support

- **Luceda IPKISS PCells**
- **PyCell Studio PCells**
- *Future OA-API Plugins*

Electrical Simulation

- **Eldo Platform with Verilog-A support**
- **Tanner T-Spice with Verilog-A support**

Photonic Simulation

- **Luceda CAPHE Simulator**
- *Future Photonic Simulation plugins*

Calibre RVE / Calibre Interactive

Lithography Simulation

Calibre LFD

Design Verification

*Calibre nmLVS
PERC,
PERC LDL*

Photonic DRC and Chip Finishing

*Calibre nmDRC,
Calibre Yield*

Calibre Verification Platform

Mentor's Photonic IC Design Flow

Customer Driven

Native Open Access Design Environment

Design Capture

Tanner S-Edit

- Upcoming OA Native support in v17.2
- Photonic SDL support
- Supports Pre/Post-layout simulation

Layout Implementation

Tanner L-Edit

- Advanced Curves
- X-Section
- Photonic SDL Support

Luceda IPKISS

- Photonic PCells
- Waveguide generation
- Layout direct simulation

Comprehensive Open Access PDK Support

- **Luceda IPKISS PCells**
- **PyCell Studio PCells**
- *Future OA-API Plugins*

Electrical Simulation

- **Eldo Platform with Verilog-A support**
- **Tanner T-Spice with Verilog-A support**

Photonic Simulation

- **Luceda CAPHE Simulator**
- *Future Photonic Simulation plugins*

Calibre RVE / Calibre Interactive

Lithography Simulation

Calibre LFD

Design Verification

*Calibre nmLVS
PERC,
PERC LDL*

Photonic DRC and Chip Finishing

*Calibre nmDRC,
Calibre Yield*

Calibre Verification Platform

Physical Verification Challenges

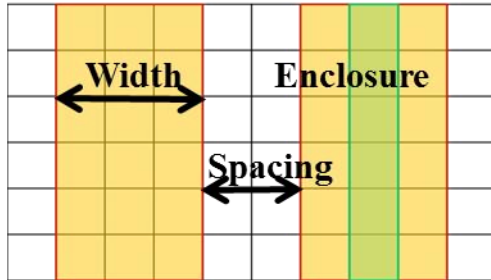
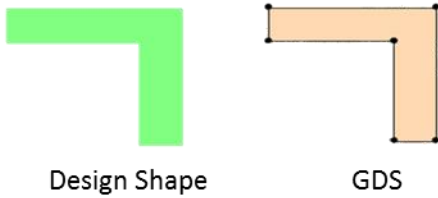
- **Rendered Curves Results in False DRC Errors**
- **Difficulty in LVS Device Recognition and Optical Property Comparison**
- **Need to Pass Waveguide Interconnect Extraction to Post-Layout Simulation**
- **Mask Generation and Silicon Manufacture Varies from Design Intent**



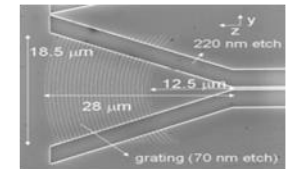
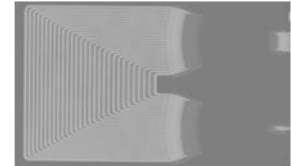
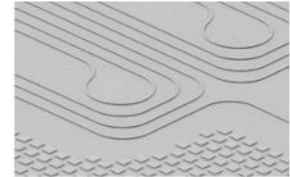
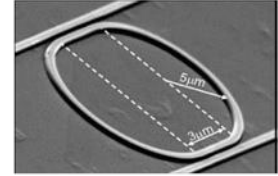
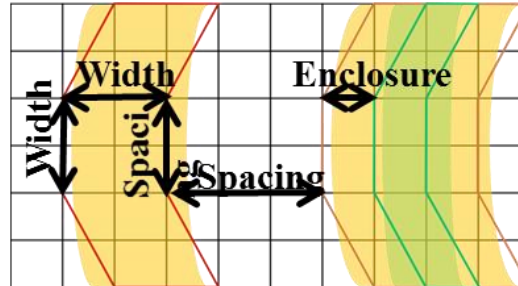
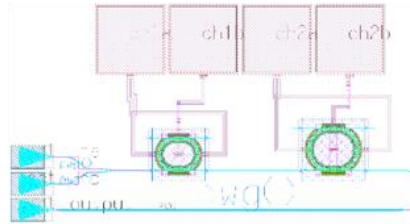
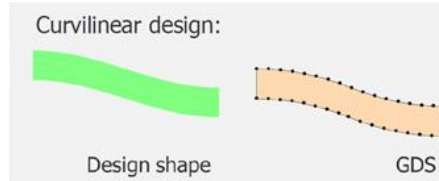
DRC FOR NON-MANHATTAN PHOTONIC DESIGNS

DRC on Si-Photonics Components

Electronic IC (EIC) Layout (Manhattan Shapes)



Photonic IC (PIC) Layout (Non-Manhattan Shapes)



SEM images, Europractice

Addressing DRC Photonics Challenges

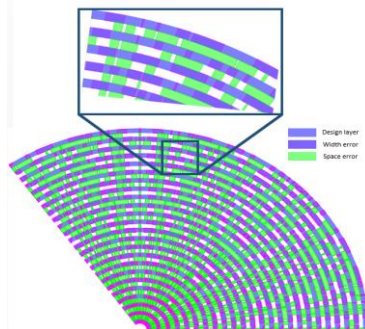
I. False Error Induced by grid Snapping (1/2)

- **Concentric arcs:**

- **Fabrication constraint :**

Width > 1 μm , **Space** > 1 μm

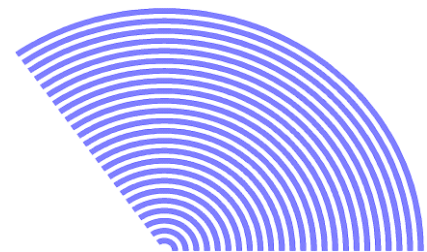
Error_width := width < 1 μm
Error_space := space < 1 μm } **Traditional DRC Check**



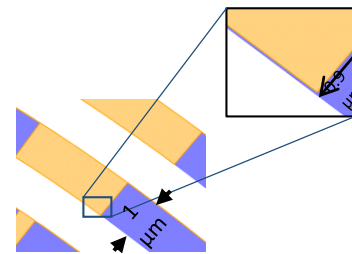
Concentric Arcs with DRC violations

Number of
Violations = **1500**

"Silicon Photonics Design Rule Checking: Application of a Programmable Modeling Engine for Non-Manhattan Geometry Verification", presented at VLSI-SoC 2014



Concentric Arcs components



Addressing DRC Photonics Challenges

I. False Error Induced by grid Snapping (2/2)

- **Concentric arcs:**

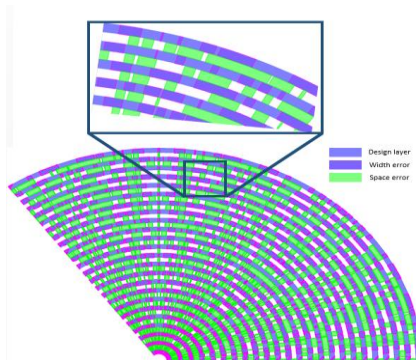
- **Fabrication constraint :**

Width > 1 μm , Space > 1 μm

Error_width := width < 1 μm
Error_space := space < 1 μm } **Traditional
DRC Check**



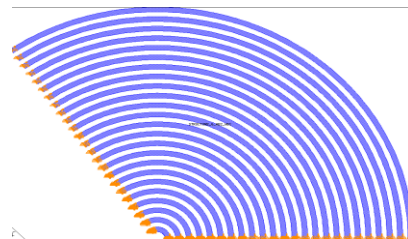
**New DRC
Check using
Calibre EqDRC**



Number of
Violations
= **1500**

Number of
Violations
= **145**

All_Thin_rod := Width (rod) < 1 μm
W = Width (Thin_rod_width)
 α = Angle (Thin_rod_width)
L = Length (thin_rod_width)
If (0 < α < max_angle) OR (L < max_length) Then:
Error_rod_width := Width(rod) < (1 - tol*) μm
Else:
Error_rod_width := Width(rod) < max_width μm
*.tol tolerance determined by applying tolerance factor
according to fabrication grids and DRC rounding factors.
(2sqrt(2). Grid)



DRC Post Processing using EqDRC capabilities

Concentric Arcs with DRC violations

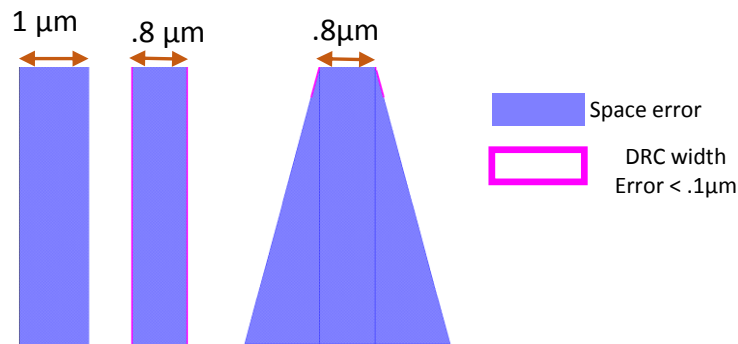
"Silicon Photonics Design Rule Checking: Application of a Programmable Modeling Engine for Non-Manhattan Geometry Verification", presented at VLSI-SoC 2014

Addressing DRC Photonics Challenges

II. Enable Multi-Dimensional Check (1/2)

- **Taper test structure**

- Taper is a trapezoidal shape.
- End width (w) varies from .05 to 1 μm
- Fabrication constraint :
 - Line width > 1 μm
 - For Robust strip design : relaxed width constraint with increased angle



Addressing DRC Photonics Challenges

II. Enable Multi-Dimensional Check (2/2)

Traditional DRC Rule (Complicated and non accurate)

Error_Width_1 := width < w1 when $0 < \alpha < \alpha_1$

Error_Width_2 := width < w2 when $\alpha_1 < \alpha < \alpha_2$

Error_Width_3 := width < w3 when $\alpha_2 < \alpha < \alpha_3$

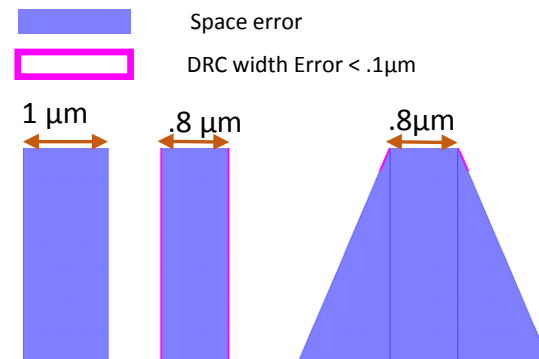
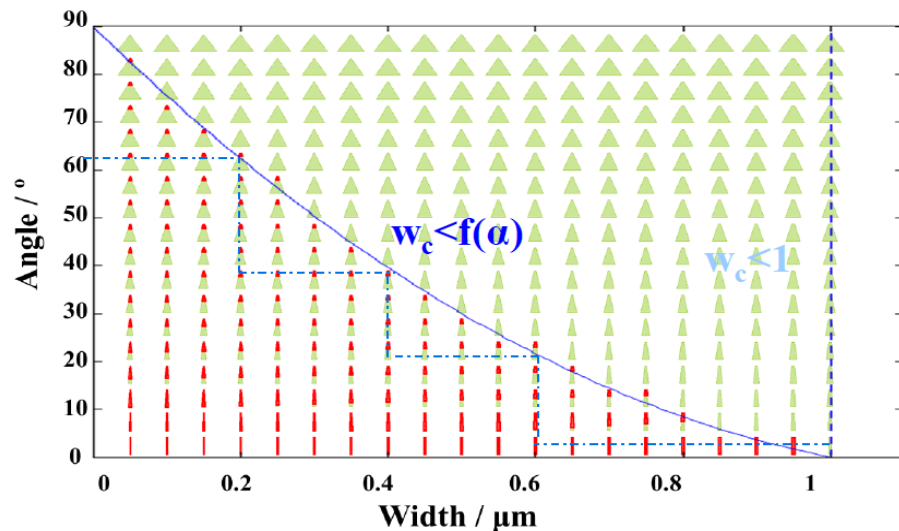


EqDRC Rule (Simple and Accurate)

α = Angle (rod)

$\alpha_{\text{critical}} = f(\text{width}(\text{rod}))$

Thin_rod := $\alpha_c / \alpha > 1$





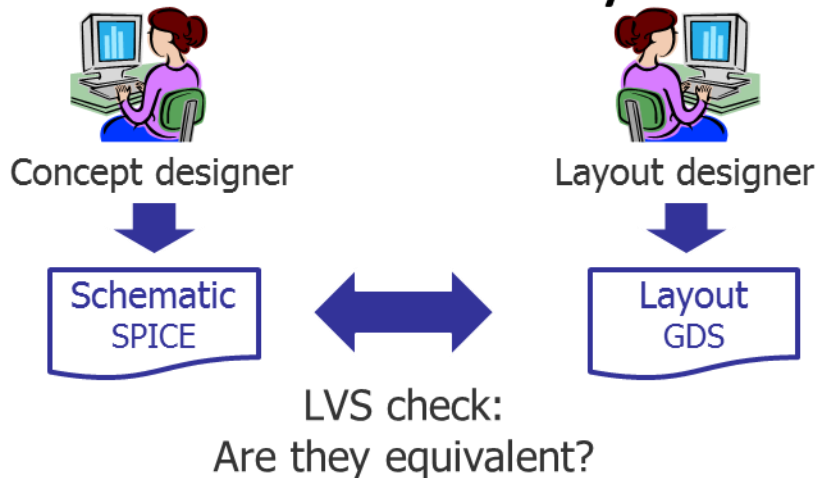
PHOTONIC LVS AND POST-LAYOUT SIMULATION

Photonic Layout versus Schematic (LVS) Check

– Why Needed?

- Photonic designers are used to a “Layout-centric” design flow
- But as more complex and larger scale designs emerge, IC design flow-like methodology is required – “Schematic/Layout” design flow

➡ LVS to check if schematic and layout are equivalent

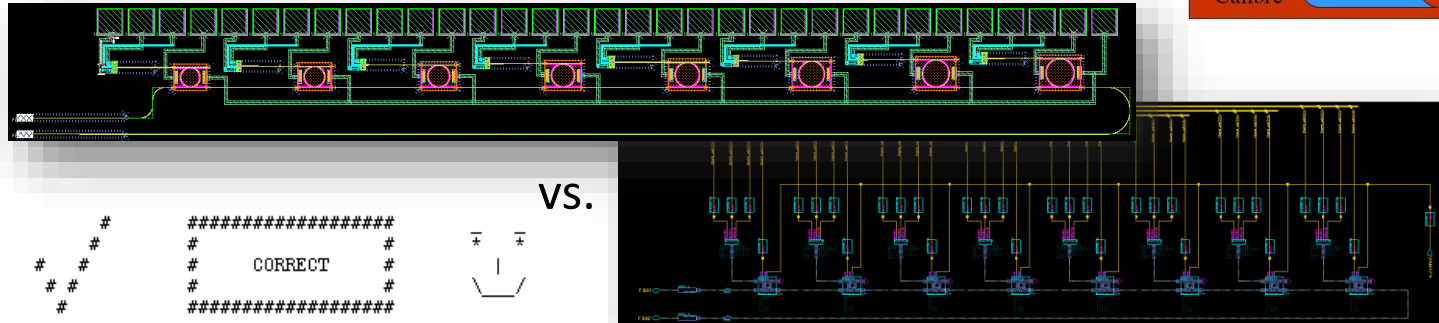
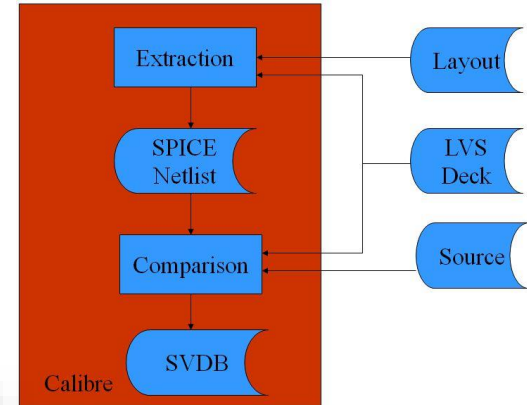


LVS equivalent:

- Circuit topology – Device type and count, Connectivity
- Device topology

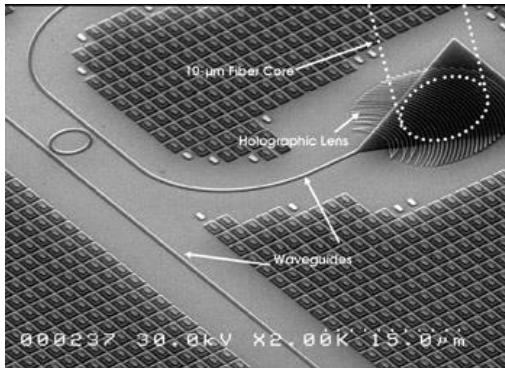
LVS Overview

- Ensures the schematic of the design is equivalent with the layout
- Extraction Phase
 - Connectivity extraction
 - Device Extraction
 - Parameter Extraction
- Comparison Phase
 - Extracted design VS. Source design
 - Property Tracing
 - Discrepancy reporting

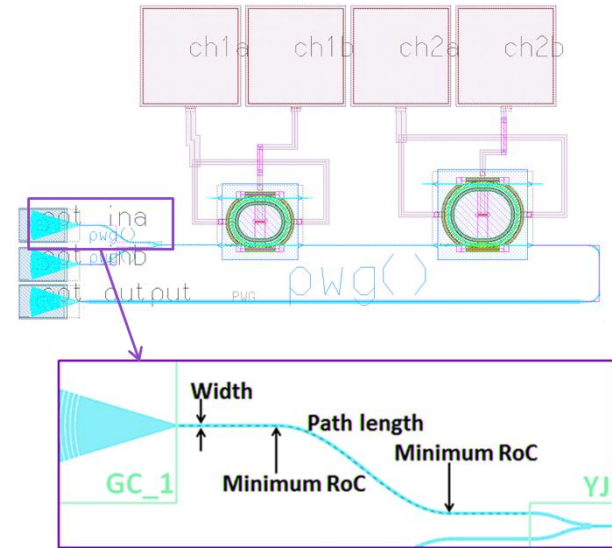


What's New for Photonics LVS

- **Wild design shape**
 - Non-Manhattan or curvilinear
- **Extraction and careful validation required on non-traditional geometrical parameters:**
 - Bend curvature
 - curvilinear path length
- **Those properties can be context dependent**

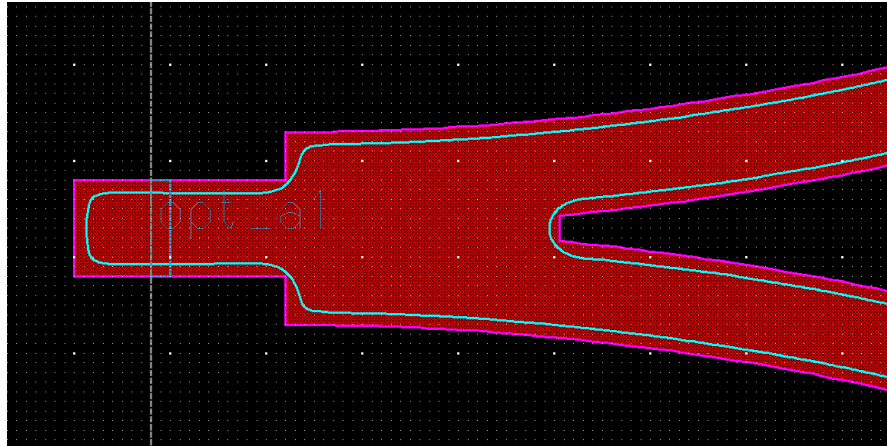


Luxtera



Litho Impacts on Silicon Photonics

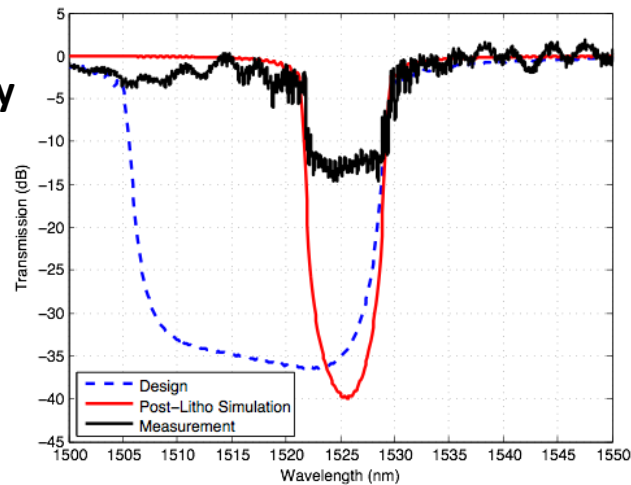
- **Optical Simulations Often do not Match Silicon Results**
 - Litho simulation better captures 'as manufactured' structures
- **Recommended Litho-Aware Device Characterization**
 - Link to Lumerical Simulator improves device model parameters
 - Retargeting best practices to preserve intended topology



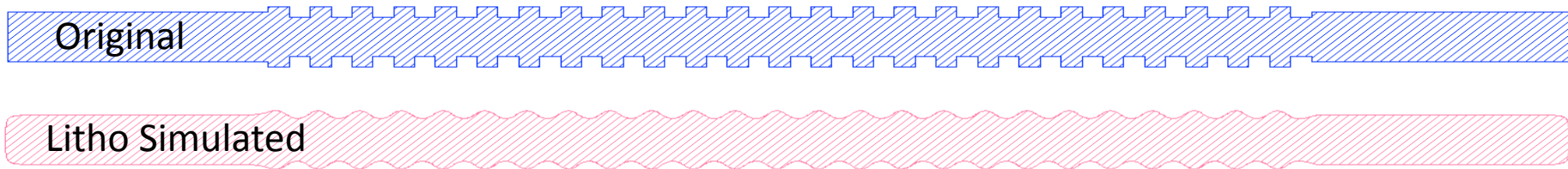
Lithography Simulation

Calibre LFD: Waveguide Bragg Grating Example

- **Waveguide Bragg Grating Example**
 - Ideal sharp edges of grating will smooth due to lithography resolution
 - This change in geometry will affect component attributes
- **Modeled layout passed to simulation**
- **Litho Correction simulations match experimental Bragg bandwidth.**



[Xu Wang, et al., "Lithography Simulation for the Fabrication of Silicon Photonic Devices with Deep-Ultraviolet Lithography", IEEE GFP, 2012](#)



The background of the slide features a dark blue gradient with numerous bright, thin, radial light streaks emanating from the top and bottom edges, creating a sense of depth and focus.

CONCLUSION

General Recommendations

- **Need DRC decks dedicated for silicon photonics design**
 - Cannot re-use decks targeted for IC design out of the box
 - Consider to add device shape-matching into DRC
- **LVS checking for accuracy**
 - Black-box devices for simple connectivity checking (shorts, opens)
 - Device shape matching (or push to DRC) for validation of pre-characterized device behavior
- **Litho-simulation**
 - Reduce mfg iterations through process modeling and simulation
 - Capture behavior impact through S-parameter update to optical simulation
 - Layout re-targeting or updated lithographic techniques to address outstanding issues

Growing Collaborations to provide “Full Scalable Si-Photonics Design Framework”

Mentor Graphics and Lumerical Unify Optical Design and Simulation Flow

WILSONVILLE, Ore., September 19, 2014 – Mentor Graphics Corporation, today announced a new collaboration with Lumerical, a leading provider of optical circuit simulation automation, today announced a new collaboration with Lumerical, a leading provider of optical circuit simulation methodologies that leverage the power of Lumerical's technology to perform optical circuit simulation.

With this integration, users can perform frequency analysis, perform simulation, and deliver a tremendous boost in design productivity. While traditionally used for circuit simulation, Lumerical's technology includes a built-in waveform-based analysis tool to deliver results.

Complementing the Pyxis Schematic Editor, renowned for its all angle editing capabilities, assemble photonic PCells using Lumerical's technology. To complete this full-flow silicon photonics design, ensuring photonic circuit simulation within the design flow.

Lumerical INTERCONNECT for

Optical circuit simulation within the design flow. circuit design and simulation to enable design capture, simulation, and verification. Simulations are run using the Lumerical INTERCONNECT, operating parameters of the photonic circuit.



News Events Archive

Mentor Graphics

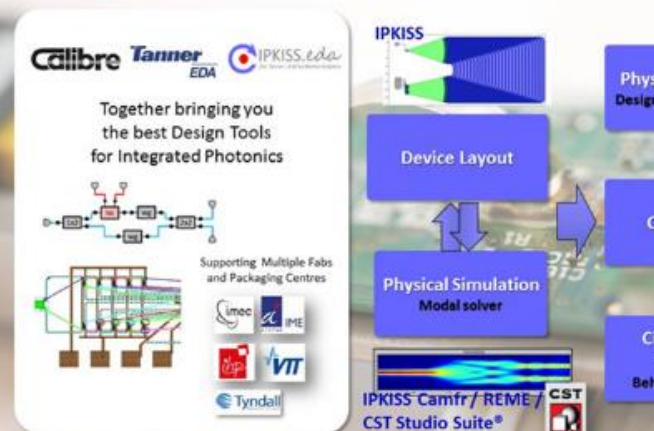
To support electronics design, Mentor Graphics in providing a full range of design tools and S-Edit.

Keywords: L-Edit, layout implementation

With the growing interest in dedicated photonics or mixed-signal oriented facilities are using sign-off dedicated Electronic Design Environments. These environments provide a platform to overcome some of the limitations of traditional design tools to facilitate all angle design concepts for functional verification. Also the other photonics tools are being integrated with Mentor Graphics as one of the leading software vendors to improve the design flow with leading edge photonic design tools.

Pyxis

Pyxis is the layout tool for photonic design. It is driven layout as well as a design capture tool. It has native support for Lumerical's technology and excellent custom design assembly capabilities.



Take control of your photonics design flow

Mentor Graphics and Luceda Photonics Deliver a PDK for imec's Integrated Silicon Photonics Platform

WILSONVILLE, Ore., March 20, 2017 — Mentor Graphics® Corporation (NASDAQ: MENT) today announced, in collaboration with Luceda Photonics, the availability of a full flow process design kit (PDK) for imec's Integrated Silicon Photonics Platform (iSiPP50G) to promote a 'right-the-first-time' approach to silicon photonics. The result is an exceptionally easy-to-use environment for integrated circuit (IC) design, simulation and layout with reliable, industry-standard physical verification for one of the industry's most advanced silicon photonics platform's available today.

The PDK supports the Tanner IC design suite along with Tanner Calibre® One for physical verification. Luceda's IPKISS.eda is integrated within Tanner's L-Edit full-custom layout tool providing drag-and-drop photonic components and fine-grained control over every aspect of the design flow. The imec process is suited to devices such as high-performance optical transceivers, optical sensing and read-out ICS and biomolecule detection.

The Tanner IC design suite supports analog, mixed-signal, RF, MEMS and silicon photonic design in one complete, highly integrated, end-to-end flow. Designers capture the schematic, perform analog and mixed-signal simulation, and lay out the physical design within this unified flow.

"Imec's iSiPP50G process technology is a key platform for silicon photonics companies," said Greg Lebsack, general manager Tanner EDA at Mentor Graphics. "Delivering this PDK is significant for the market as it eliminates the manual, error-prone steps to establish a repeatable, efficient design flow. Now companies can get their innovative products to market more quickly and reliably using cost-effective tools and manufacturing."

IPKISS.eda inside L-Edit gives photonic IC designers full control of their design framework to ensure that what they fabricate matches exactly how they designed it. In addition, it enables the reuse and distribution of the design work in a hierarchical framework that saves time and improves reliability.

"Our customers ask for help automating the mechanics of design so they can use their skills and knowledge to deliver functionality, performance and quality," said Pieter Dumon, CTO, Luceda. "The qualification of this PDK together with integration of IPKISS.eda within the Mentor Tanner design flow delivers just that."



www.mentor.com