From Circuit-Level to Component-Level Simulation and Back

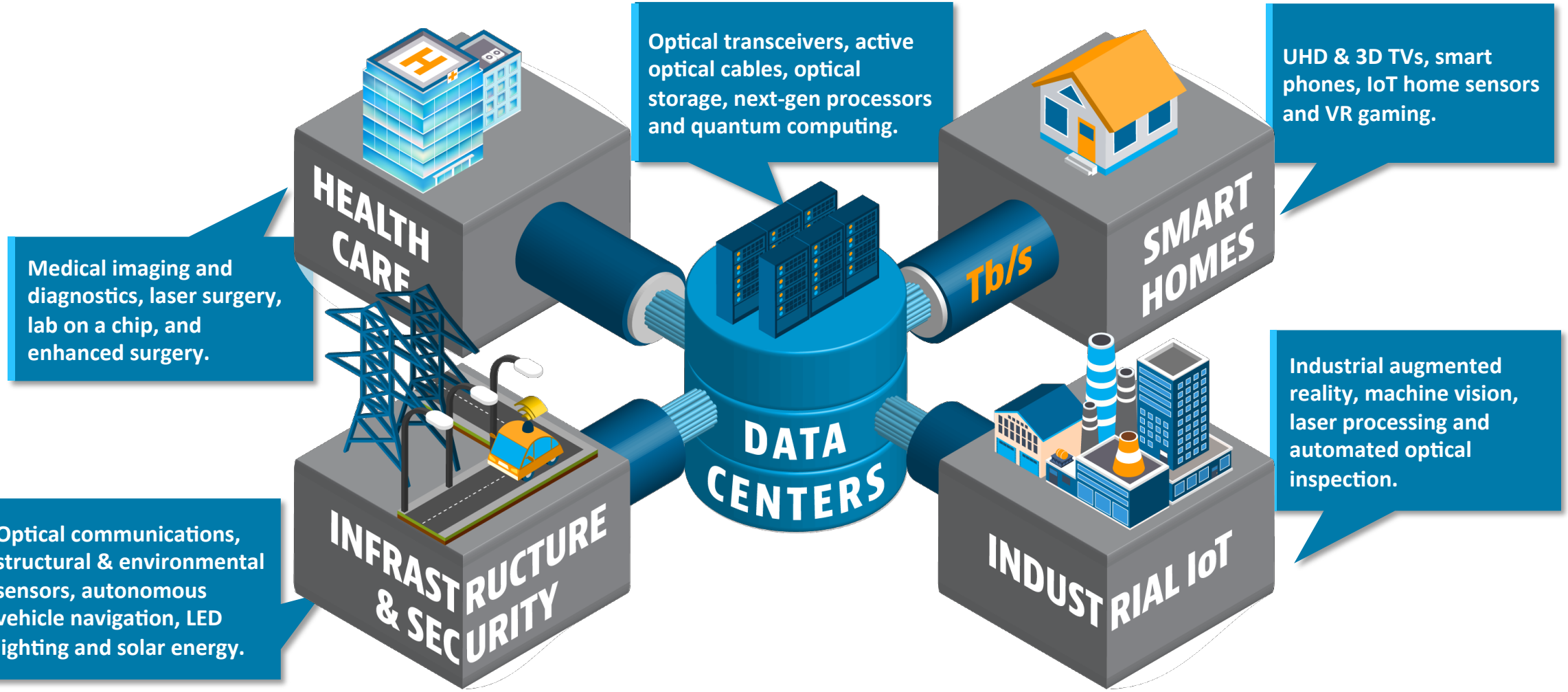
-

PDK Driven Design Automation

THE 3RD INTERNATIONAL WORKSHOP ON OPTICAL/PHOTONIC INTERCONNECTS FOR COMPUTING SYSTEMS (OPTICS WORKSHOP)

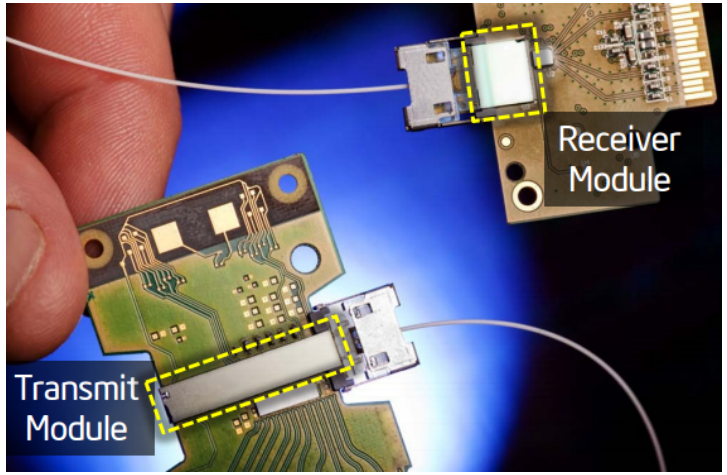
MARCH 31ST, 2017

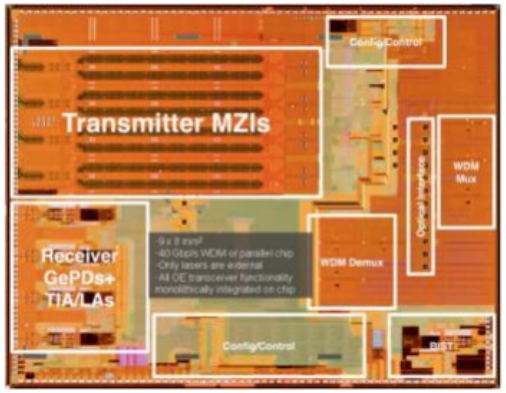
A Photonic Future

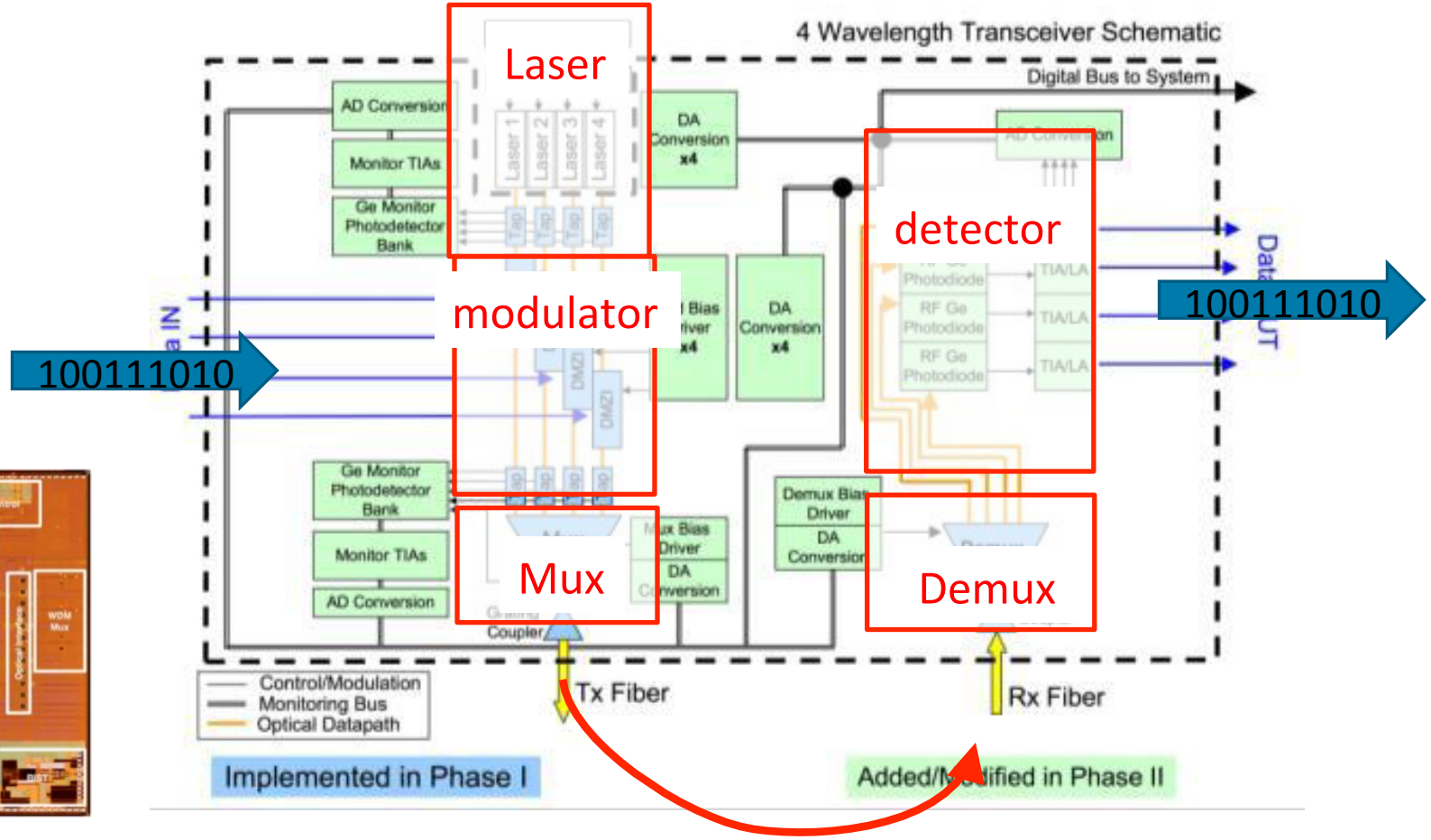


lumerical

Example: multichannel optical transceiver





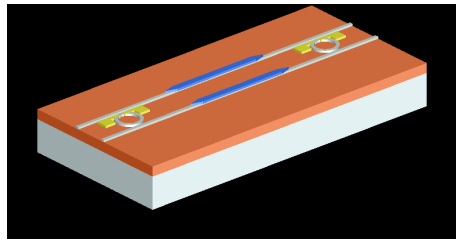


*DARPA-EPIC program

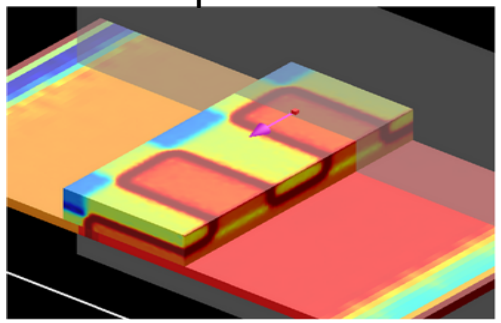
*Tom Palkert, "Technical Feasibility Using Silicon Photonics", Luxtera, Next Generation 100Gb/s Optical Ethernet Study Group, Plenary Meeting Material, Nov 8th - 10th, 2011, Atlanta, GA, USA

Integrated photonics

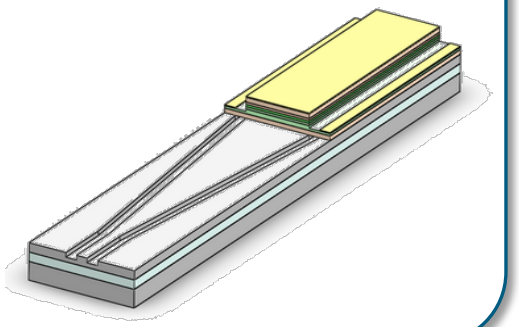
laser



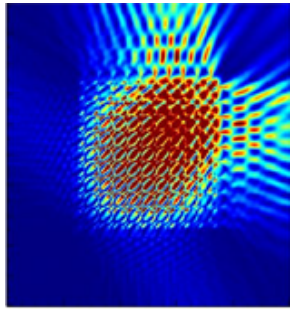
electro-optic modulator

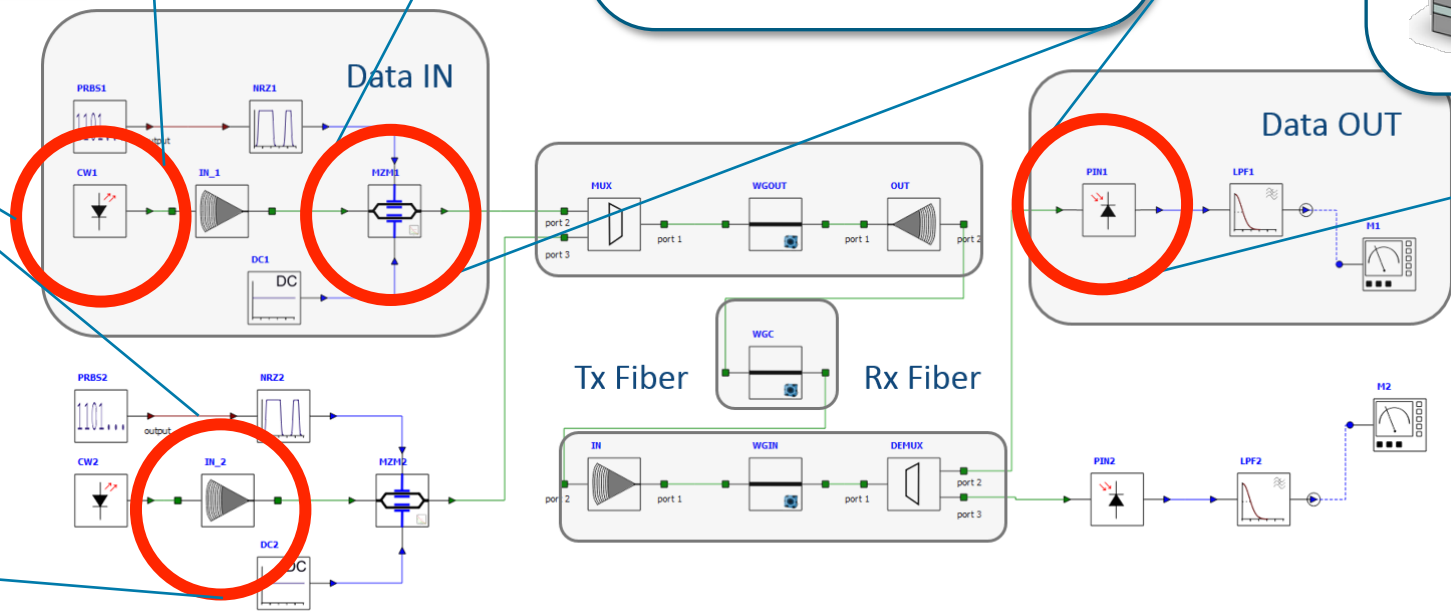


photodetector



grating coupler





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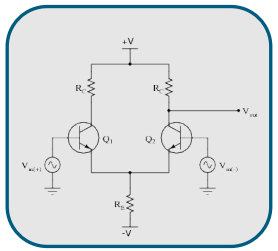
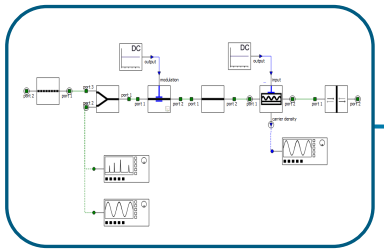
System modeling

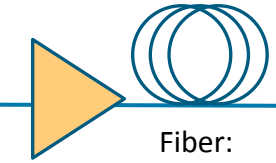
Transmitter





Electrical sub-circuit:
- Pre-emphasis
- Feedback loops
- D/A

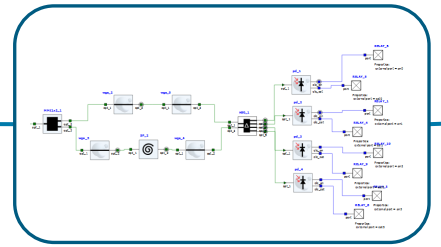
Optical sub-circuit:
- Wavelength
- Linewidth
- Reflections
- Carrier dynamics
- Mode
- Loss / Coupling



- Gain
- Noise

Fiber:
- Loss
- Dispersion
- Nonlinearities

Receiver



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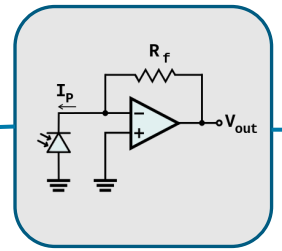

Electrical sub-circuit:
- TIA
- Amplification
- A/D

DSP
- Equalization (FFE / DEF
- Dispersion compensation
- LO Frequency Offset
- Phase Tracking
- Polarization crosstalk
- Synchronization
- Filtering

Analysis:
- BER
- Loss
- Dispersion
- Phase noise
- Chirp
- Polarization dynamics
- Inter-symbol interference
- Duty cycle distortion)
- Interaction of Noise and Signal

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Circuit / System simulation challenges

- Photonic circuit simulation needs to support:
  - Frequency domain simulation, e.g. transmission spectrum, insertion loss,…
  - Time domain simulation, e.g. BER, power budget,…
- Electronic / photonic co-simulation
  - … and also thermal
- Optical signal vs electrical signal
  - Electrical signal: Voltage / Current
  - Optical signal: propagates bidirectionally (reflections!), is multi-mode, in multiple frequency bands, and accumulates a phase.
- Lack of photonic compact models (behavioural models)
  - Validation of calibrated models to fabrication process

Integrated Photonics Designers

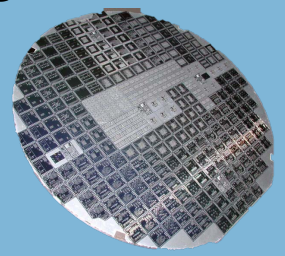
Today

Design

Component
Models/PDK
Circuit
Layout
Mask

<u>Technology Focus</u>
Many tools
Limited integration
PhD level expertise

Fabricate

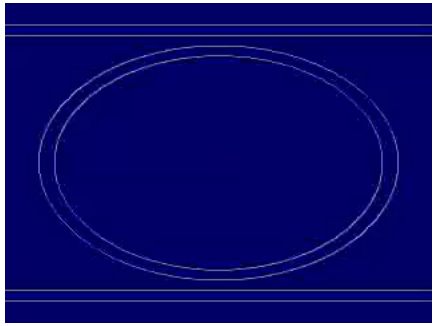


Specialized Vendors
Custom Packaging
MPW & Low volume

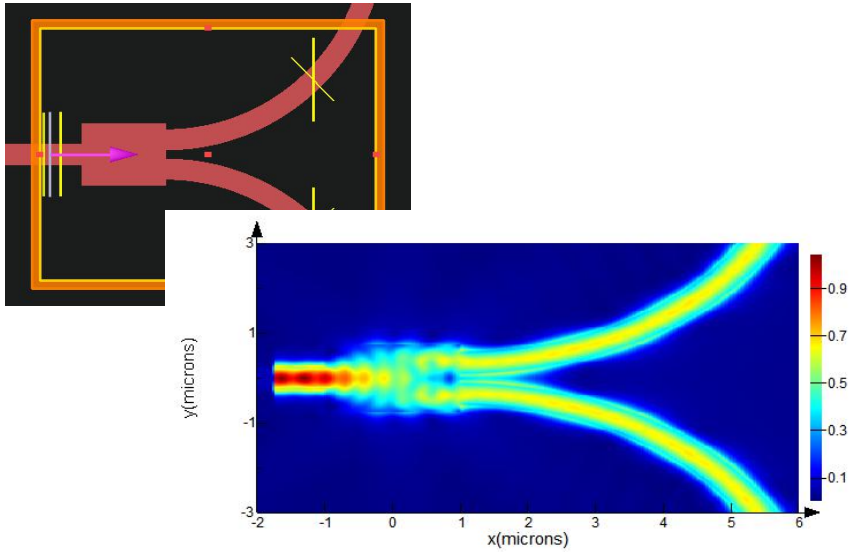
Challenges:

- Single photonics PhDs in charge of the entire framework
- Usually layout driven rather than schematic driven
- Limited circuit/system simulation capabilities
- In house code to tie different tools together

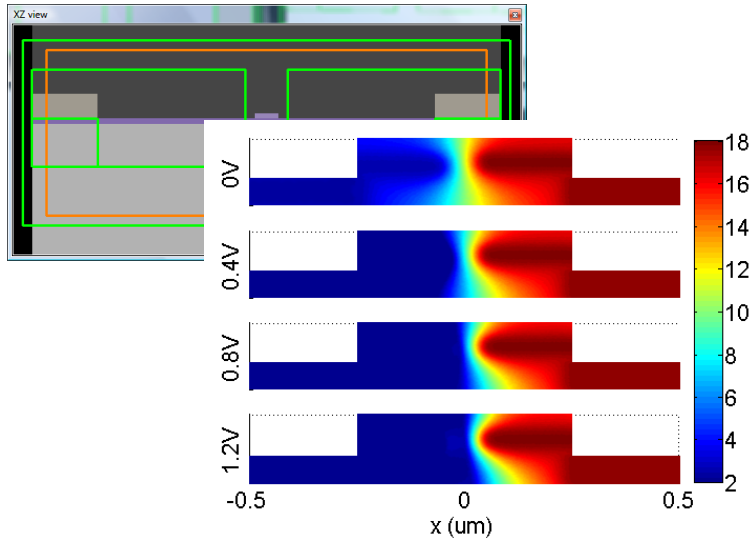
Component-level simulation



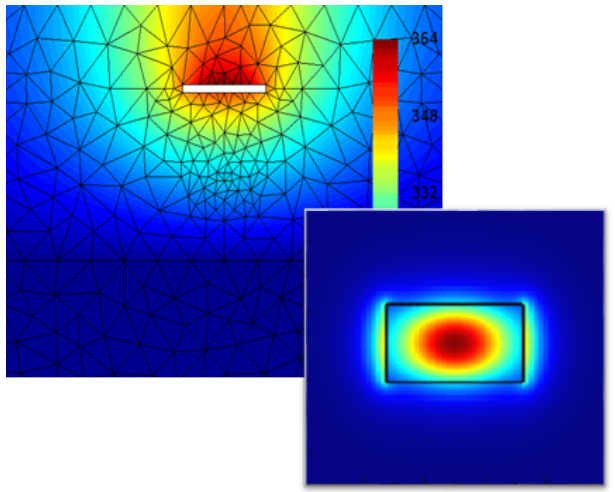
Optical



Electrical



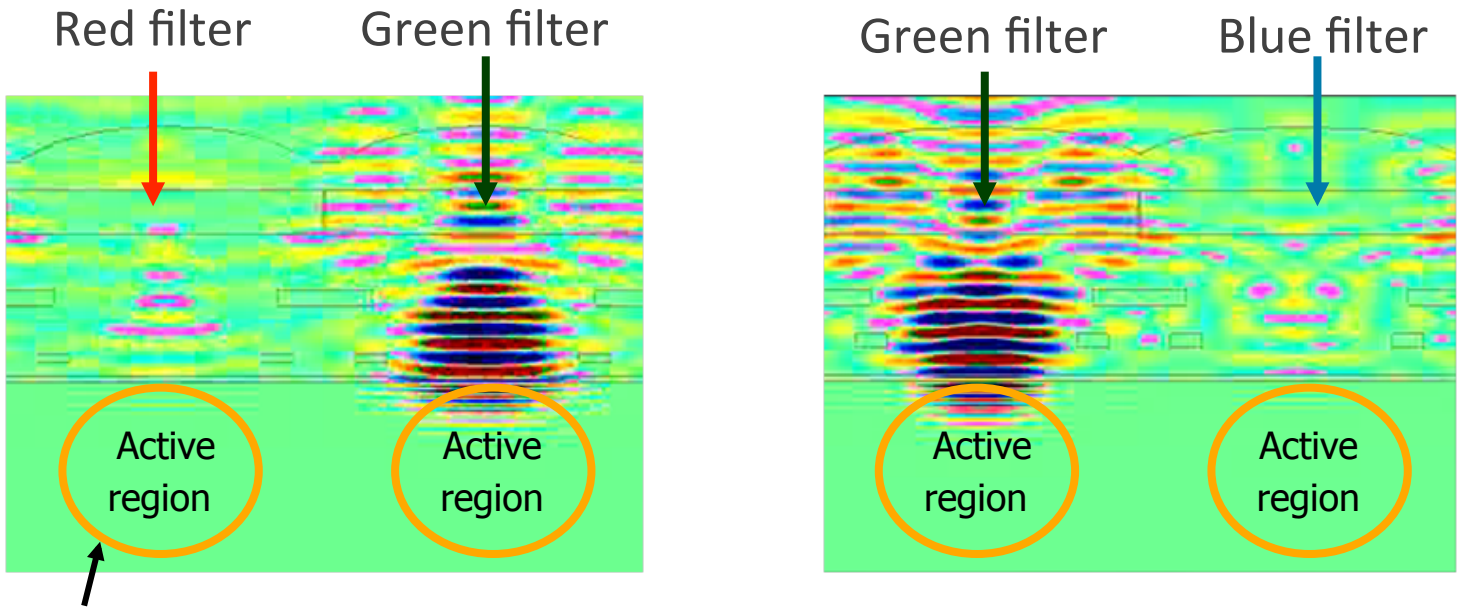
Thermal



Example: CMOS Image Sensors

Suppose the object to image is green

- Light arriving on the detector is green



Electrons are created as the light (photons) are absorbed.
The number of collected electrons in each pixel gives the pixel brightness and color for the final image

- Further electrical simulation with DEVICE

Challenges of component level simulations

The design and analysis of fundamental passive and active optoelectronic building blocks requires various solvers:

- Optical solvers to simulate the interaction of EM wave with material
  - Propagation properties, generation rates, absorption, …
- Electrical solvers to model charge transport
  - DC, large/small signal analysis, transient, …
- Thermal solvers to model heat transfer
  - Steady state and transient, self-heating, …
- Stress and strain
- Process simulation
  - Doping profiles, lithography correction, etch profile, sidewall angle, roughness

Extract accurate, and **calibrated** compact models from simulations and **measured** data for circuit simulation.

Integrated Photonics Designers

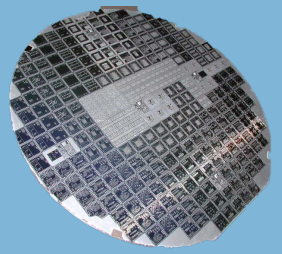
Today

Design

Component
Models/PDK
Circuit
Layout
Mask

<u>Technology Focus</u>
Many tools
Limited integration
PhD level expertise

Fabricate



Specialized Vendors
Custom Packaging
MPW & Low volume

Future

Design

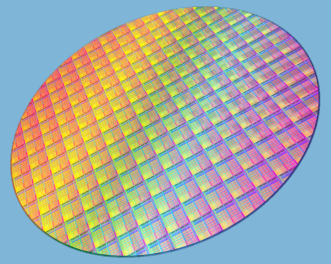
Component
Models/PDK

Circuit

Layout
Mask

<u>Application Focus</u>
EDA style tools
Tight integration
Design teams

Fabricate



Fabless, high volume
Custom, full wafer
Standard Packaging

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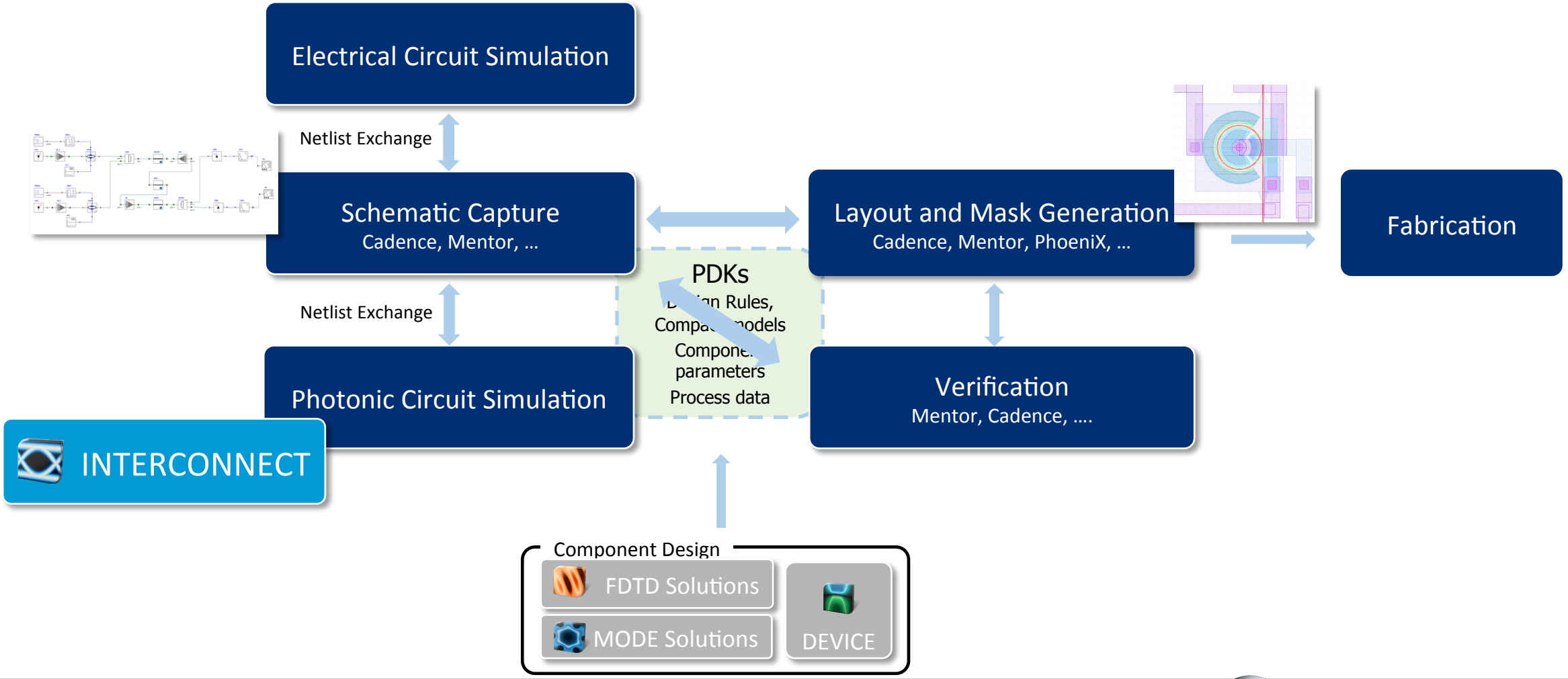
Design framework

PIC design is much more than just simulation. From and efficient, scalable EDA design frameworks to an EPDA framework:

- Design capture (layout-driven vs schematic driven)
  - Pre-layout simulation (only for SDL)
  - Curvilinear shapes!
- Use of pre-characterized building blocks (PDKs)
  - Including compact models for circuit simulation
- Hierarchical DRC & LVS
- Extraction and back-annotation for re-simulation
- Statistical Analysis / Yield
- Design for test, design for manufacturing, regression testing,…

EDA-style flow with a process design kit (PDK)



The photonic PDK

Technology Focus

Application Focus

Photonic PDK

Design Rules (for manufacturability, optical performance)

Mask layer and material information

Die (and package) templates

Library of validated components

Measured data

Compact models (CML)

Component & Model Library Design

Component Simulation
Optoelectronic solvers

Measured Results

Define Compact Model

System/Circuit Design & Fabrication

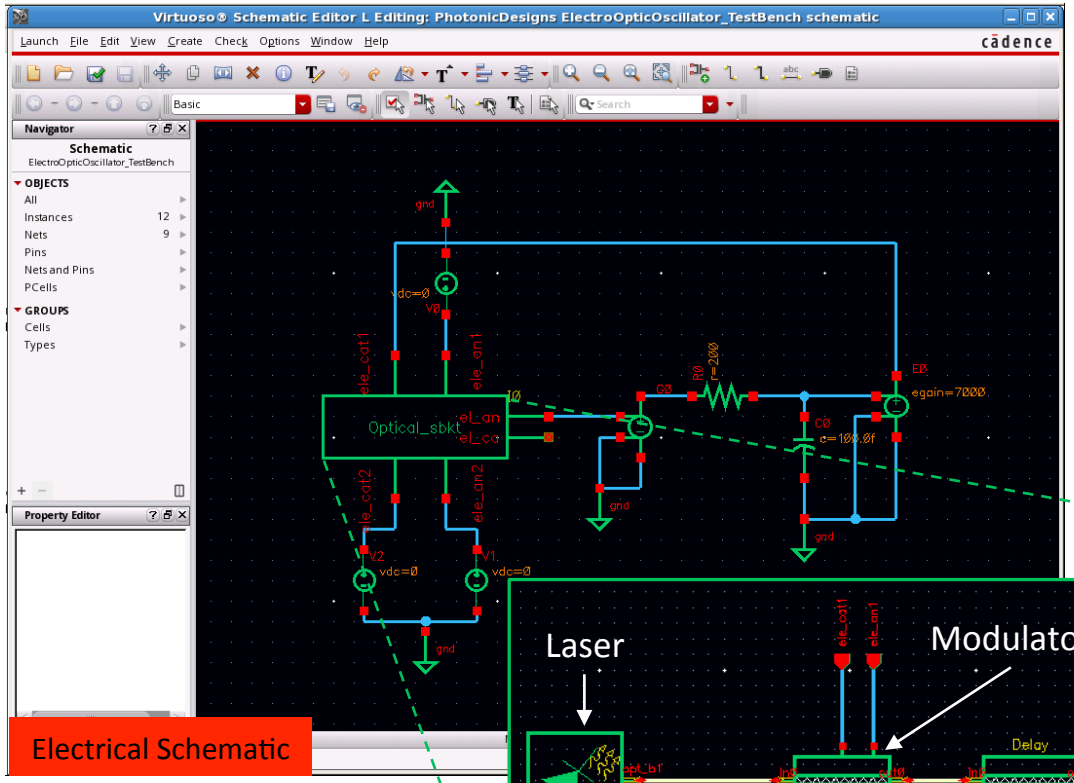
Circuit
Design, Layout, Verification

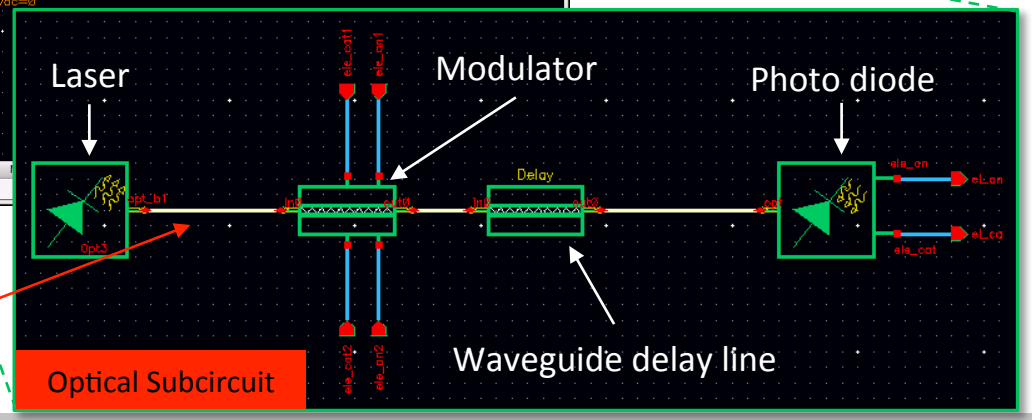
Fabrication and Test

[redacted]

Virtuoso driven design capture

Electro-optic oscillator

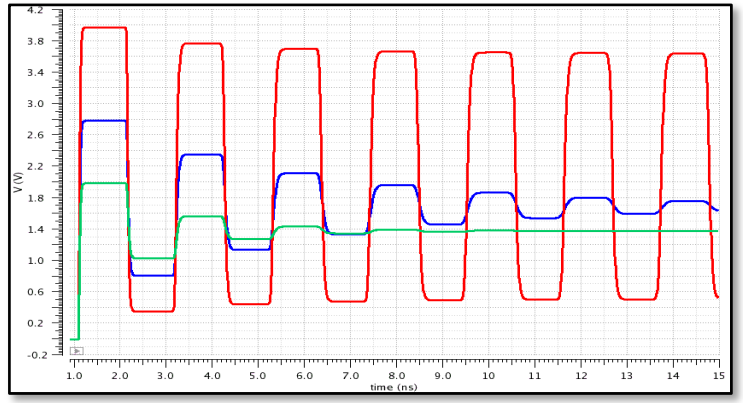




Optical signal type

Schematic driven layout

- Design capture – single golden schematic
- Dedicated optical circuit simulator (INTERCONNECT) and Spectre allow for co-simulation
- Electrical and optical components from generic PDK (availability of compact models
- Supports optical signal type (inclusive error checking)



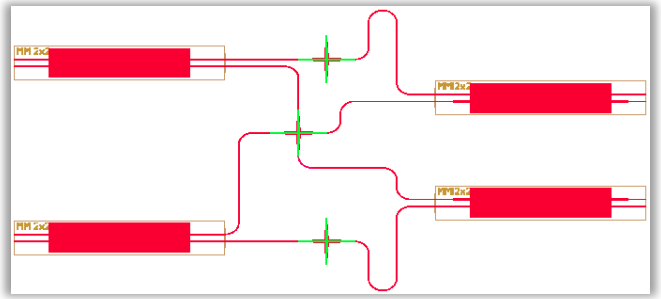
Photonic layout

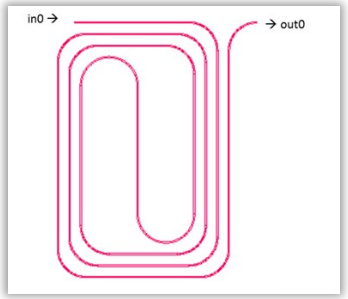
Curvilinear layout

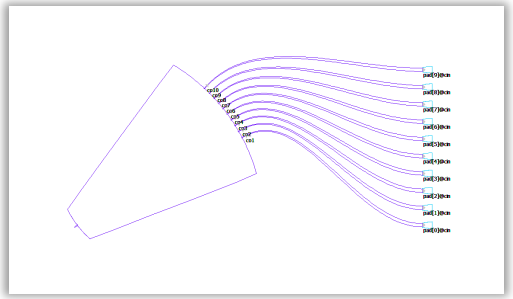
- non-Manhattan and requires all angle design features (location of ports, rotation, smooth curves, connectivity
- The provided library of validated components is not sufficient for a complete PIC design – waveguide routing

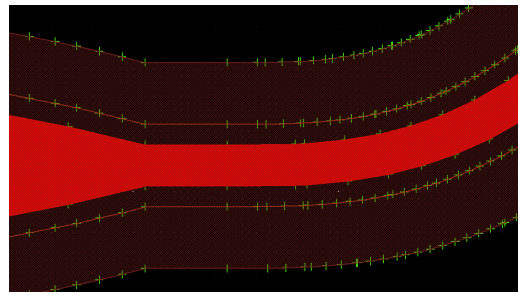
Traditionally IC design tools are missing generic photonic elements and components.

- Optimized discretization









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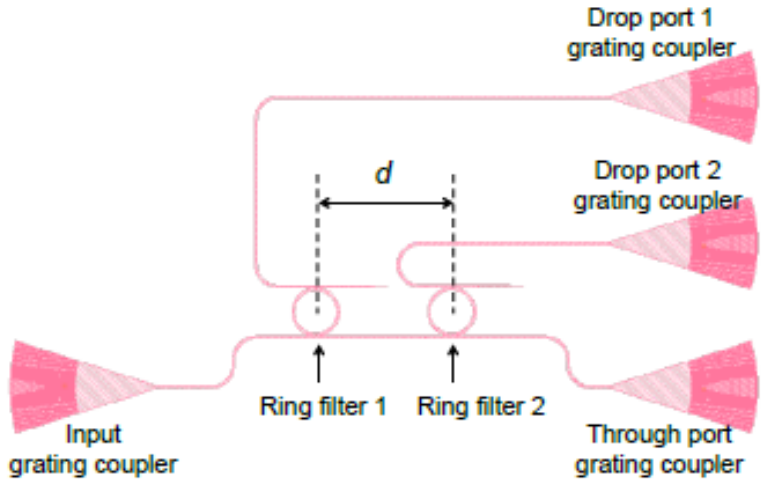
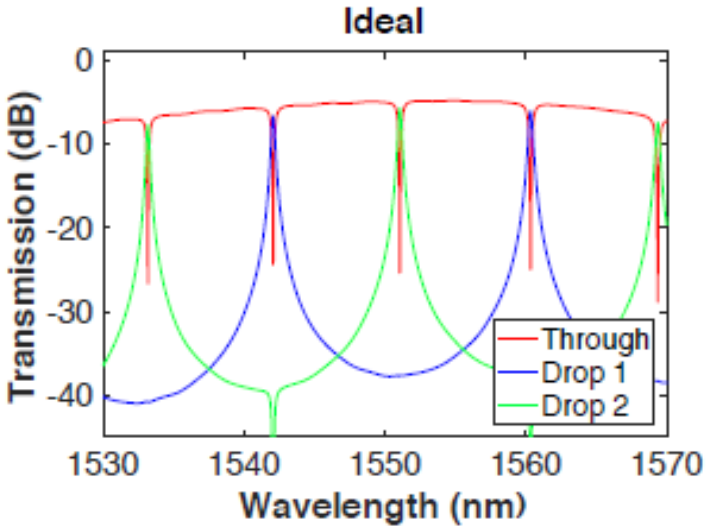
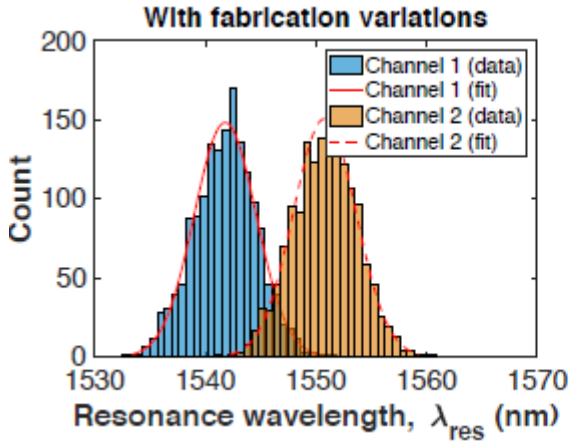
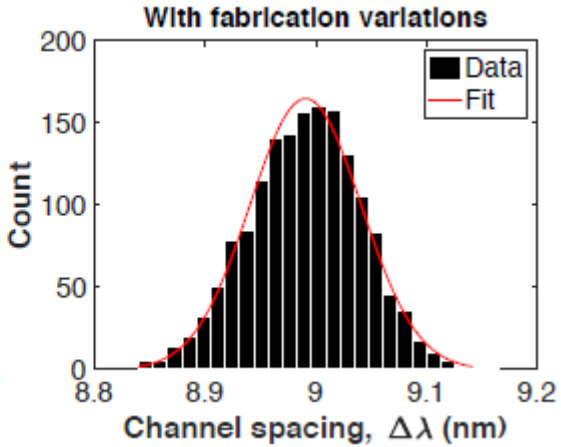
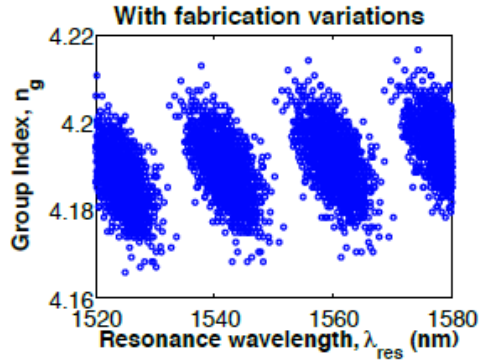
Statistical analysis – layout aware





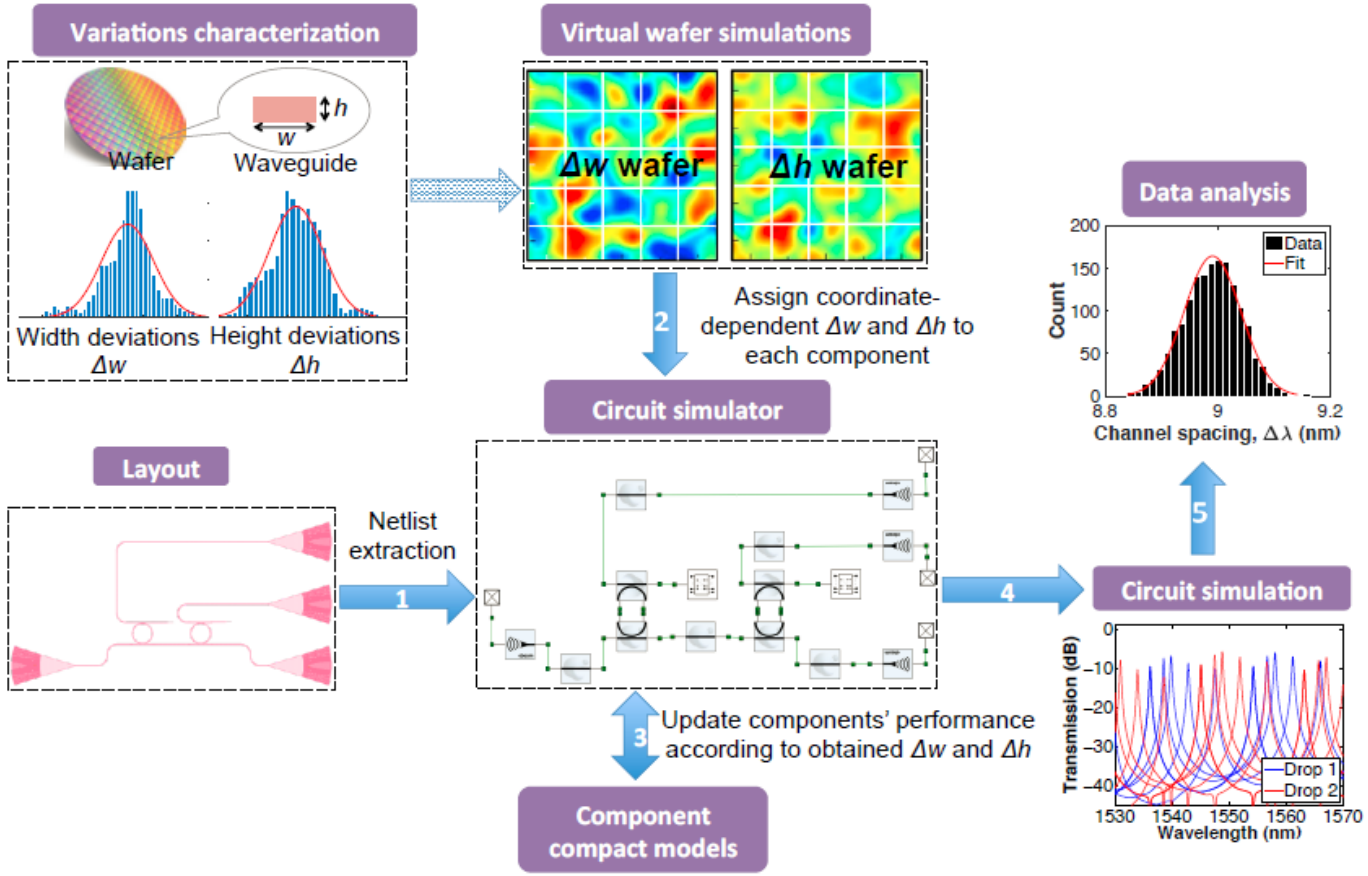






Z. Lu, J. Jhoja, J. Klein, X. Wang, A. Liu, J. Flueckiger, J. Pond, and L. Chrostowski, "Performance prediction for silicon photonics integrated circuits with layout-dependent correlated manufacturing variability", submitted, 22 pp. (2017).

Design for Manufacturability (DFM)



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Conclusion

There is clear advantage to combine the efforts of EDA and PDA to deliver a complete and efficient solution for Integrated Photonics

- 3 decades of CMOS EDA tools + over a decade of optical component design software development

But Photonics is not the same as electronics

- New signal types
  - Allows segregation (and automation) of electrical vs. optical (V,I vs TE and TM,…)
- Dealing with curvilinear shapes
  - Including discretization challenges
- A waveguide is usually a complex 3D structure vs. a wire in electronics
  - Typically a waveguide will be modeled as a device, not a piece of “interconnect”
- Optical connectivity is NOT the same as electrical connectivity…
  - 2 electrical signals crossing make a short... 2 optical crossing make ... A crossing...

Foundries are an integral part of the solution and need to upgrade their “Photonics PDK” to a similar level of completeness and features to what is the standard in electronics

Dr. Jonas Flueckiger

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