

Mask Layout Challenges for Silicon Photonics

Session IV: Design Automation and Methodologies

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DESIGN, AUTOMATION & TEST IN EUROPEAN CONFERENCE
OPTICAL/PHOTONIC INTERCONNECTS FOR COMPUTING SYSTEMS
MARCH 31ST 2017



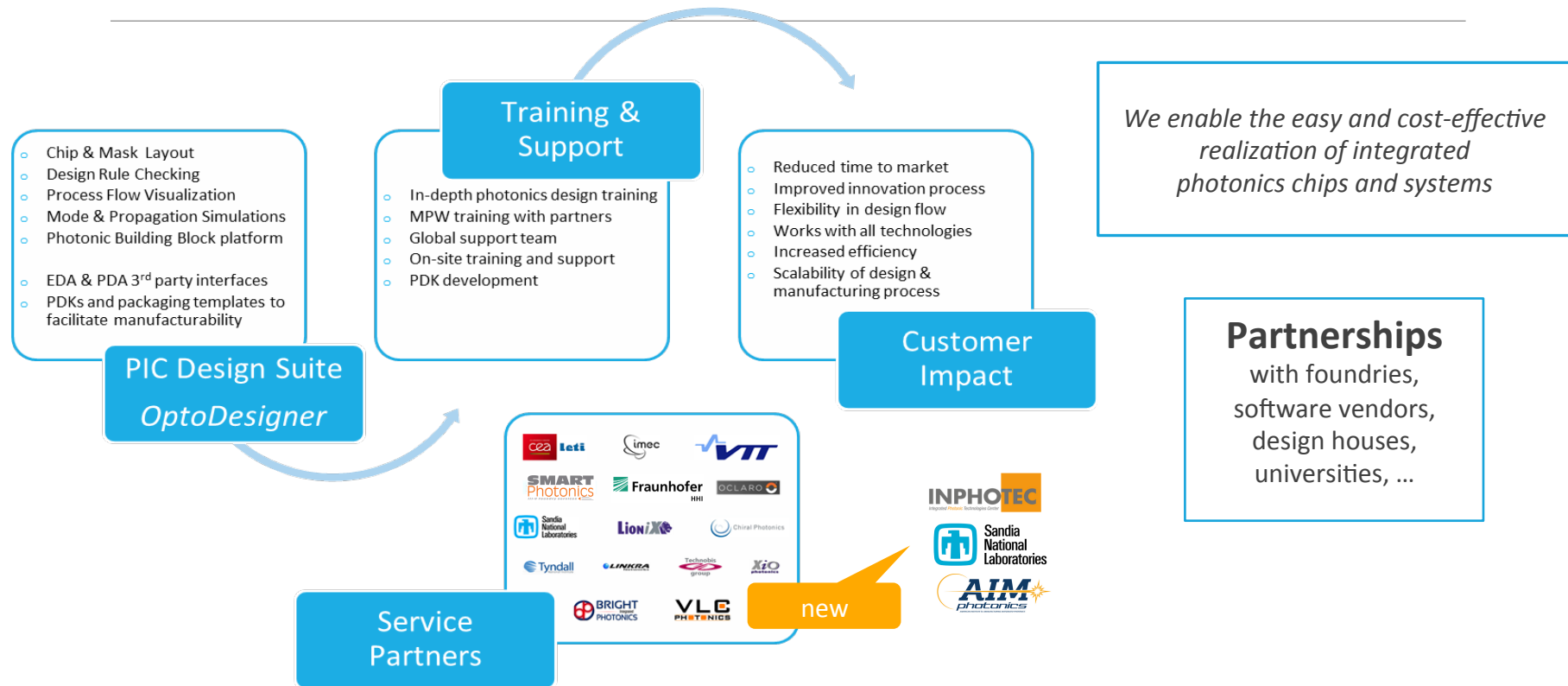


Outline

- Phoenix Software
- Discretization
- Design Intent
- Design Rule Checks
- PDA – EDA Integration

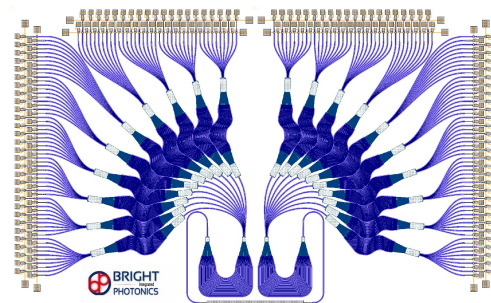
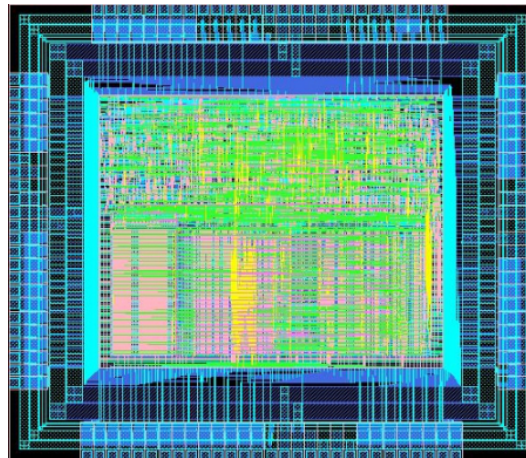


Phoenix Software





EDA versus PDA

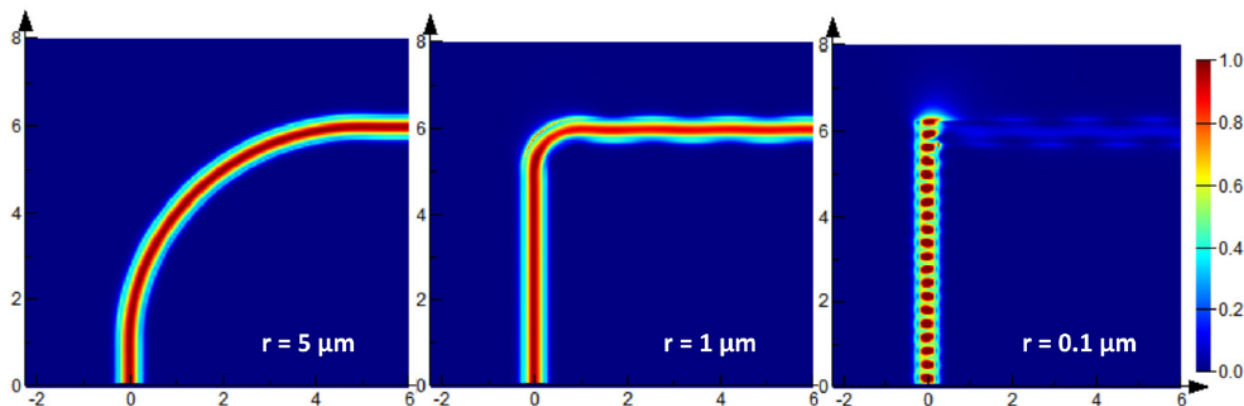


Manhattan versus “Erice” patterns

Manhattan versus curvilinear patterns



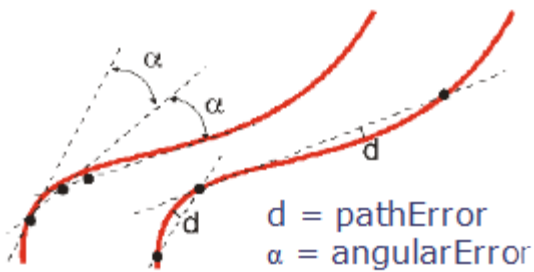
Non-Manhattan / curvilinear design



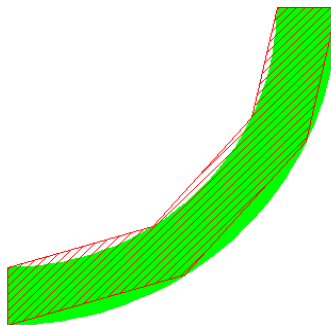
Waveguide routing requires a curved format instead of rectilinear/Manhattan-style routing to ensure that light stays in a waveguide. Simulation of a curved waveguide with different radii. Image courtesy of Lumerical Solutions, Inc.



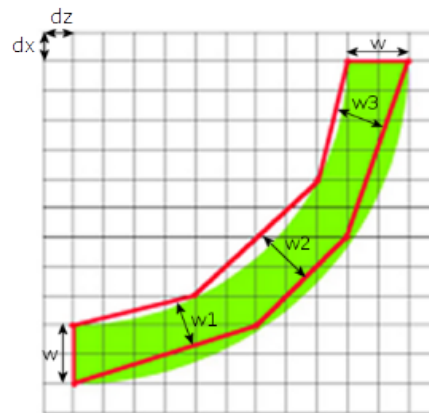
Curve Discretization



From ideal (analytical) curve



To a discretized polygon



Mapped onto GDS grid

Need for tools to translate ideal curves (Design Intent) into discretized polygons, controlling phase relations

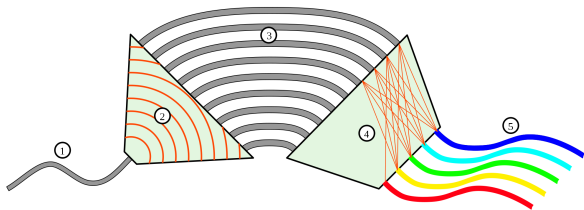


Mask layout impacts:

- **Losses**
 - Obtaining smooth curves and side-walls
 - Mask orientation of waveguides (due to writing direction of mask)
- **Back Reflection**
 - Smooth curves and side-walls
 - Limits on angle changes (radius)
- **Phase Changes**
 - Width (and height) control of waveguides (1 nm -> 125 GHz)
 - Changes in optical path-length



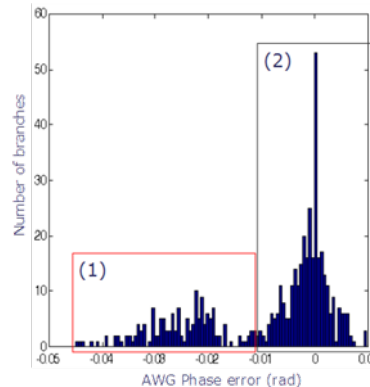
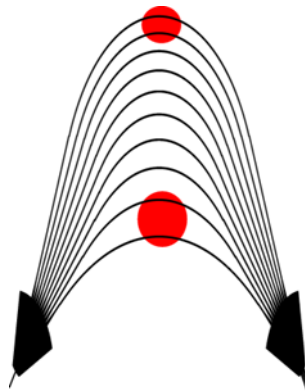
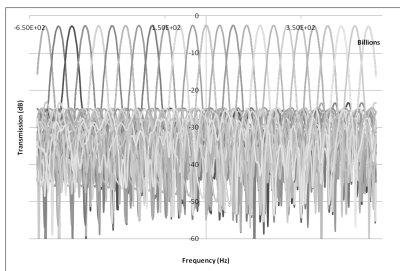
Impact of optical path-length



Example: Arrayed Waveguide Grating

It is in fact a (de)multiplexer for light. Different colors (data streams) are filtered into different waveguides.

The geometry determines the optical performance, and can be calculated through simulations from specifications like bandwidth, number of output channels, channel spacing, etc.



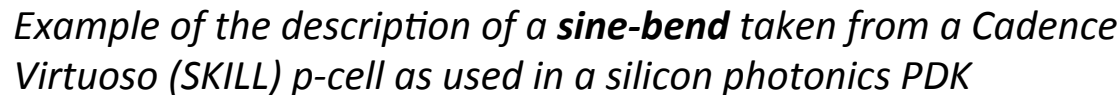
Phase errors resulting from:

- (1) errors due to mismatches in the optical path lengths in the branches in the array
- (2) stochastic errors from fabrication variations



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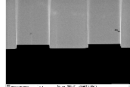
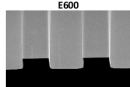


Same applies to Mentor Graphics AMPLE or generic languages like Matlab, Python, ...



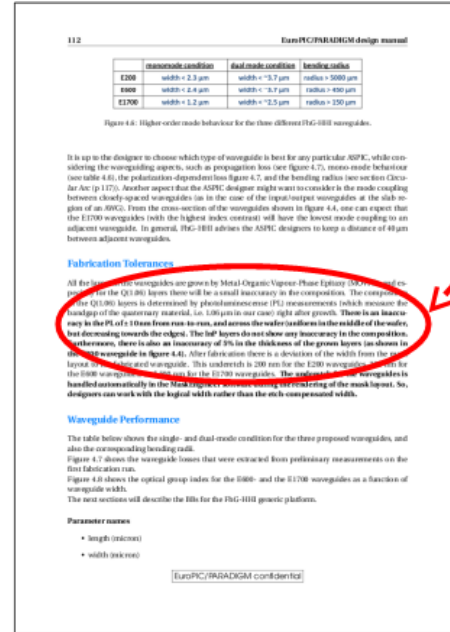
Design for Manufacturing

- Fabrication -> cross-section -> performance

Waveguide Performance		Photonic Components			
	single-mode	dual-mode	bends	prop. loss	
E200		$w < 2.3 \mu\text{m}$	$w < 3.7 \mu\text{m}$	$R > 5000 \mu\text{m}$	0.5-1.5 dB/cm
E600		$w < 2.4 \mu\text{m}$	$w < 3.7 \mu\text{m}$	$R = 500 \mu\text{m}$	0.5-1.5 dB/cm
E1700		$w < 1.2 \mu\text{m}$	$w < 2.5 \mu\text{m}$	$R = 150 \mu\text{m}$	0.5-1.5 dB/cm

Fraunhofer
Heinrich Hertz Institute

europic



After fabrication there is a deviation of the width from the mask layout to the fabricated waveguide. This underetch is 200 nm for the E200 waveguides, 300 nm for the E600 waveguides, and 500 nm for the E1700 waveguides.



From Design Intent to GDSII

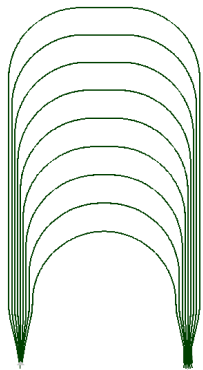
- Fabrication → cross-section → performance



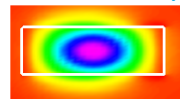
Designer:



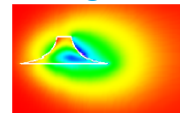
Process:



Ideal/theory



Not guided





From Design Intent to GDSII

- Fabrication → cross-section → performance



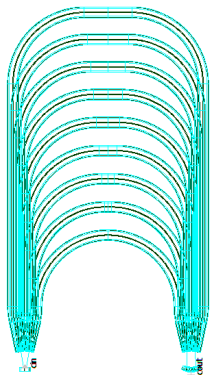
Designer:



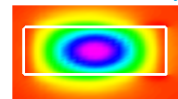
Process:



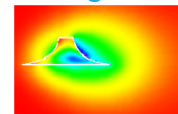
OptoDesigner: mask widening to compensate underetch



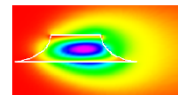
Ideal/theory



Not guided

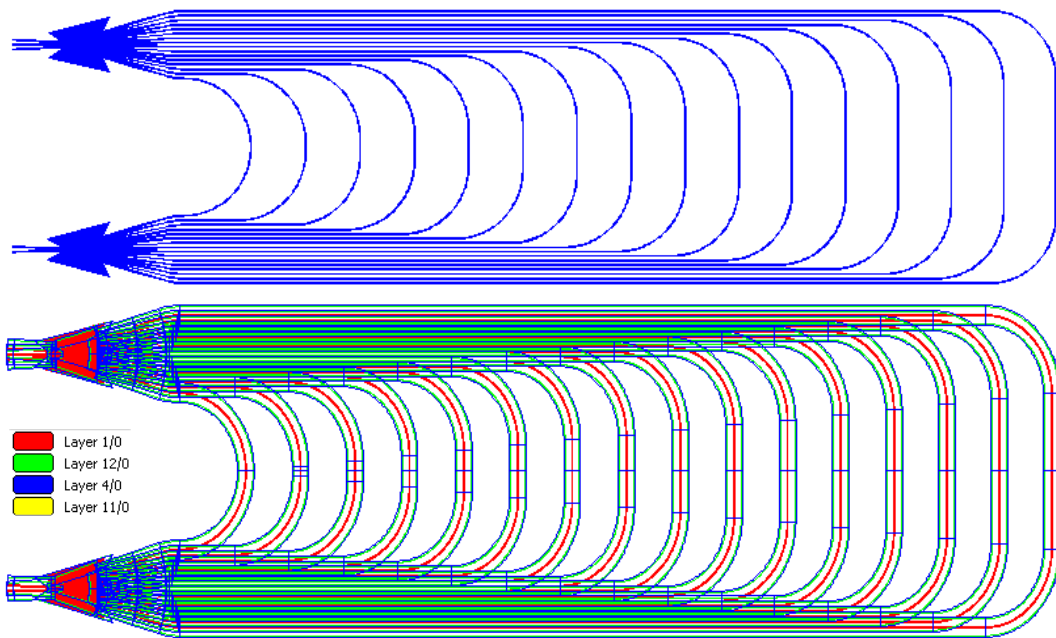


Guided





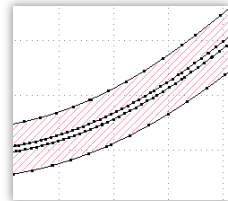
Real life example for Design Intent



AWG example: from intended waveguide or “logical” design into actual mask or “GDS” design to fabricate with the correct waveguide dimensions (cross section)

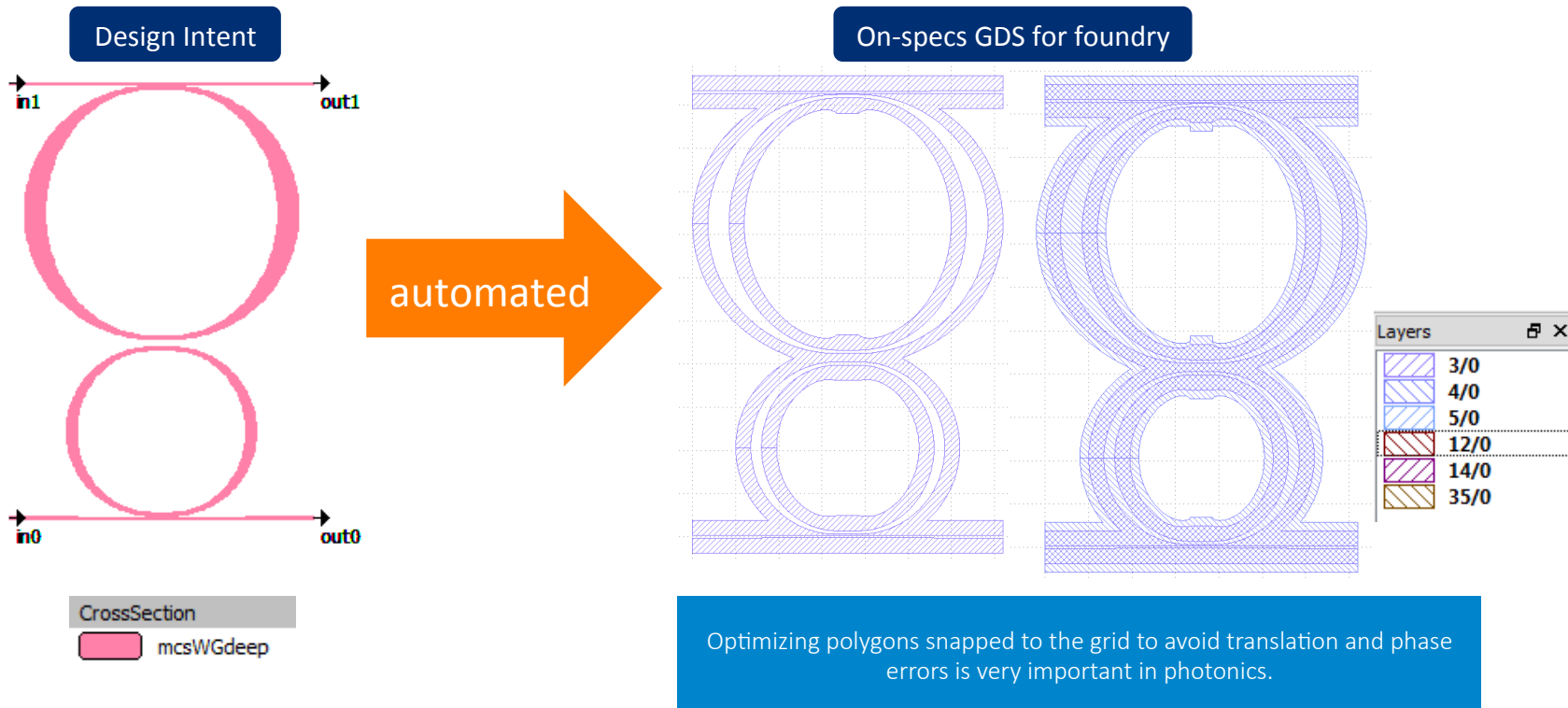
From design intent to final mask layout:

- Calculating the required shapes, given the design intent and the fabrication information
- Turning these into polygons, given a maximum allowed path error
- Placing the polygons into the required mask layers, including sizing, inversion, boolean operations, etc.
- Checking design rules
- Exporting mask (GDS2) files





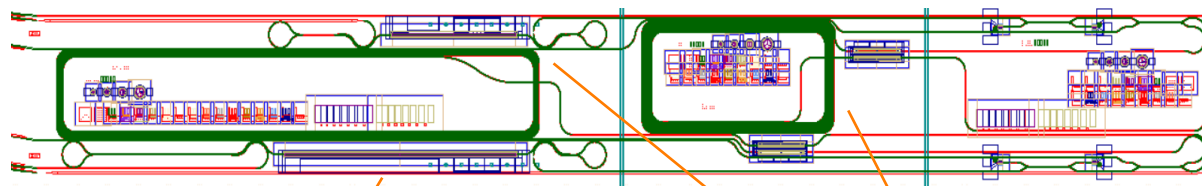
Using Design Intent in the UCSB PDK





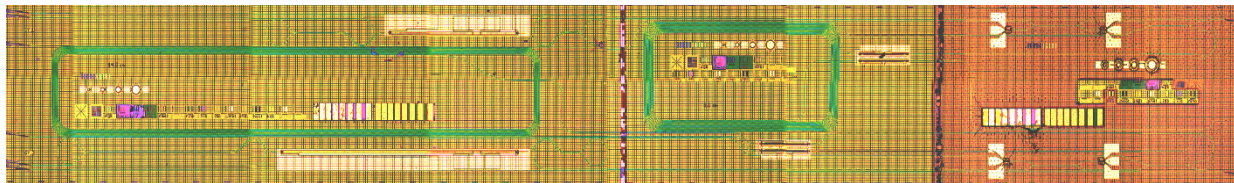
Heterogeneous SOI & III-V Integration – PDK Available

Optical gyroscope

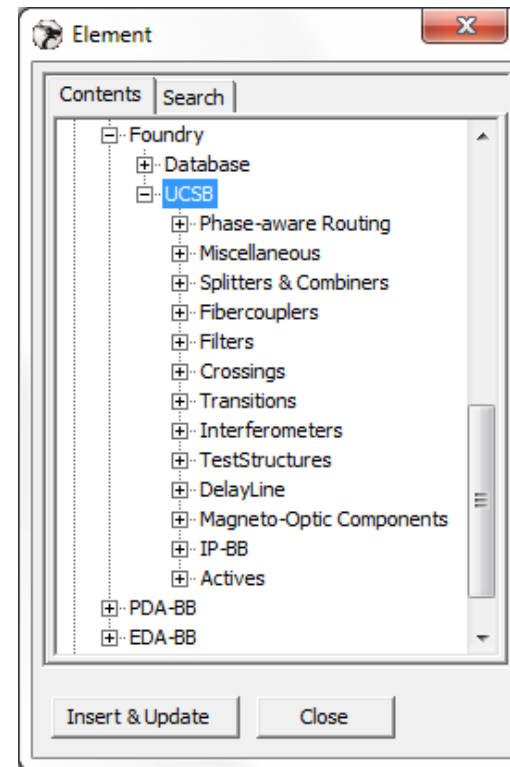


Widely tunable laser (III-V) enables line measurement of phase change

Two phase matched delaylines (SOI) measure rotation angle of gyroscope



Minh A. Tran et al., "Integrated optical driver for interferometric optical gyroscopes,"
Opt. Express 25, 3826-3840 (2017)





UCSB Heterogeneous SOI & III-V Integration – PDK available

InGaAs PIN PD



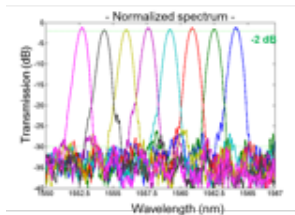
AlGaInAs DFB



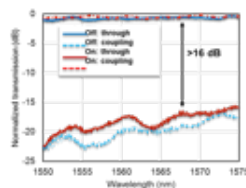
AlGaInAs EAM



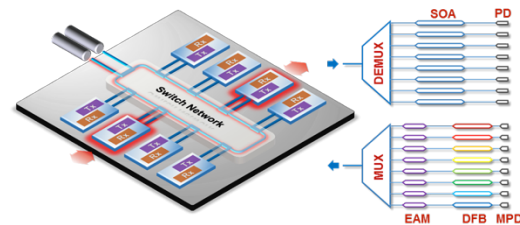
1×8 (De)Mux



Broadband MZI switch array



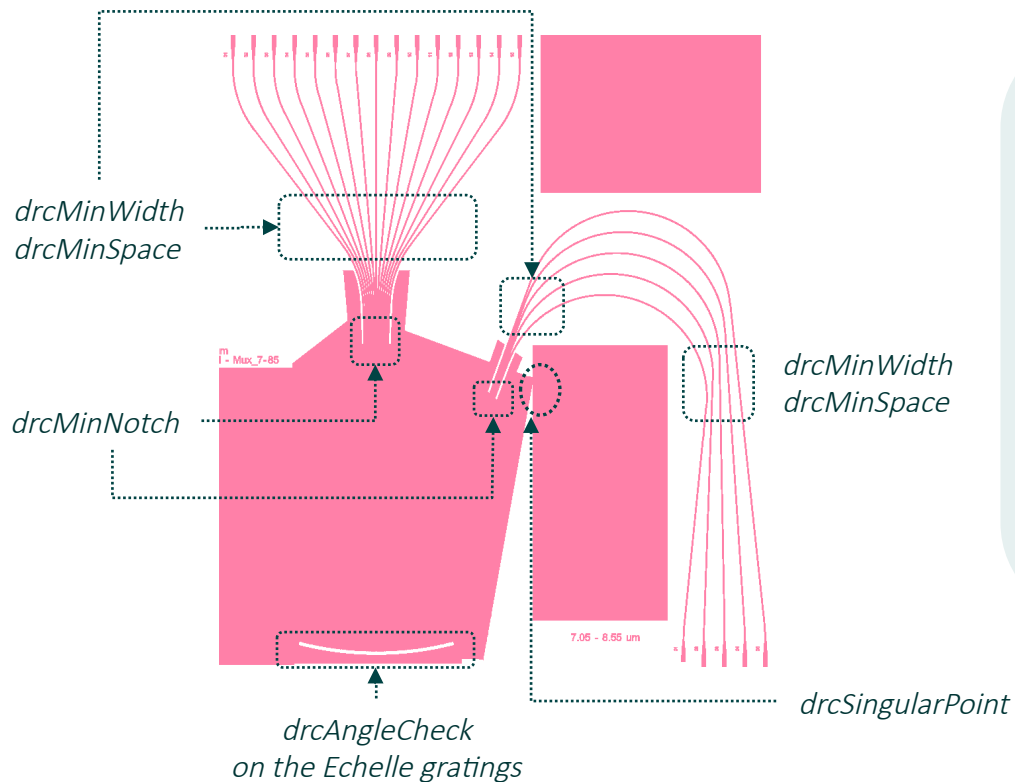
More than 400
Photonic Building
Blocks in one PIC! 😊



8 × 8 × 40 Gbps fully integrated silicon photonic
network on chip, Zhang et al., 2334-2536/16/070785-02 Journal, 2016 Optical Society of America



DRC Design Rule Checks



Fabrication errors can lead to high costs and unwanted delays, however, they can be prevented by using verification and Design Rule Checks (DRC).

Both for academic research as well as commercial product development, it is a key step in the whole design flow from initial concept to manufacturable mask layout.



DRC example Notch Check



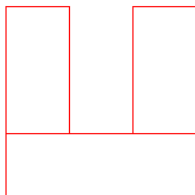
Notch too small



Error! Fail on: Too small Notch
too small notch

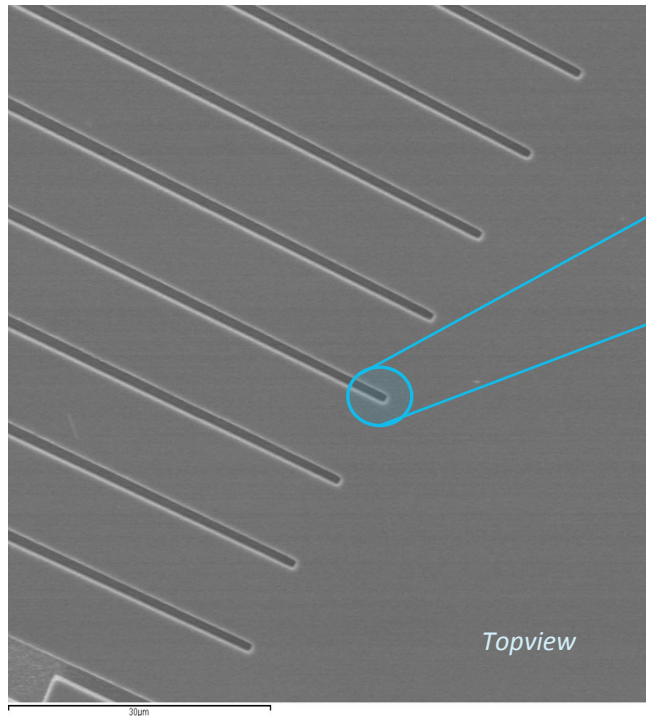


Notch large enough

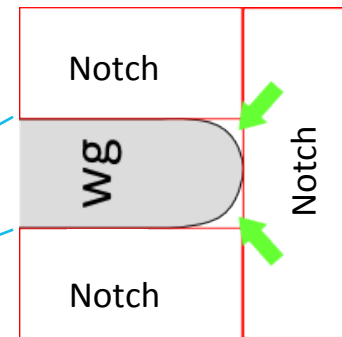


large notch

Rounding of a square feature (the end of the waveguide) as a result of the distance to surrounding features (or non etched surfaces)



Topview

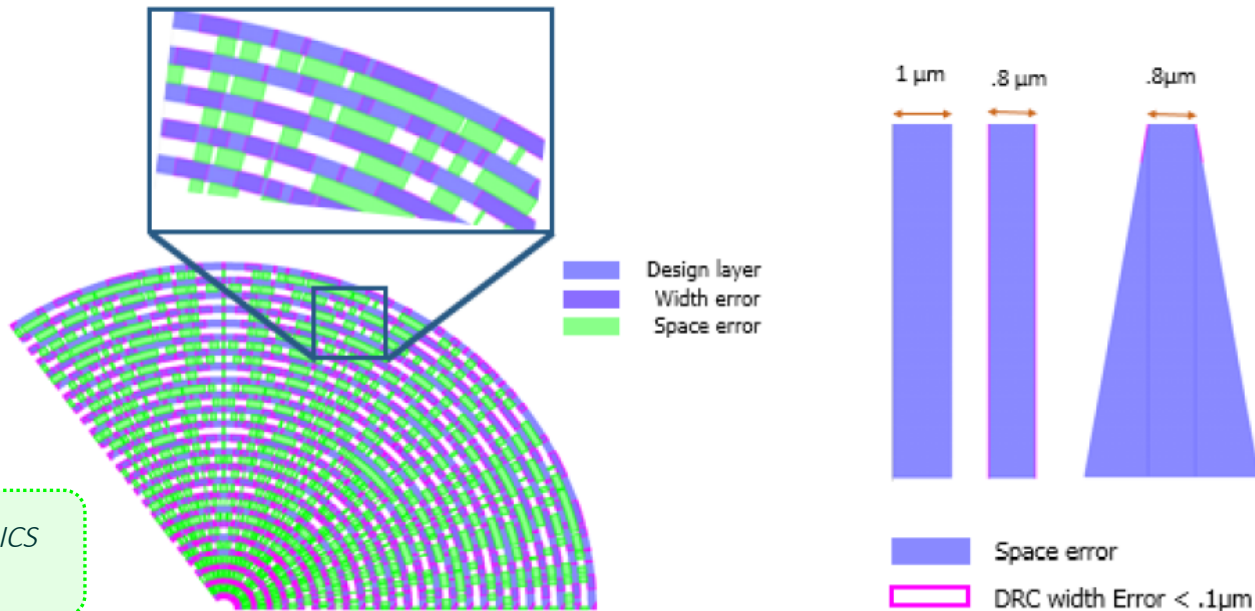




Challenges for Calibre

Silicon photonics components are usually formed by curvilinear geometries (non-Manhattan shapes). Traditional IC DRC tools are incompatible with these geometries, resulting in false errors reported during the physical verification phase.

MOHANED ELSHAWY, MENTOR GRAPHICS
MGC 06-16 TECH14370

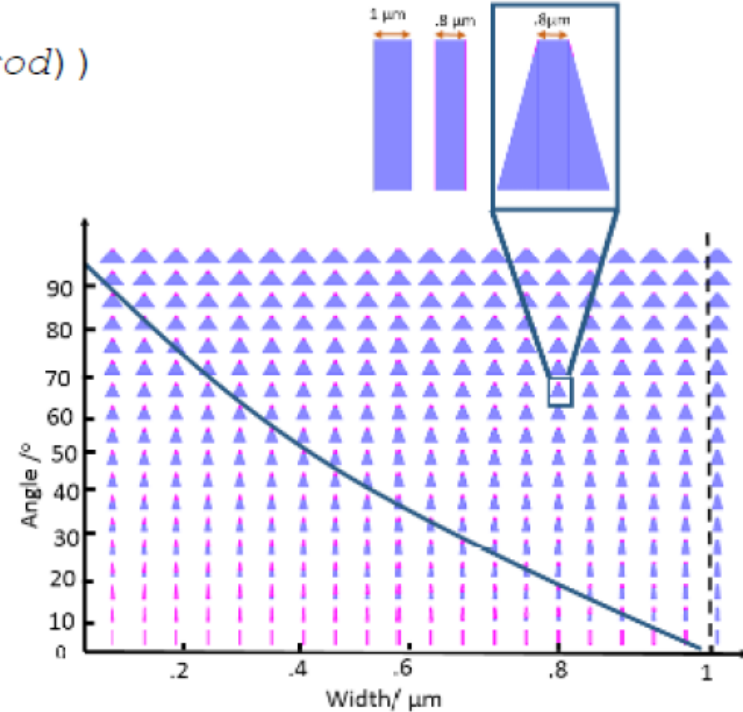
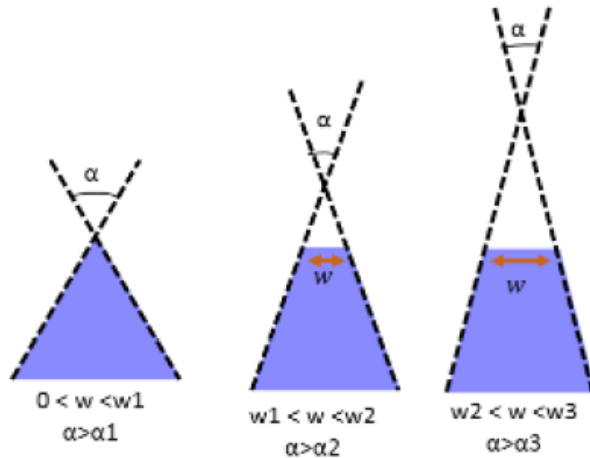




Conditional and multidimensional DRC

$\alpha = \text{Angle}(\text{rod})$, $\alpha_c = f(\text{Width}(\text{rod}))$

Then, $\text{Thin_rod} = \alpha / \alpha_c > 1$

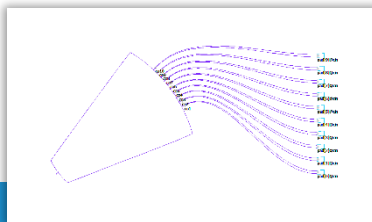
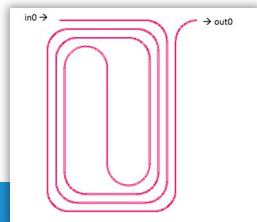
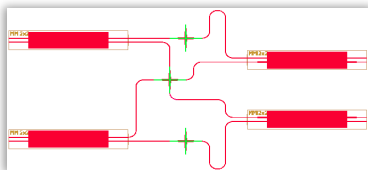




Situation today

- Challenges we see customers and foundries running into:
 - Increasing complexity of PIC designs
 - Significant waveguide routing challenges
 - Limited circuit simulation capabilities with validated models
 - Design verification: design rule checking and layout vs schematic
 - Co-design of electronics and photonics

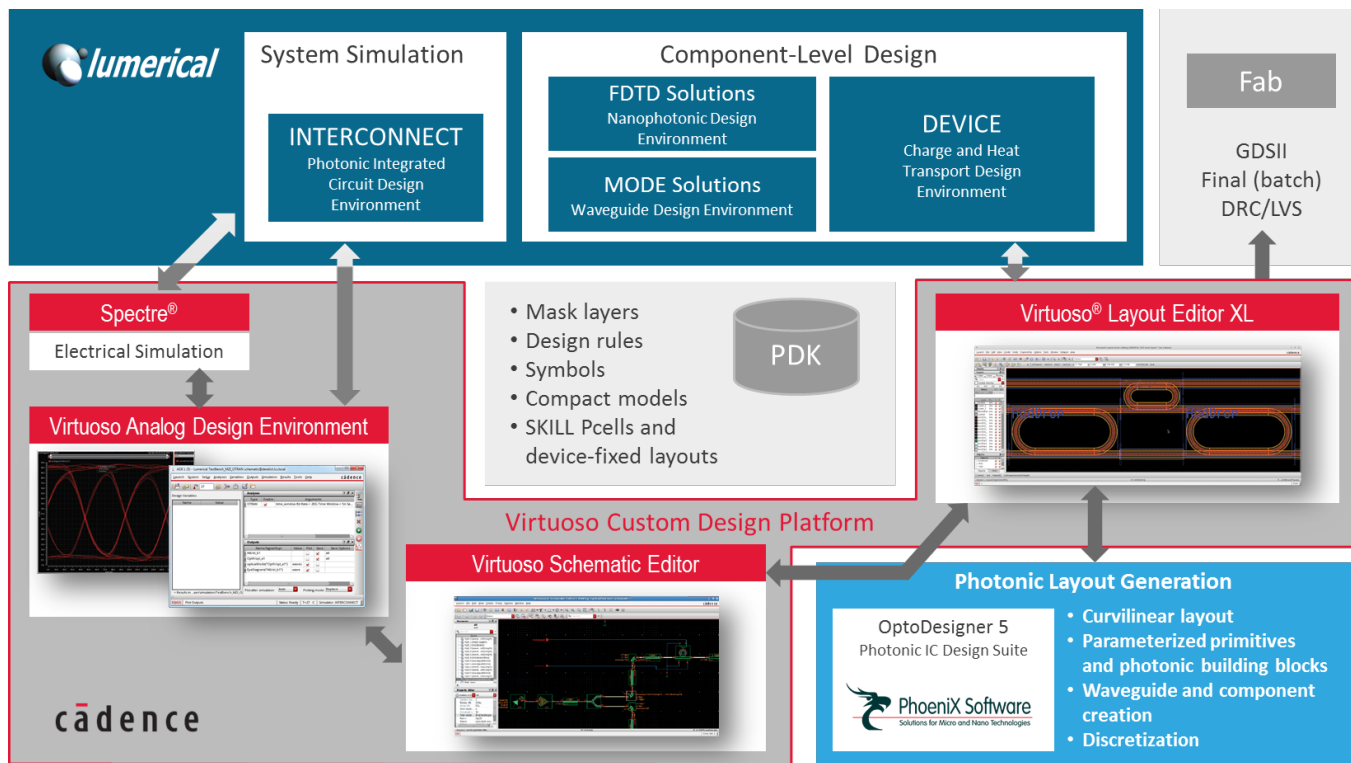
To support the industry in the transition from research to commercial product development, we need integrated design flows supporting a design for manufacturability design strategy, making use of strengths of both PDA as well as EDA tools





EDA – PDA integration

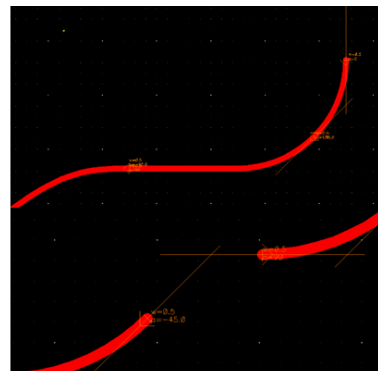
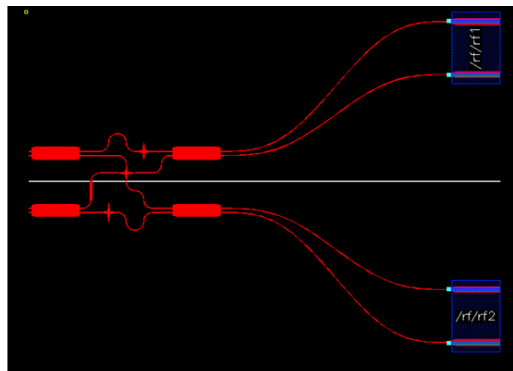
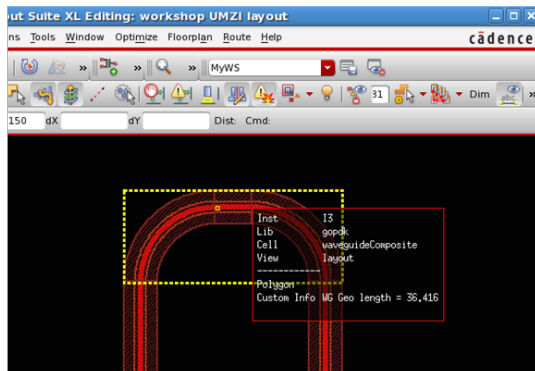
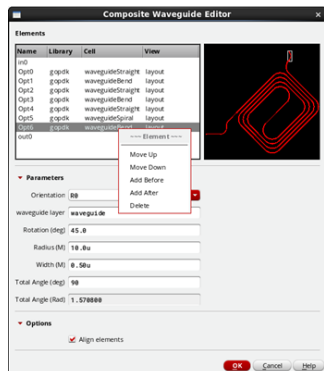
Example of 3-party collaboration



- Collaboration announced in December 2015
- Schematic Driven Layout flow, centered around a PDK approach



Phoenix Software's Virtuoso integration with PDA-Link access point into all Phoenix Software's PIC design routines

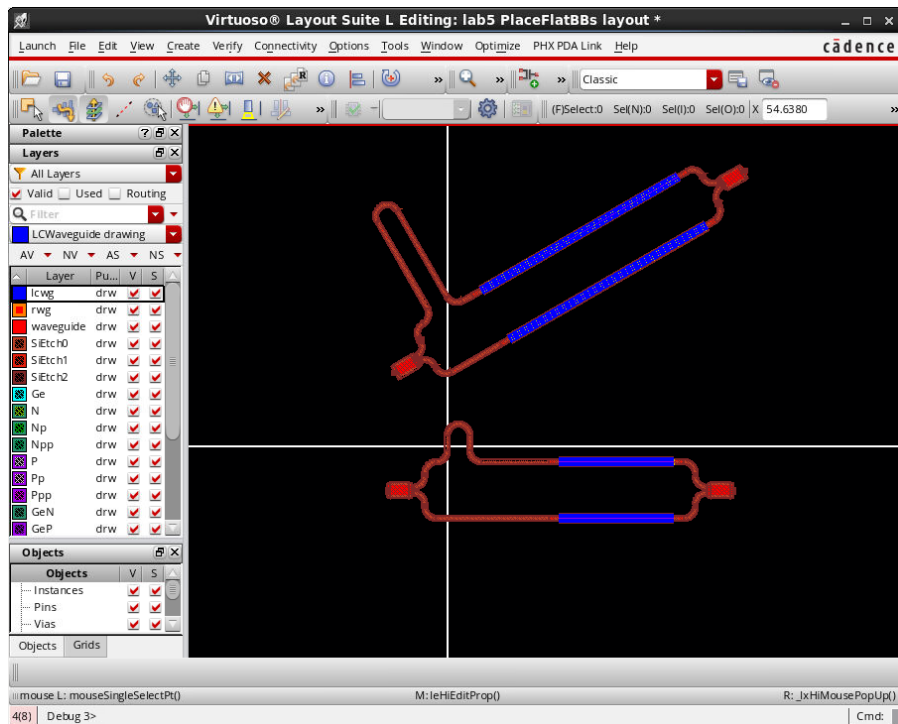


All photonics parts are provided by Phoenix Software technology

Overcoming the grid-based “Manhattan” design limitations in traditional IC design tools



All angle in Virtuoso



- Fully Parameterized
 - Path Length Difference
 - Modulator Length
 - ...
- All Angle



Summary

- Discretization impacts device performance
 - Good algorithms required
- Technology dependencies can create complex tasks
 - Need good PDKs
 - Hybrid PDK design environment
- Design rule checks of EDA are not sufficient
- Need integration between EDA and PDA tools

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