An Optical Parallel Adder Towards Light Speed Data Processing

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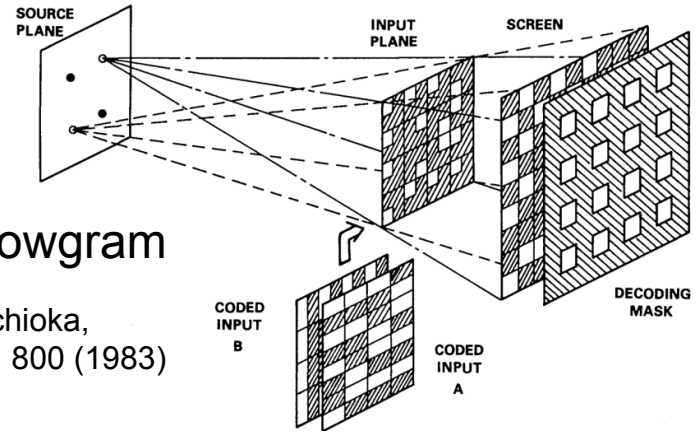
History of Optical Computing

■Opt. computers

Intensively studied in 1970's, but CMOS computers are much more superior to the optical computers

Based on optical filters

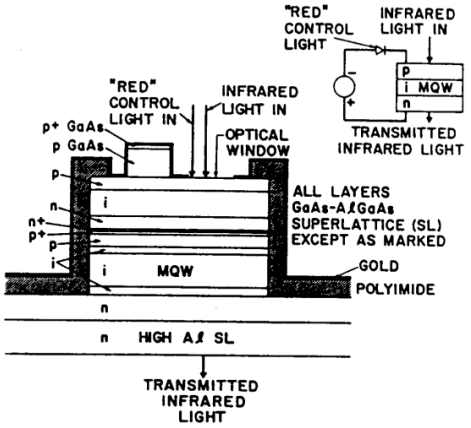


Shadowgram

Tanida, Ichioka,
JOSA 73, 800 (1983)

Hard to miniaturize

Based on optical transistors



SEED
(Bell Labs.)

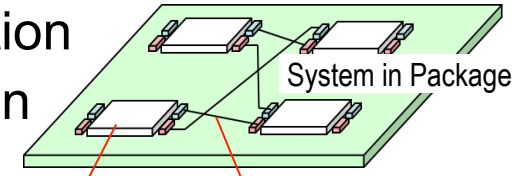
Miller et al.
OQE 22, S61 (1990)

Lower performance than CMOS

■Opt. interconnect

In 2000's, optical interconnects got into computers
Intel, IBM, PETRA lead investigation (Si photonics)

Electronics → computation
Optics → communication



CPU Optical interconnect

Only for interconnect ?

Beyond Optical Communication

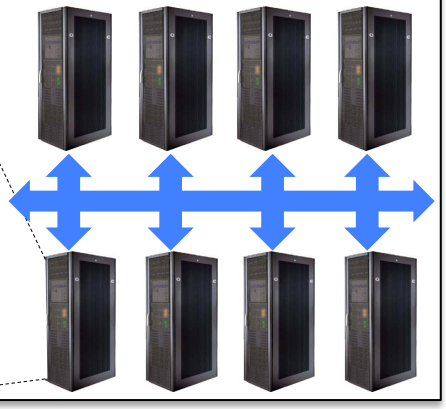
Chip-to-chip interconnect

DRAM

CPU/GPU

Intra-rack optical interconnect

Inter-rack optical interconnect



Network-on-Chip

NoC

Optical accelerator

Optical accelerator

Optical accelerator

CMOS CPU

Optical accelerator

Optical accelerator

Our focus in this talk

Optical Interface

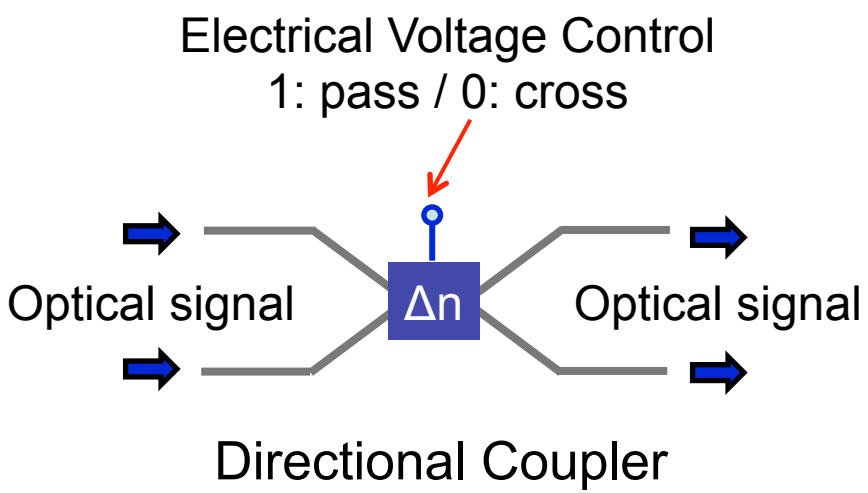
RAM

Optical data-path

Functional Unit

Functional Unit

Photonic Chrystal Optical Pass Gate



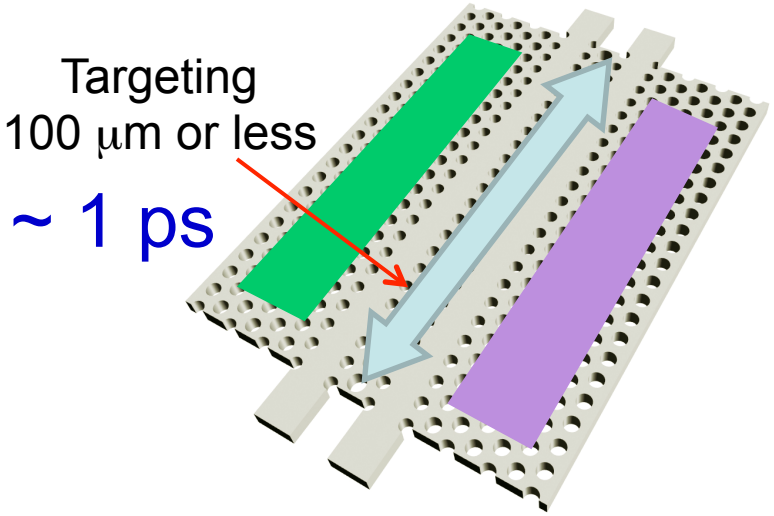
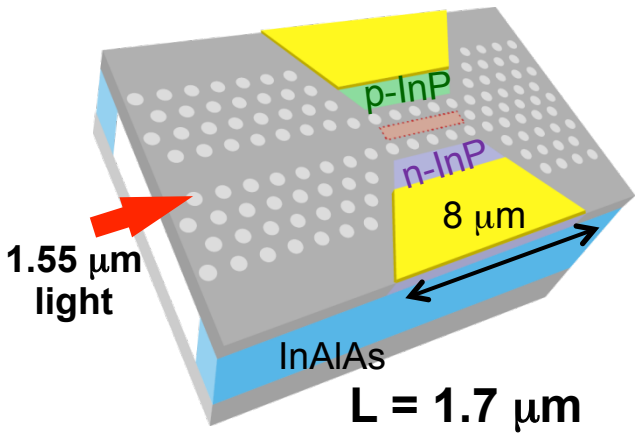
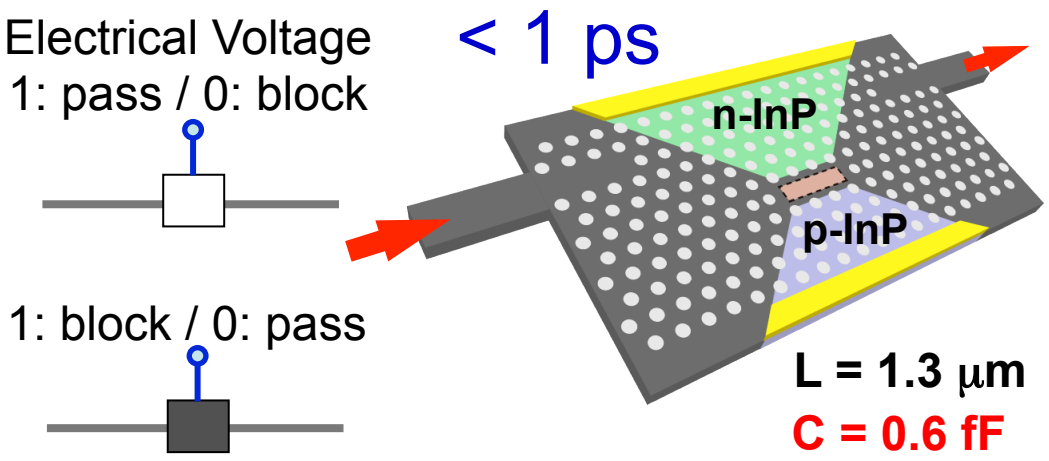


Photo Detector

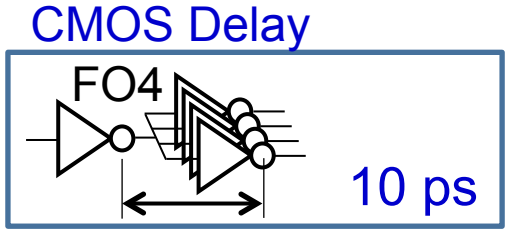




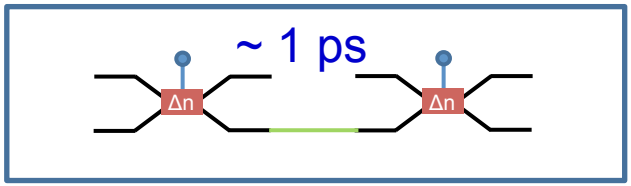
Why Optical PG for Data Path?

- Good at data path operation

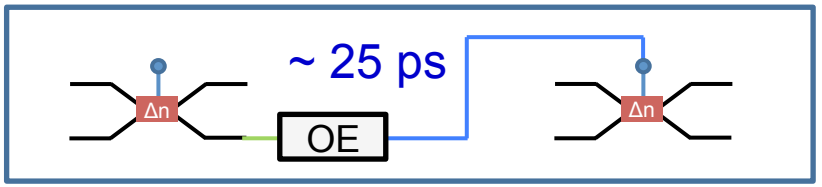
  ✓ Light speed operation



Good at serial connection (light speed)

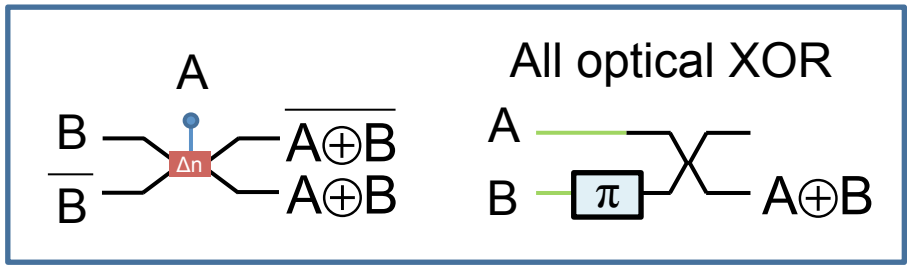


NOT good at cascade connection (OE & switching delay involved)

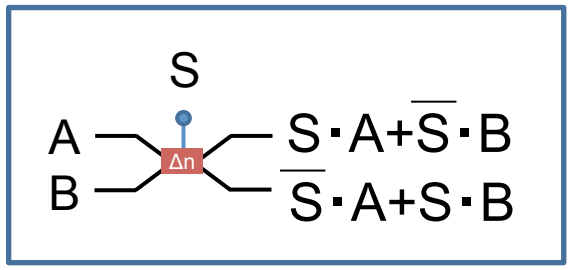


  ✓ Good at pass/cross propagations (XOR and MUX)

XOR

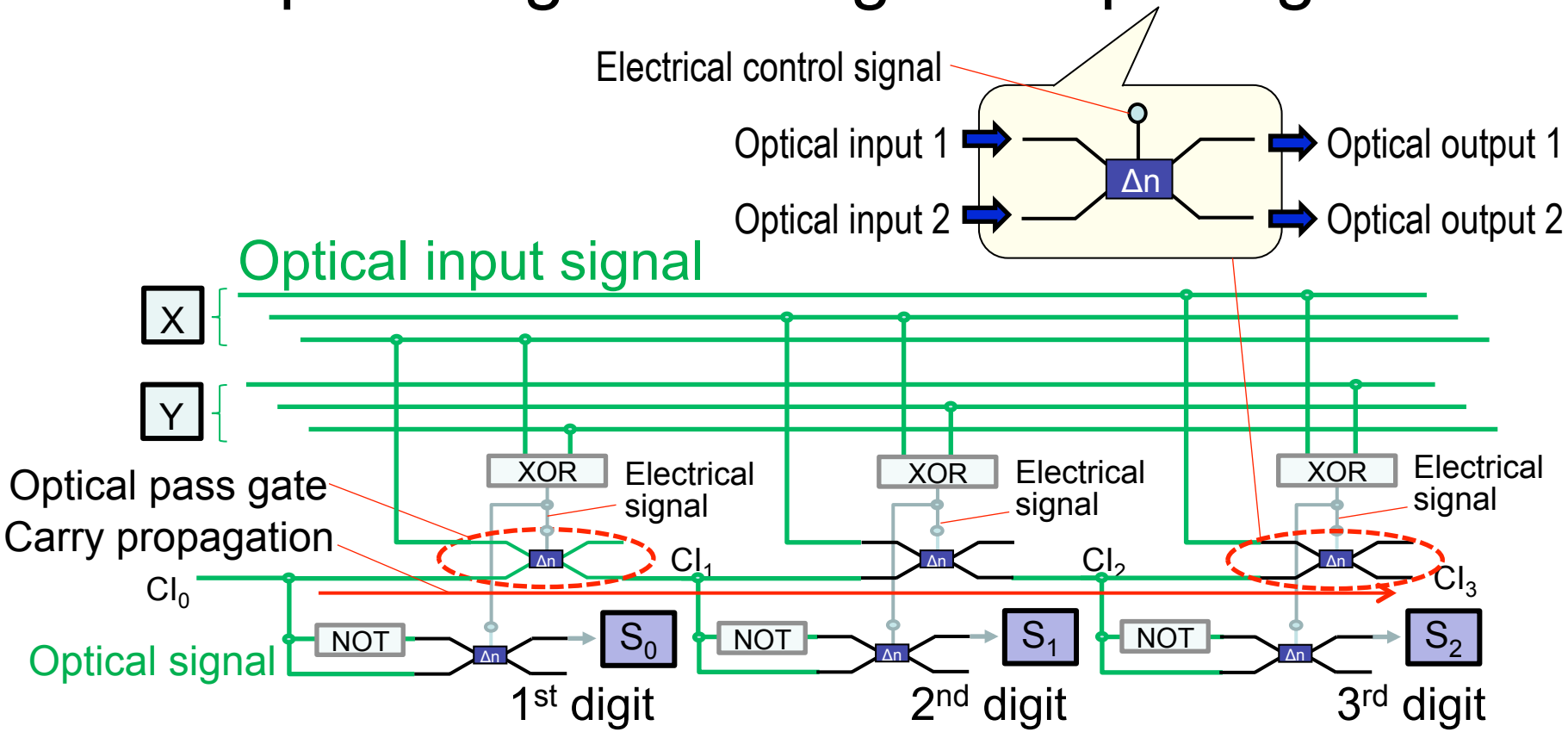


MUX



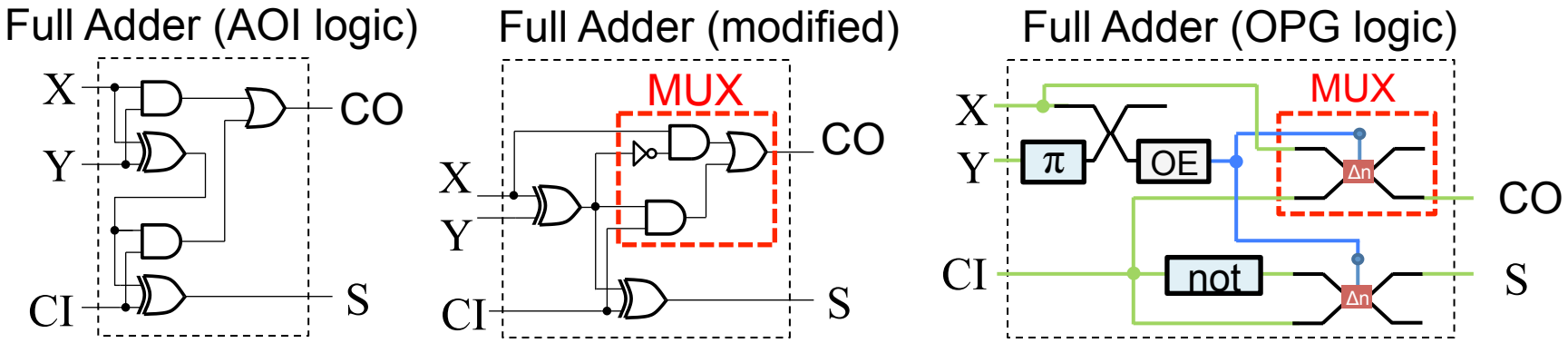
Optical Parallel Adder Example

- Computation can be done by just passing the optical signal through the “pass gates”



Arithmetic Operation with OPG

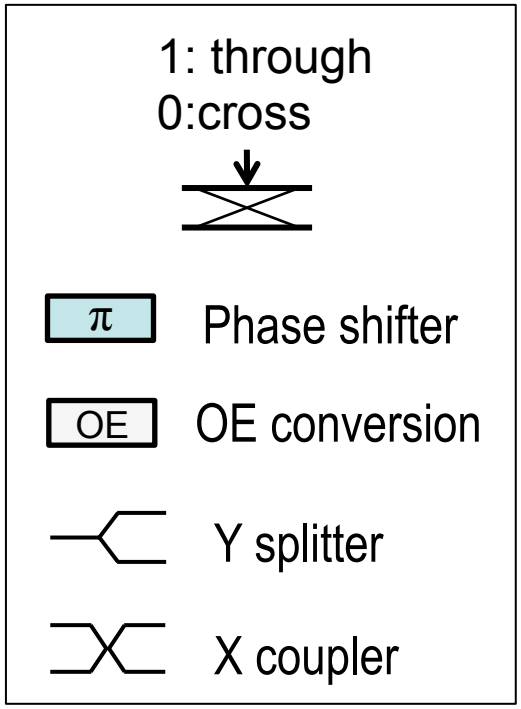
- XOR/MUX-dominant data-path operation
  - ✓ Parallel Adder, Multiplier, and Barrel Shifter etc.

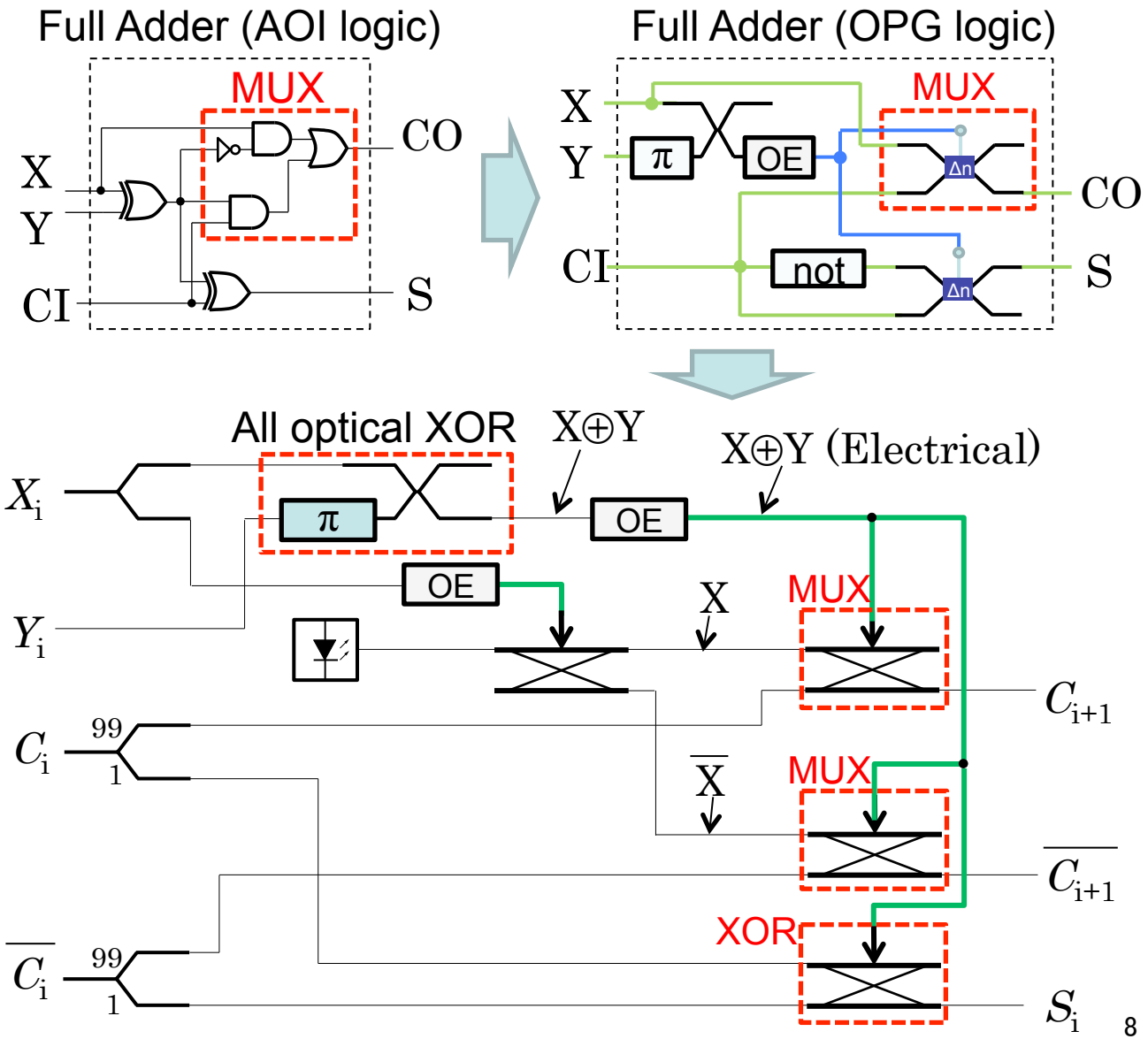


  - ✓ Parallel adder as a first step
    - ➢ Can be constructed with serial connections only

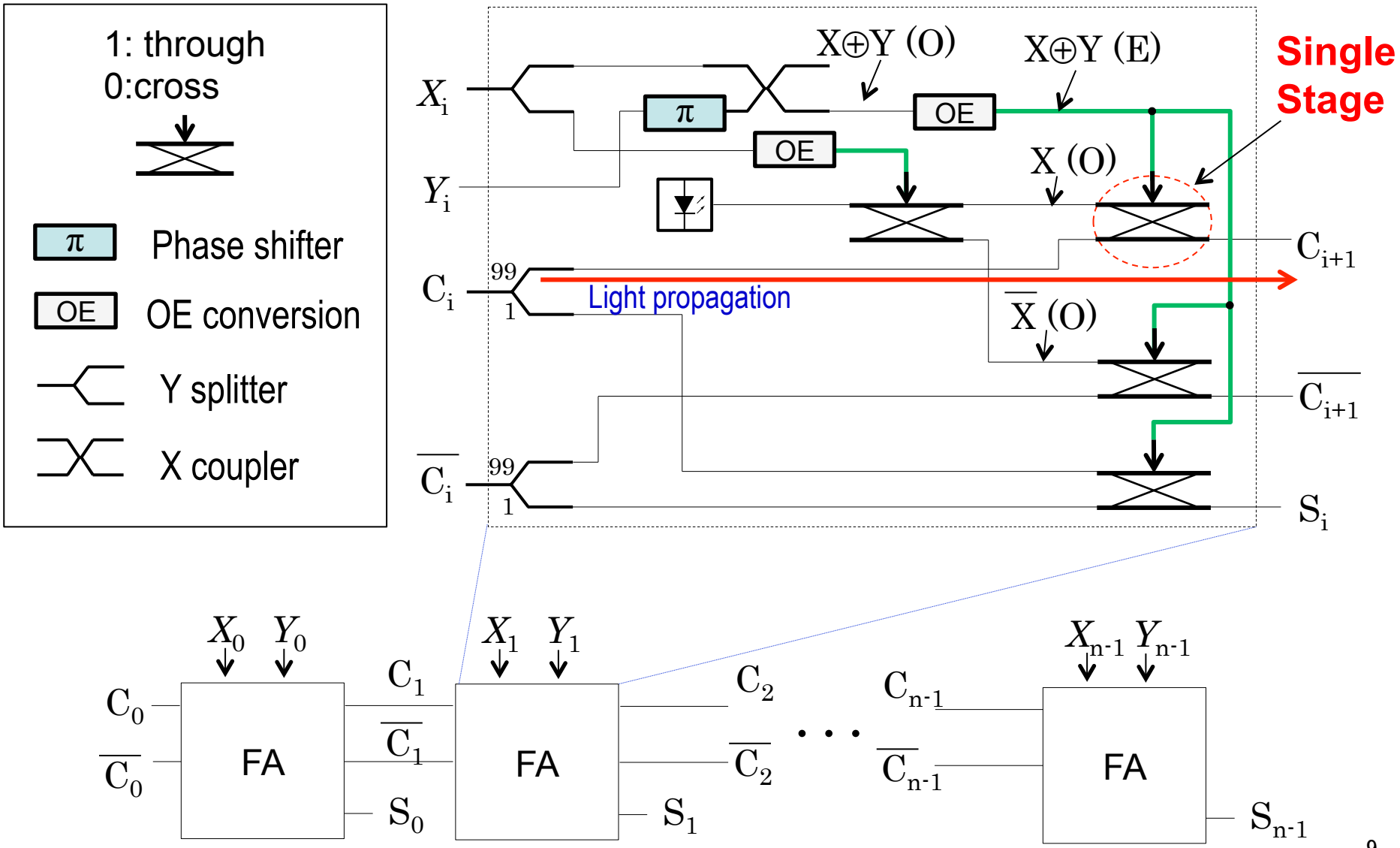
Optical Full Adder

Library Cells in OptiSPICE simulator (Optoelectronic circuit simulator)



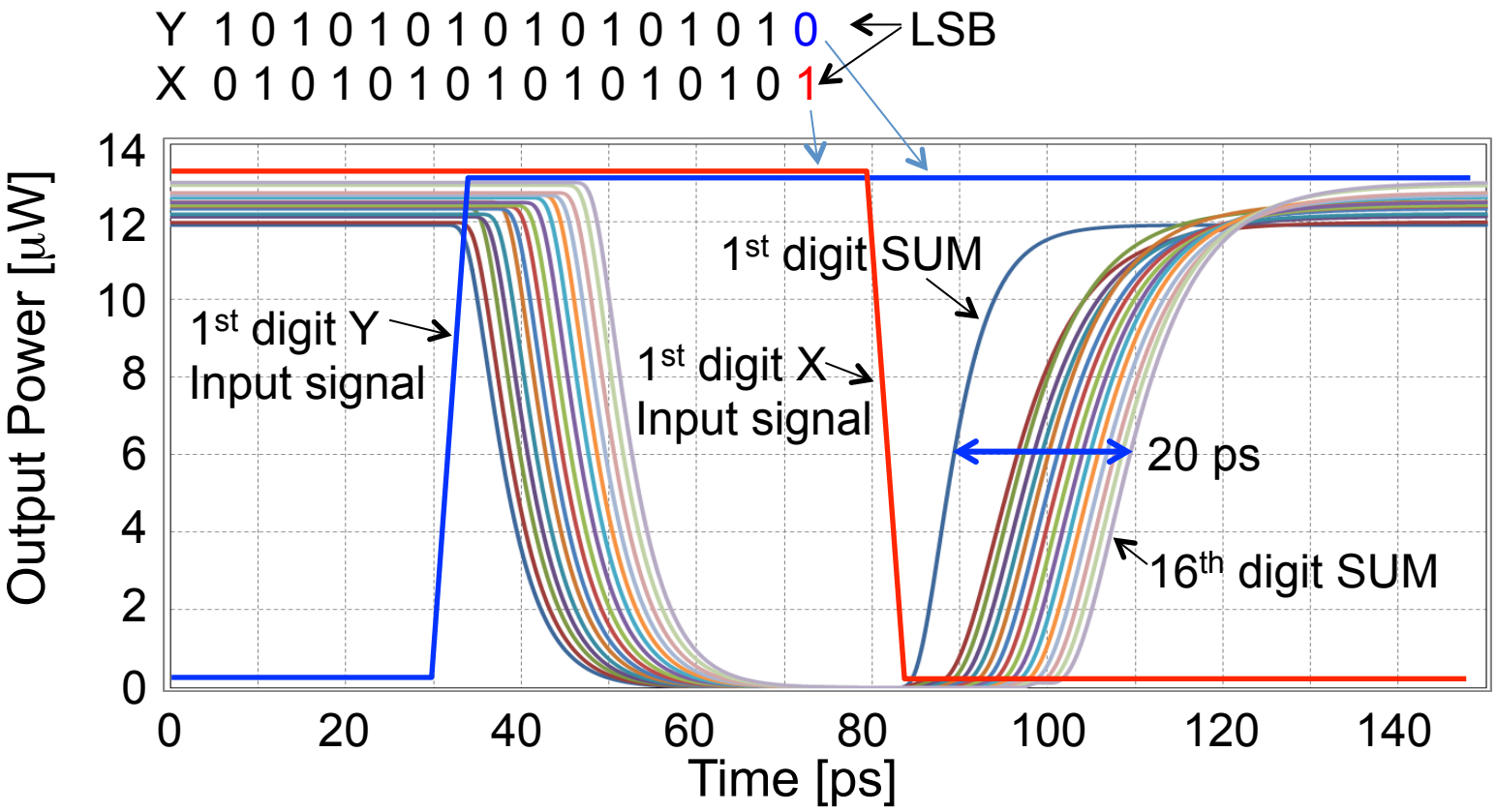


Design and Evaluation: 16-bit Adder



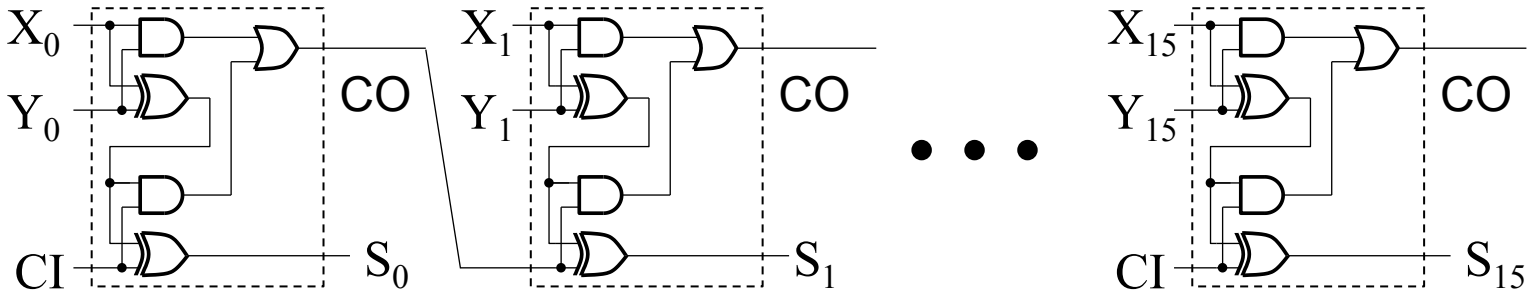
OptiSPICE Simulation Results

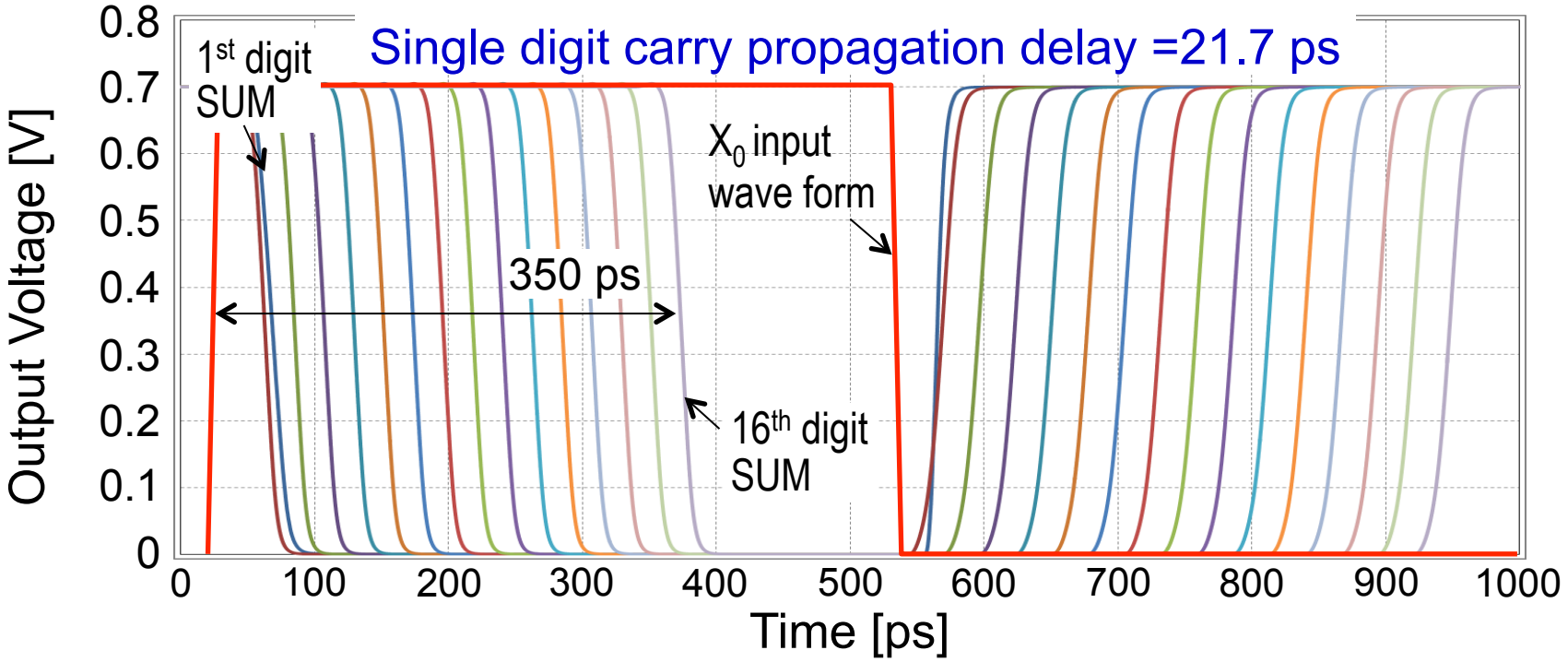
- Optoelectronic Circuit Simulator (HSPICE engine)
- Light-speed parallel adder operation confirmed
  - Per digit delay: ~1ps, Initial OE and switching delay: ~25ps



16-bit CMOS Adder as Comparison

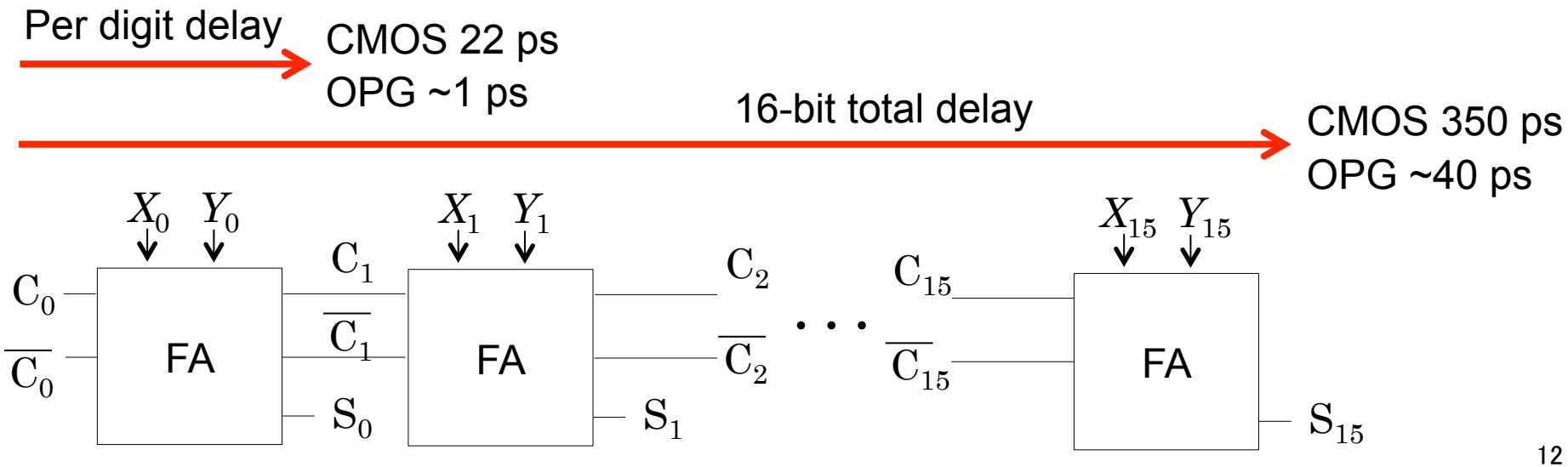
16 nm High Performance CMOS Technology PTM





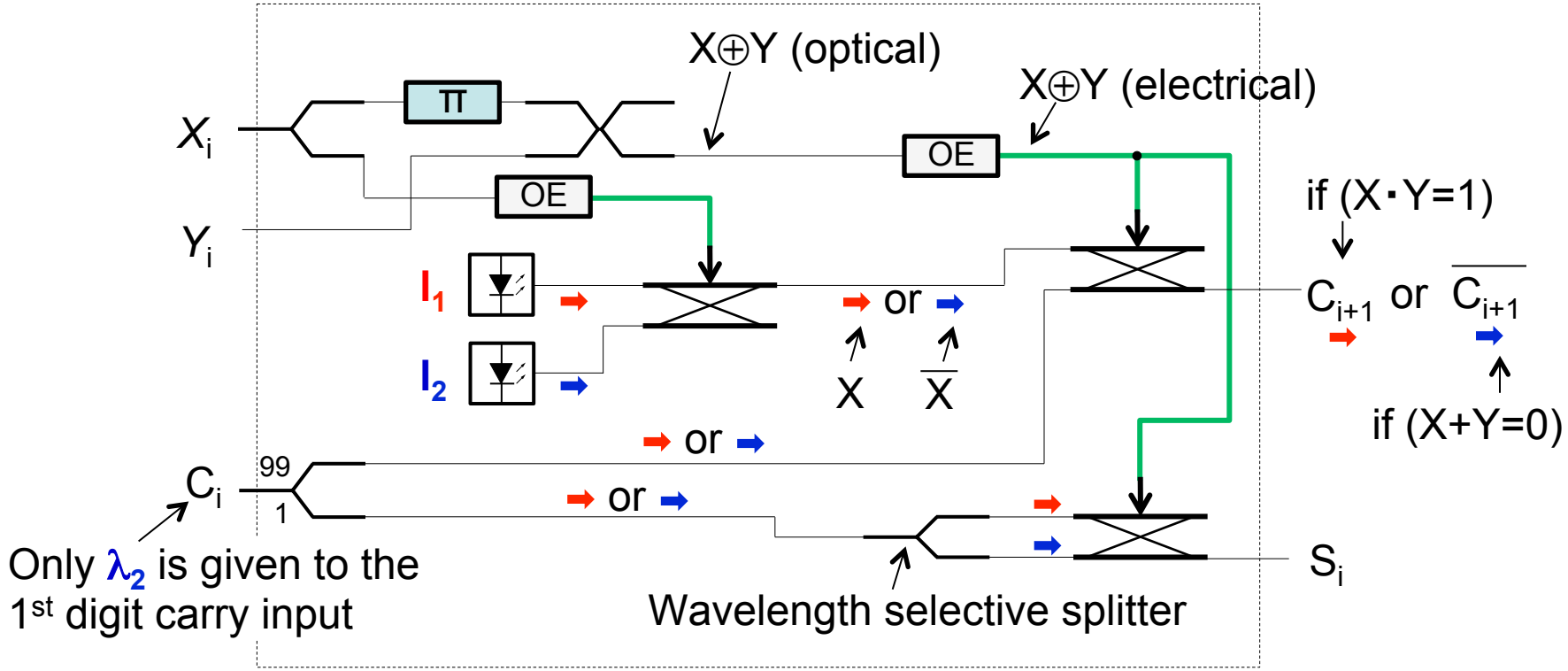
Comparison

- 16-bit parallel adder is designed with OPG
- Light-speed operation is confirmed
  - Per digit delay: OPG ~1 ps, CMOS 22 ps
  - 16-bit total delay: OPG ~40 ps, CMOS 350 ps



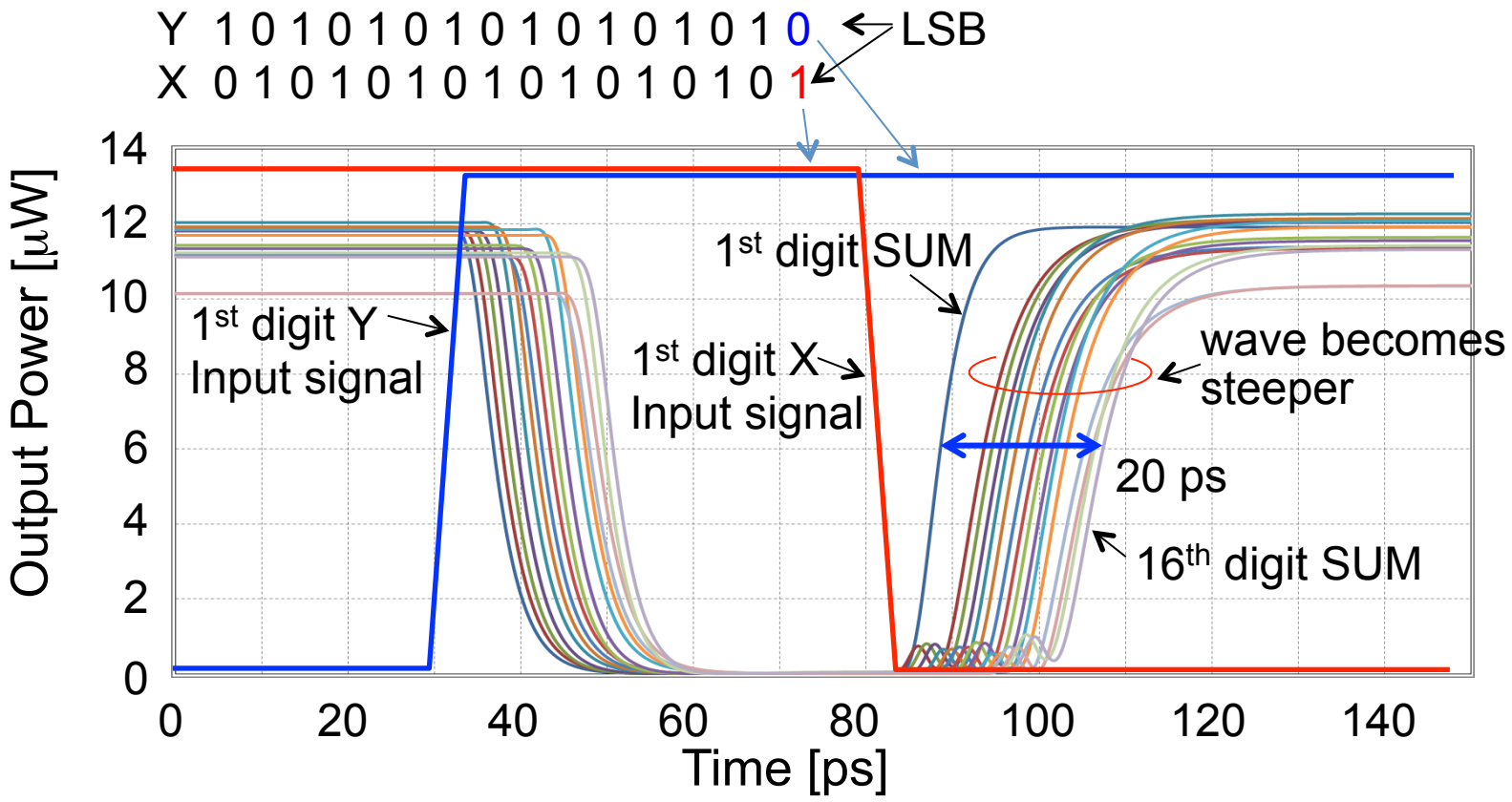
Wavelength Division Multiplexing

- Exploit WDM for reducing the circuit size
- λ_1 represents carry, λ_2 represents carry bar



OptiSPICE Simulation Results

- Different wavelengths for carry and carry bar
  - This structure reduces RC delay in electric control signal
  - Per digit delay: ~1ps, Initial OE and switching delay: ~25ps



Related Work

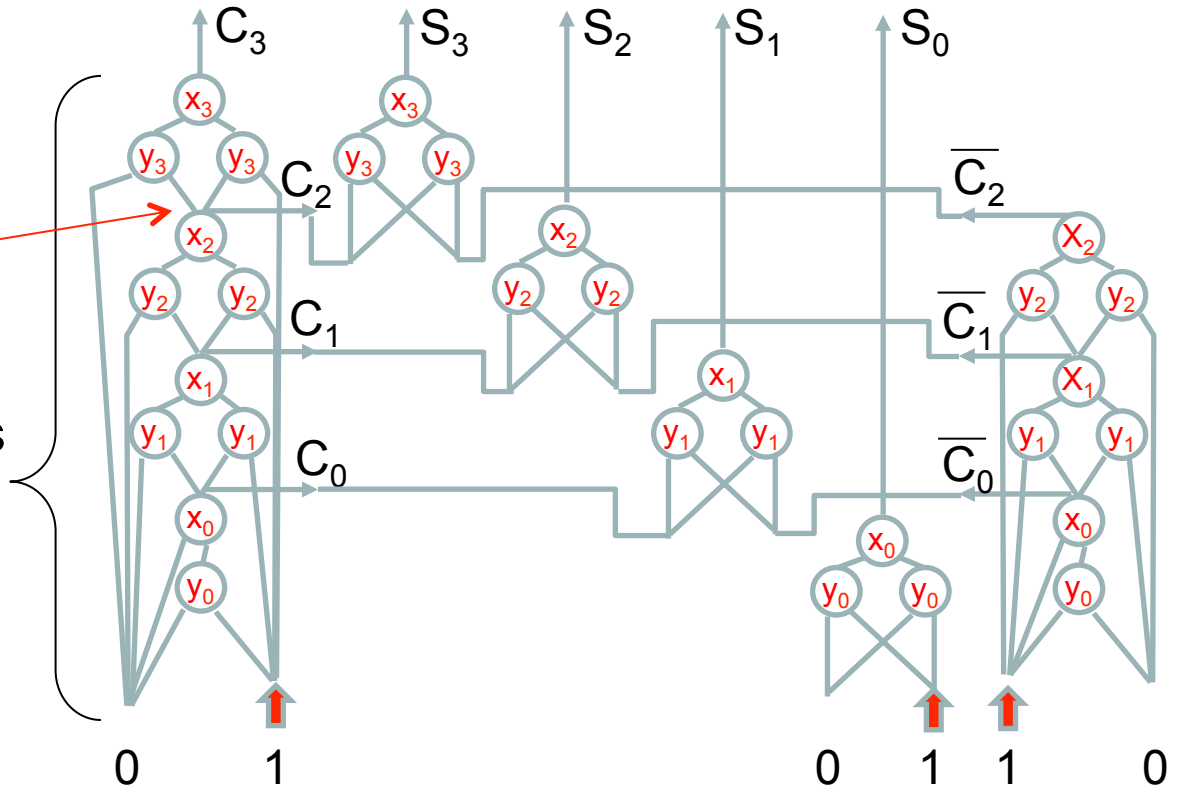
- Parallel adder based on shared BDD

T. Asai, Y. Amemiya, and M. Kosiba,“A Photonic-Crystal Logic Circuit Based on the Binary Decision Diagram," in *Proc. of IWPECS* ,T4-14, March 2000.

72% loss per digit

Max fan-out = 4
Large power loss

Serial connections
= # digits x 2
Large power loss



Summary

- 16-bit parallel adder is designed with OPG
- Light-speed WDM operation confirmed
  - Per digit delay: OPG ~1 ps, CMOS 22 ps
  - 16-bit total delay: OPG ~40 ps, CMOS 350 ps
- Power loss is an issue to be resolved
  - Per digit power loss ~20%

- Future work
  - Extend this to more complicated functions

Acknowledgement

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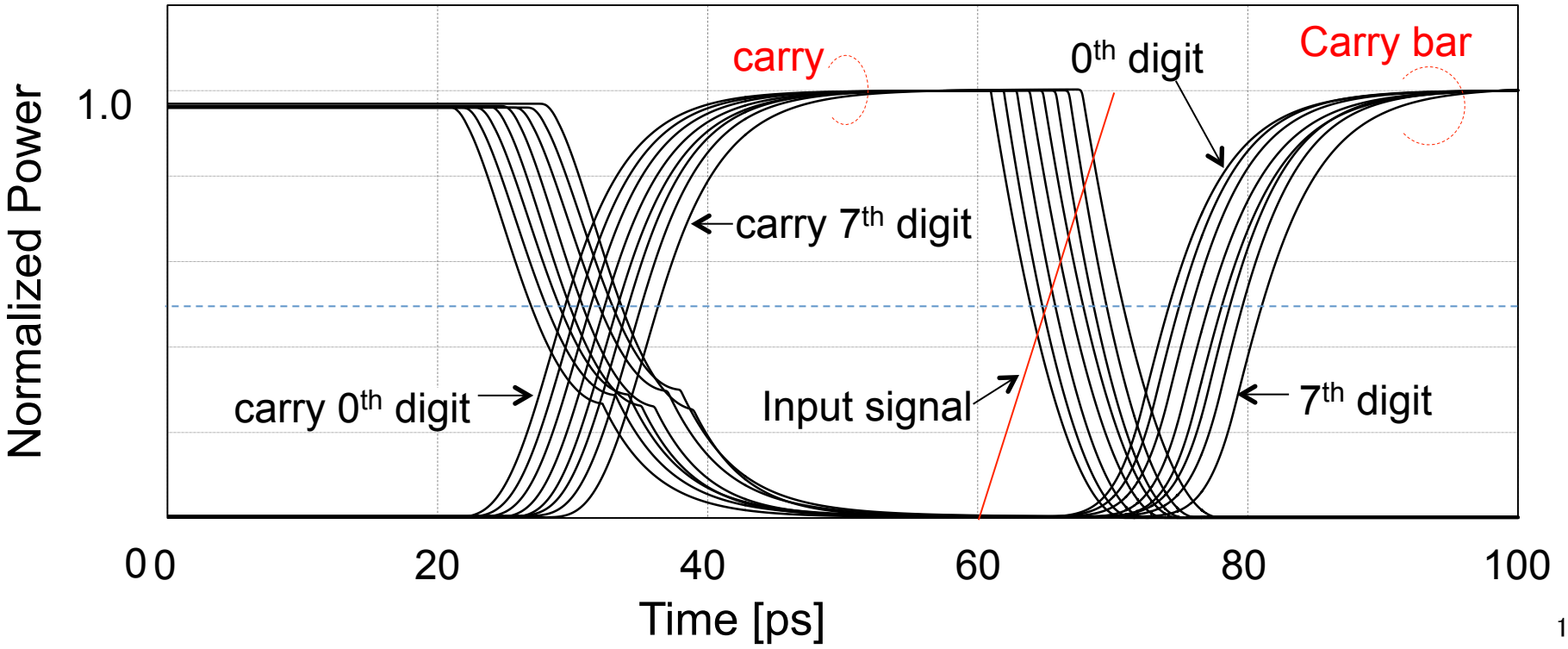
Backup

Results of OptiSPICE Simulation

- Optoelectronic Circuit Simulator (HSPICE engine)
- Light-speed parallel adder operation confirmed
  - Per digit delay: ~1ps, Initial OE and switching delay: ~10ps
  - 8-bit CMOS adder with 16nm HP PTM: 174 ps



Power Loss in Adder Operation