SCALING UP SILICON PHOTONICS: WHERE ARE THE CHALLENGES

Wim Bogaerts

OPTICS2017 Workshop, Lausanne, 31 March 2017

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imec
embracing a better life

THE PHOTONICS RESEARCH GROUP

Research Group of Ghent University

- within Engineering Faculty
- within Dept. of Information Technology (INTEC)
- associated with IMEC
- member of NB Photonics

8 Professors (5 ERC grantees)

16 postdocs

50 PhD students

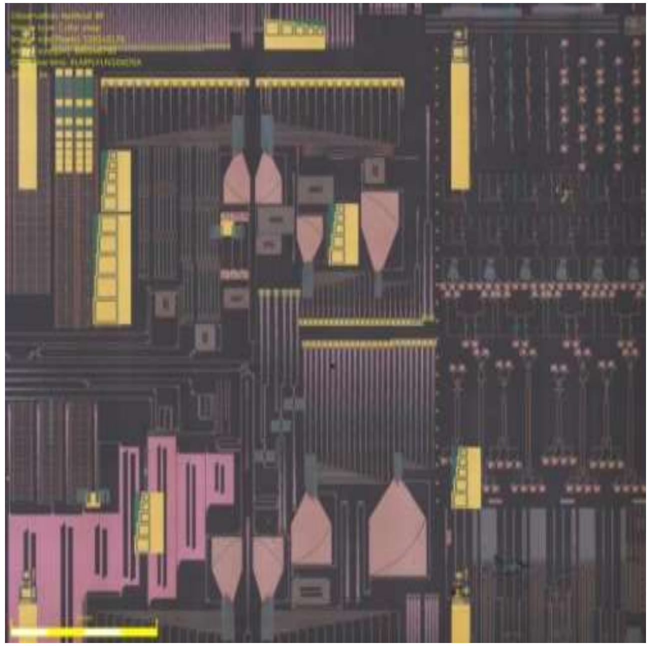
10 support staff

1 Business developer

15 nationalities

WHAT IS SILICON PHOTONICS?

The implementation of high density photonic integrated circuits by means of CMOS process technology in a CMOS fab



Pictures, courtesy of imec

Enabling complex optical functionality on a compact chip at low cost

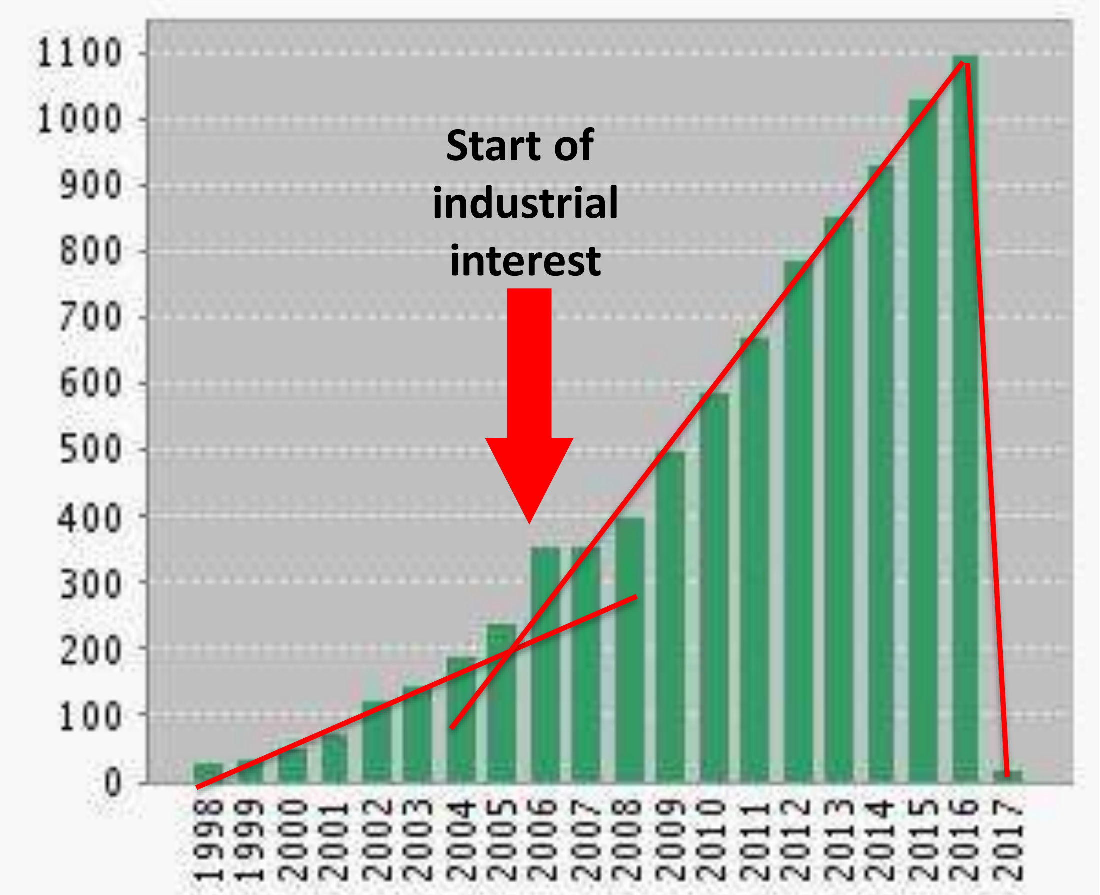
The past 15 years: stunning research progress

Citation Report: 8566

(from Web of Science Core Collection)

You searched for: **TOPIC:** (silicon) *AND* **TOPIC:** (photonic*) *AND* **YEAR PUBLISHED:** (1996-2017)

PUBLICATIONS EACH YEAR



(Conferences not included)

INDUSTRIAL TAKE-UP EXAMPLES IN TELECOM/DATACOM/DATA CENTERS

- active optical cables (eg PSM4: 4x28 Gb/s on parallel fibers)
- WDM transceivers (eg 4 WDM channels x 25 Gb/s on single fiber)
- coherent receiver (eg 100 Gb/s PM-QPSK)
- fiber-to-the-home bidirectional transceiver (eg 12 x 2.5 Gb/s)
- monolithic receiver (eg 16x20Gb/s)
- 40Gb/s, 50Gb/s and 100 Gb/s Ethernet (future: 400Gb/s)
- …

Finisar
ACACIA COMMUNICATIONS, INC.
KAIAM
JUNIPER NETWORKS
aurrion
ELENION TECHNOLOGIES
intel
CISCO
LIGHTWIRE
SKORPIOS TECHNOLOGIES
TeraXion
GHENT UNIVERSITY
IBM
imec
Mellanox TECHNOLOGIES
KOTURA
molex
LUXTERA NANOPHOTONIC INTEGRATED CIRCUITS
Caliopa
HUAWEI

Why Silicon photonics?

Large scale manufacturing

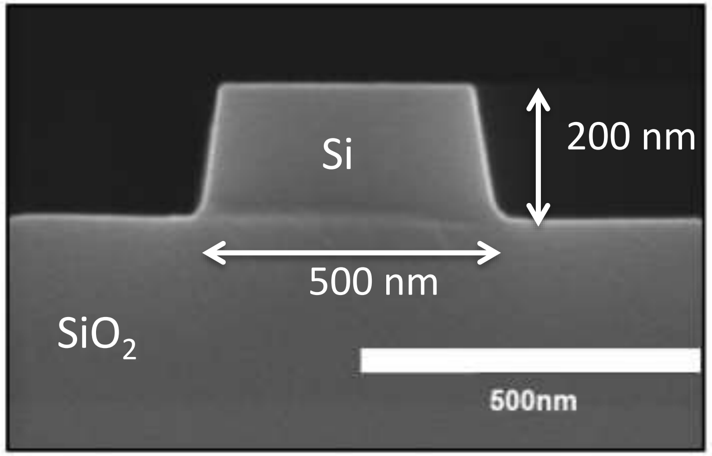
Scale

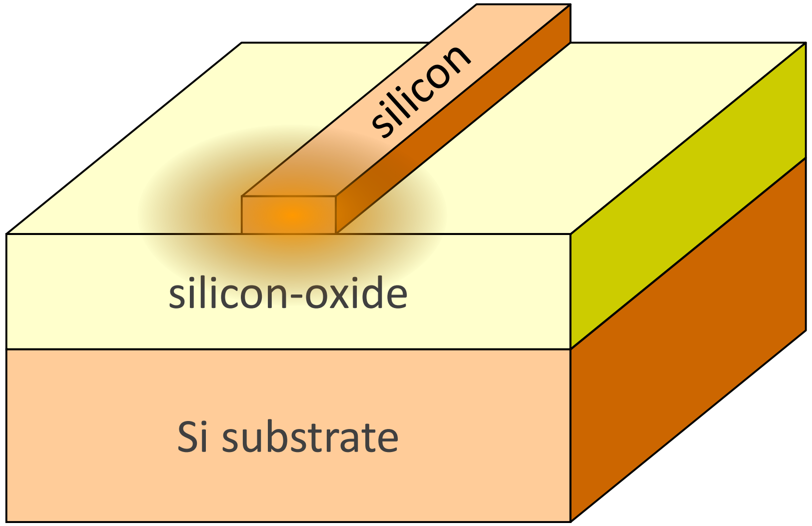
Submicron-scale waveguides

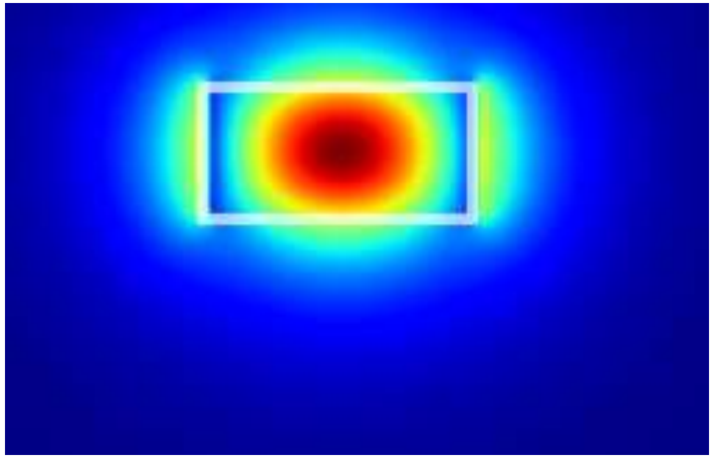
WAVEGUIDES: SILICON PHOTONIC WIRES

High index contrast waveguides

- submicrometer dimensions
- small bend radius
- high-density photonics
  (> 10000 components/chip)





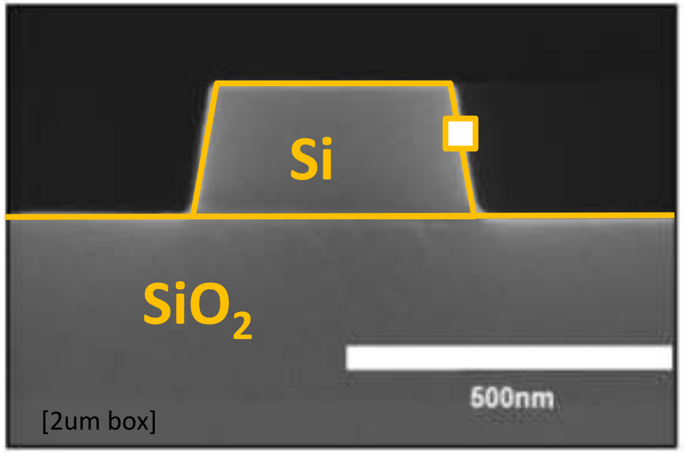


optical mode

HIGH INDEX CONTRAST: A BLESSING AND A CURSE

Every nm^3 matters

CMOS technology is the only manufacturing technology with sufficient nm-process control to take advantage of the blessing without suffering from the curse

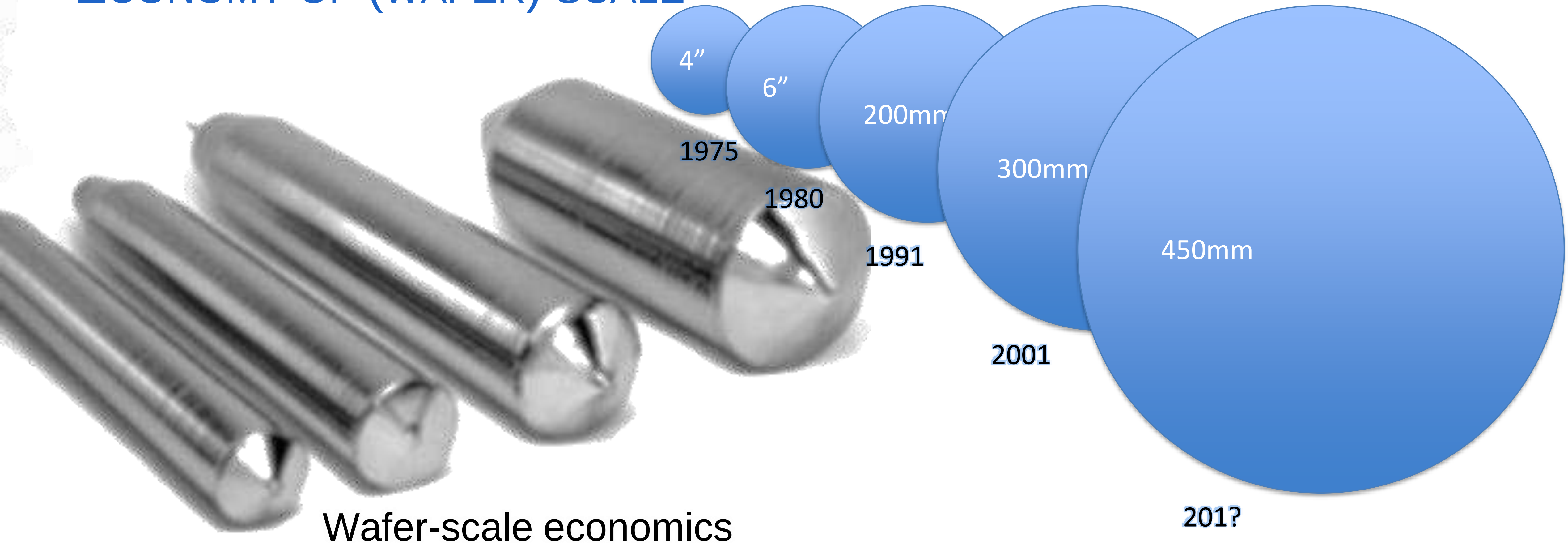


VARY LARGE SCALE (INTEGRATION)

TSMC Fab 14
1.4M 300mm wafers / year

Source: TSMC

Economy of (wafer) scale



Wafer-scale economics

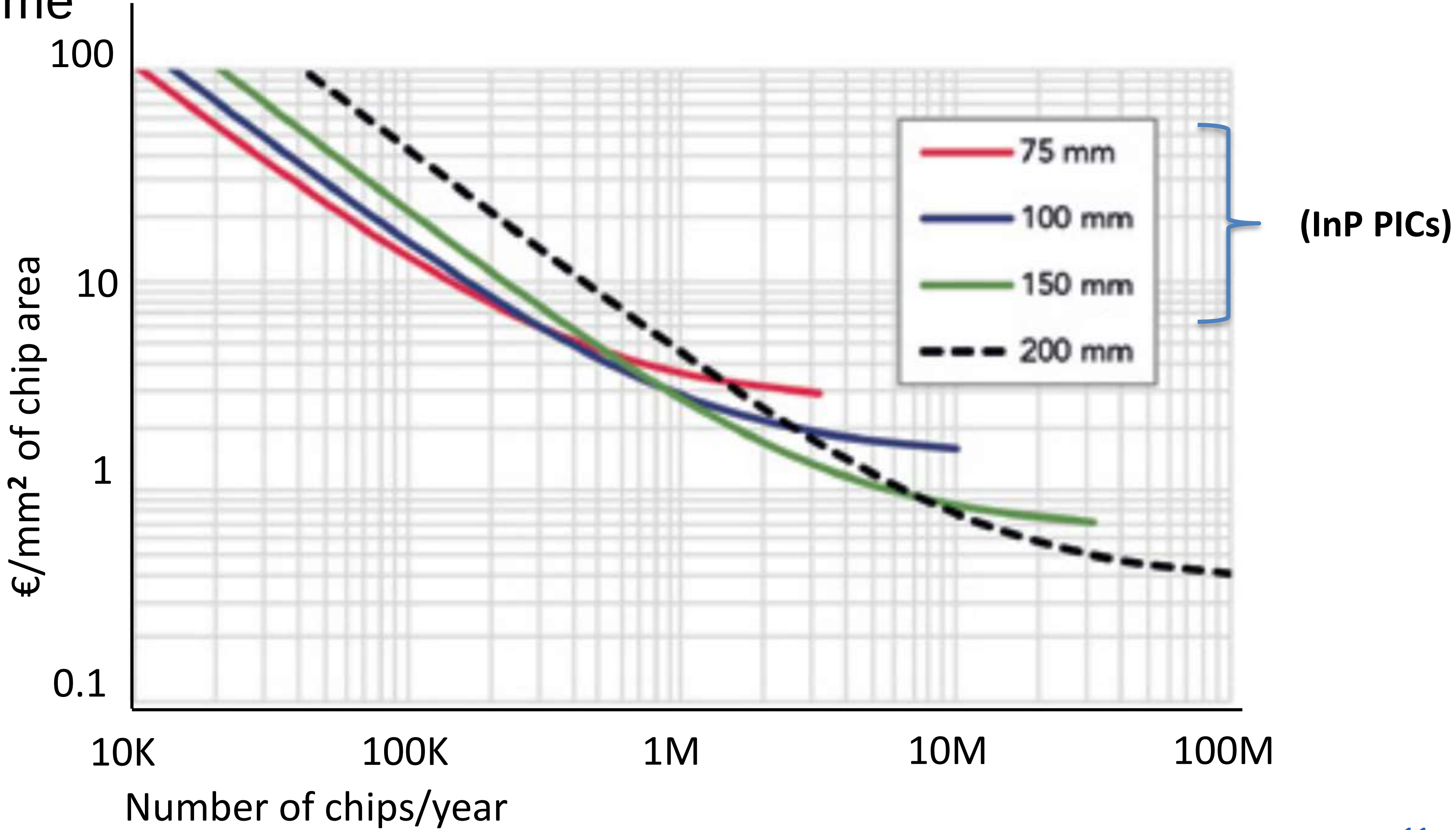
- Larger wafers
- Higher volumes
- Massive parallellism
- Minimal marginal cost

- More expensive tools
- Higher volumes
- Larger fixed cost

Economy of (wafer) scale

Chip cost per mm^2 in a dedicated, loaded fab.

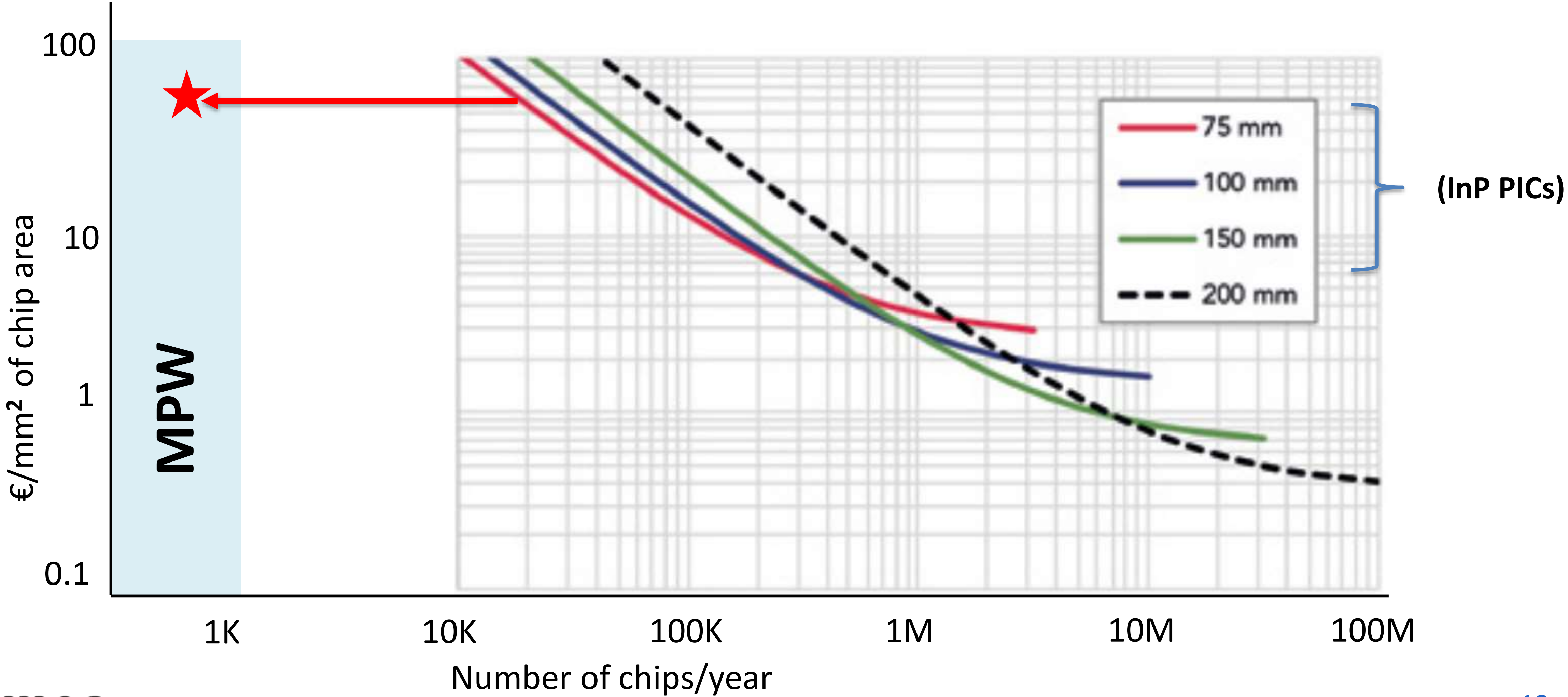
Strong function of volume



Source: JePPIX Roadmap 2015

ECONOMY OF (WAFER) SCALE

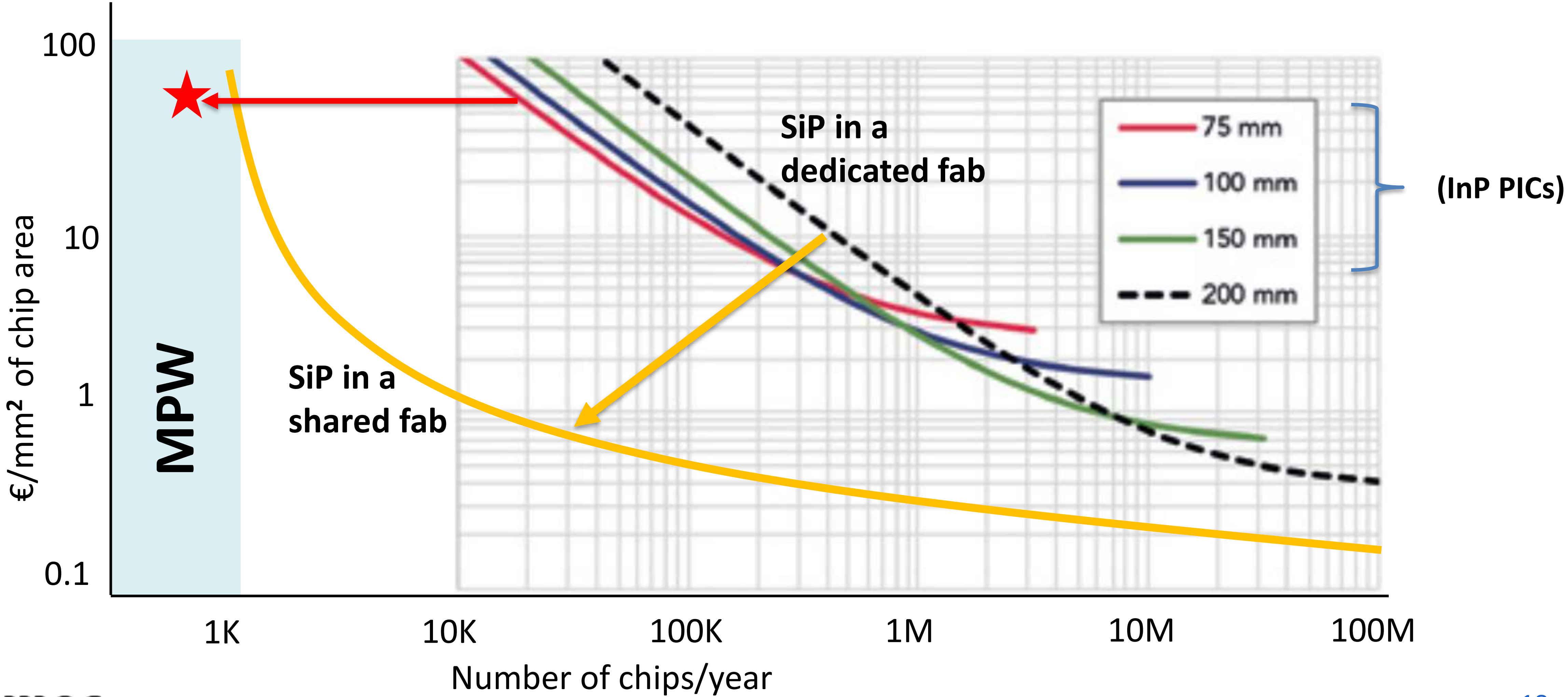
Chip cost per mm^2 in a dedicated, loaded fab.



Source: JePPIX Roadmap 2015

ECONOMY OF (WAFER) SCALE

Chip cost per mm² in a ~~dedicated~~, loaded fab.



Source: JePPIX Roadmap 2015

A SHARED FAB?

CMOS Fab making both CMOS and silicon photonics

- CapEx for CMOS fabrication fully recovered (= old fab)
- Fab should have some (variable) spare capacity

Technological capabilities required?

- preferably 300mm (better wafers)
- 65-90nm CMOS node
- Upgrade with Germanium epi
- Upgrade with better lithography

THE DRIVE FOR SILICON PHOTONICS: OPTICAL INTERCONNECTS

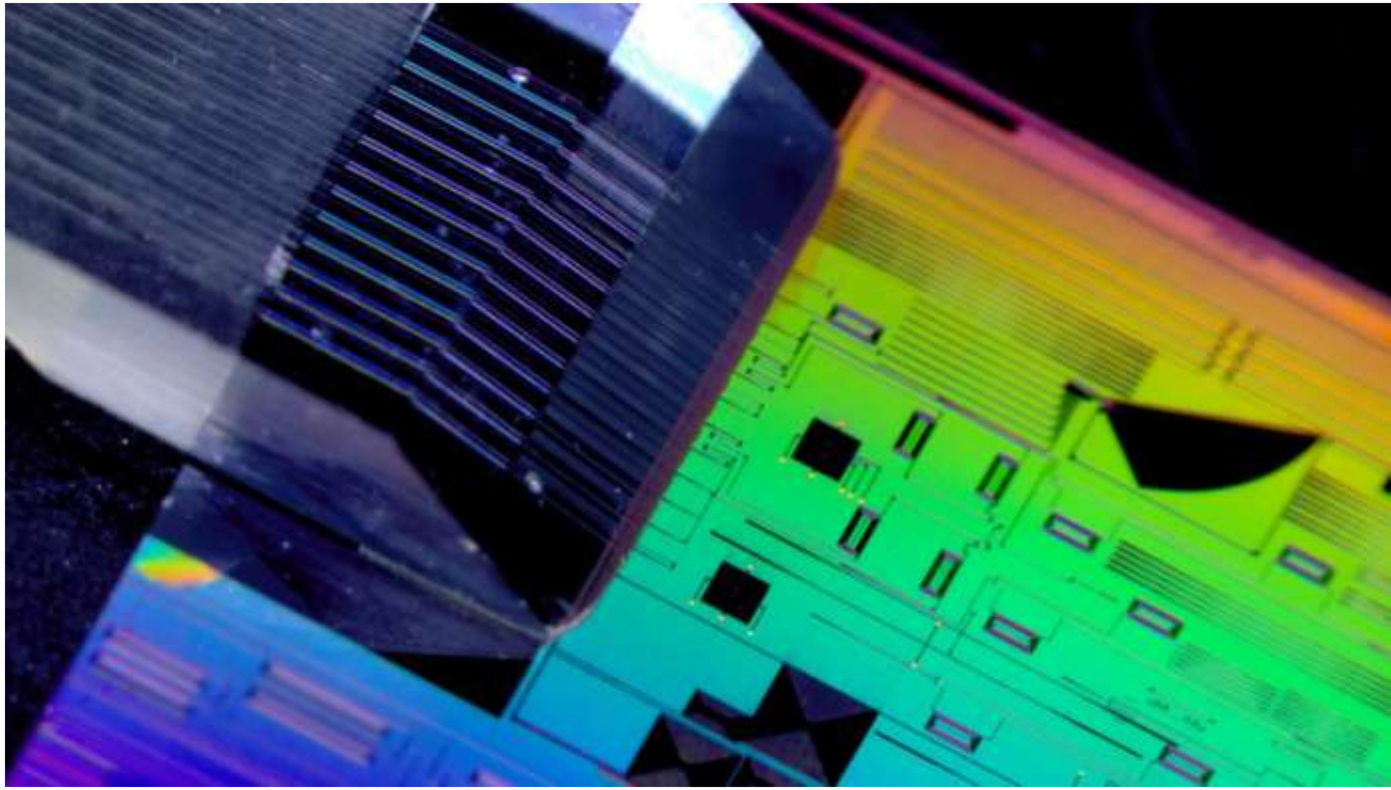
Optical communication has

- higher bandwidth
- lower propagation loss

Optical interconnects are shrinking

- Data center
- Rack-level
- Board-level
- Package level

…



WHAT IS HIGH VOLUME?

Saturated 200mm fab

5×5 mm2 per chip
1,250 chips / wafer (200mm)
40,000 wafers / month

50 Mchips / month

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What is High volume?

Saturated 200mm fab

5×5 mm2 per chip
1,250 chips / wafer (200mm)
40,000 wafers / month

50 Mchips / month

~1 fabmonth

2018

Datacenter Cabling

50 mega datacenters
10000 racks / center
64 cables / rack
2 transceivers per cable

64 Mchips

<2 fabyears

2022

Datacenter Cabling

50 mega datacenters
10000 racks / center
1000 cables / rack
2 transceivers per cable

1 Gchips

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SILICON PHOTONICS: ONLY FOR INTERCONNECTS?

Transistors: only for calculators?

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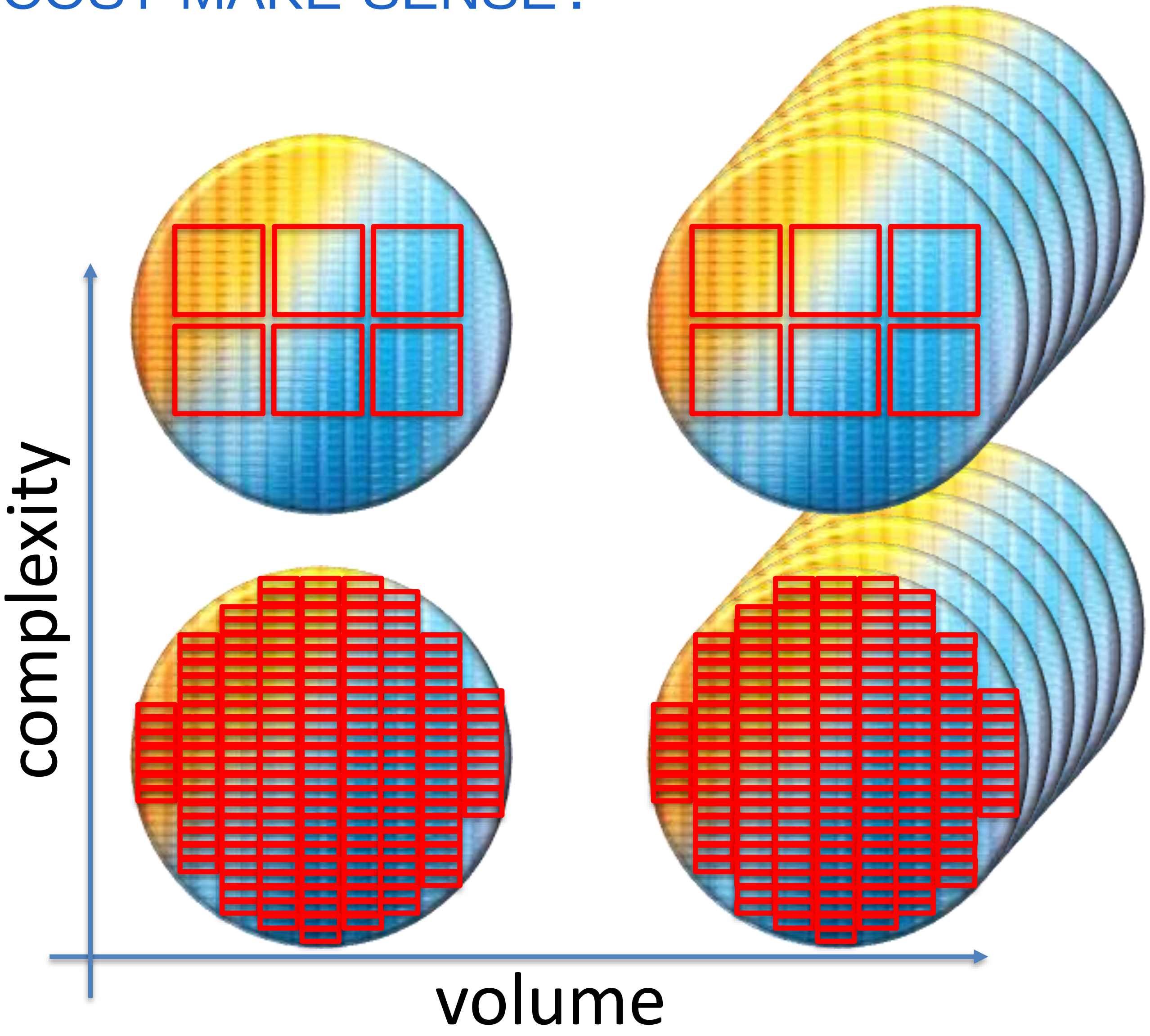
When does this functionality/cost make sense?

Large Volume

- millions of chips
- high yield
- low cost

High complexity

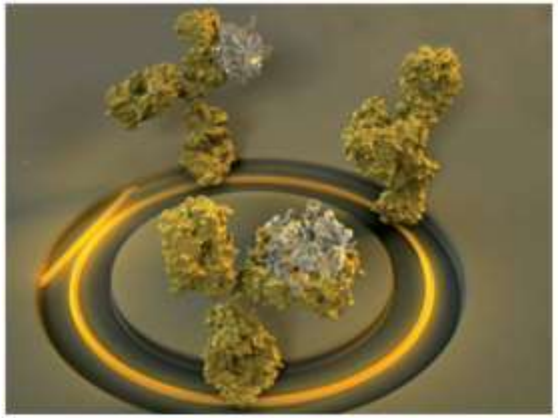
- thousands of functions on a chip
- large-scale integration
- high cost
- yield?

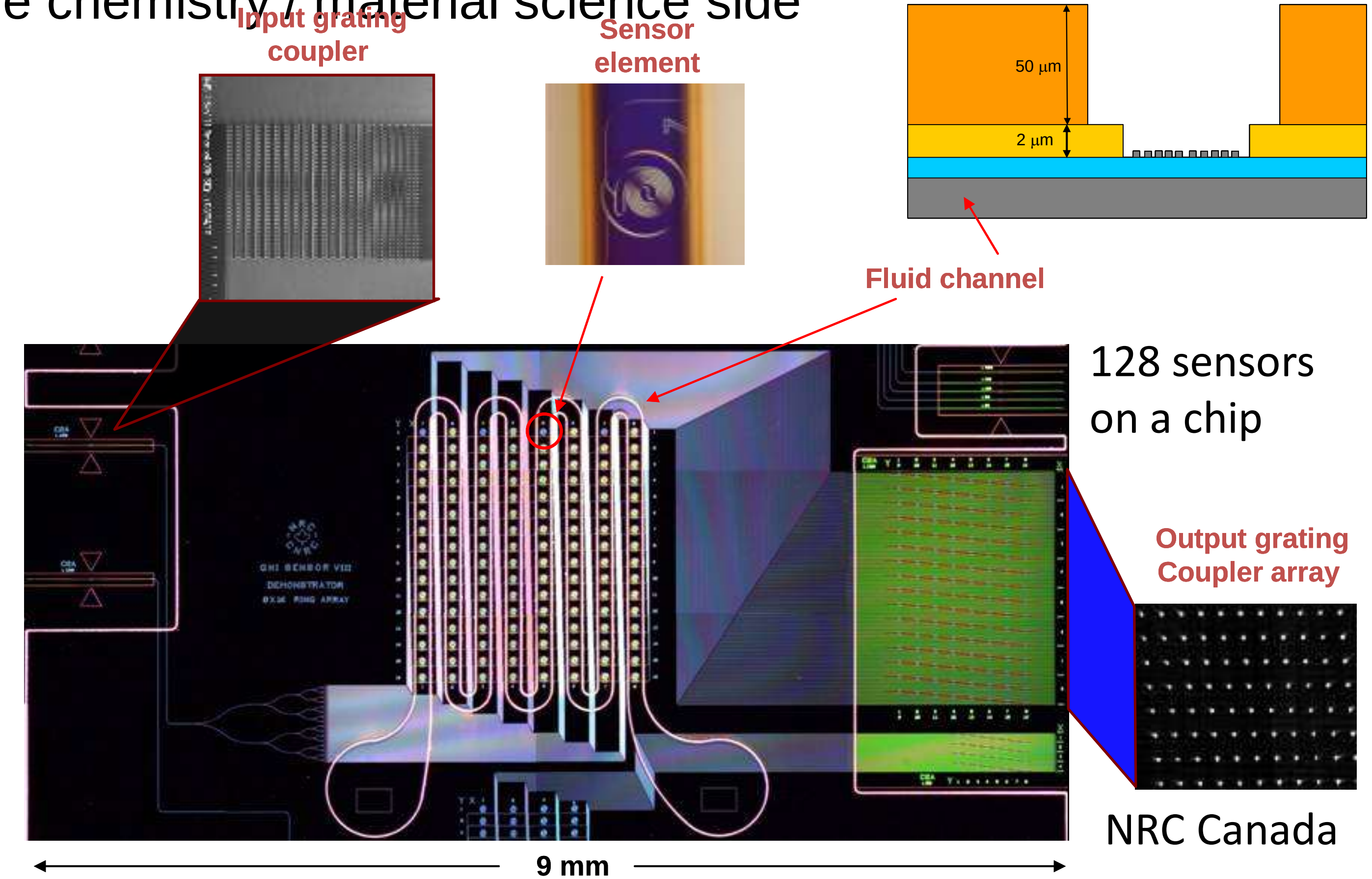


Bio & gas sensors

- Silicon photonics: cheap disposable sensor
- Needs transducer to translate the presence of particular molecules into a refractive index change
- Mostly work on the chemistry / material science side


Genalyte


Genalyte

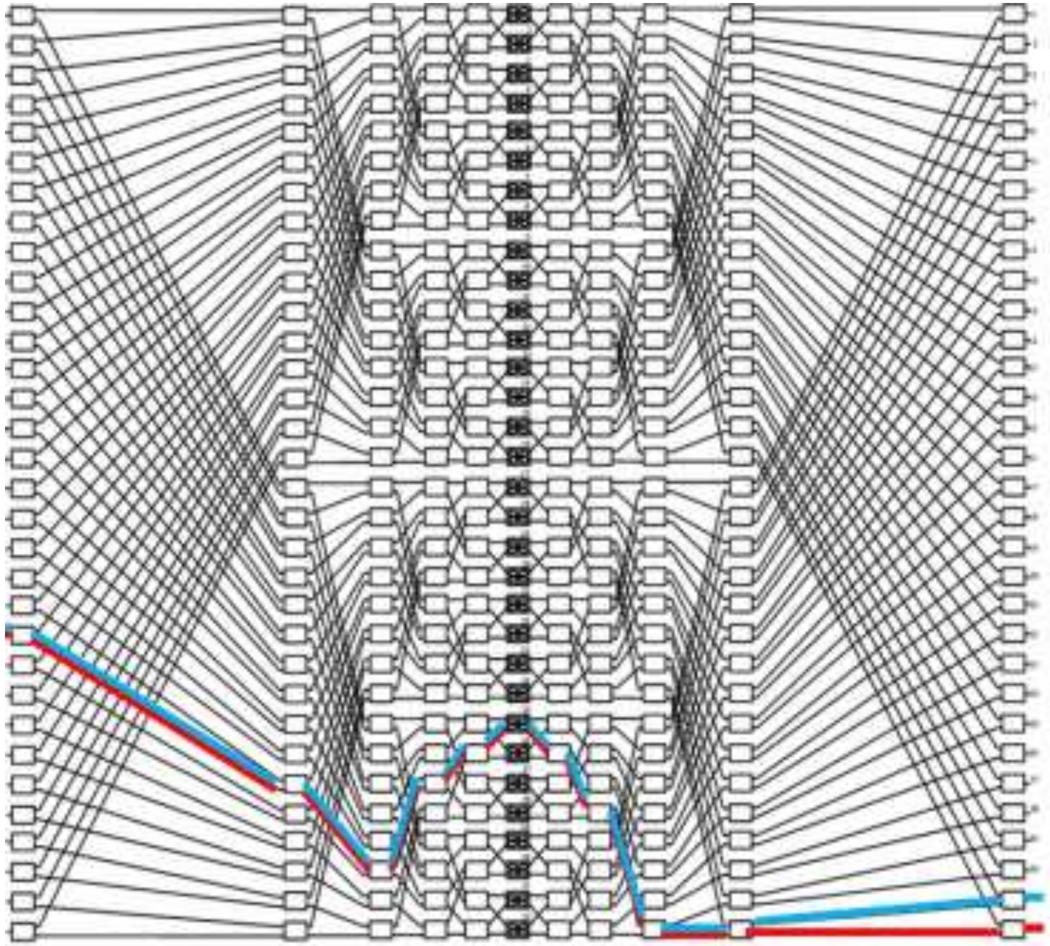


128 sensors on a chip

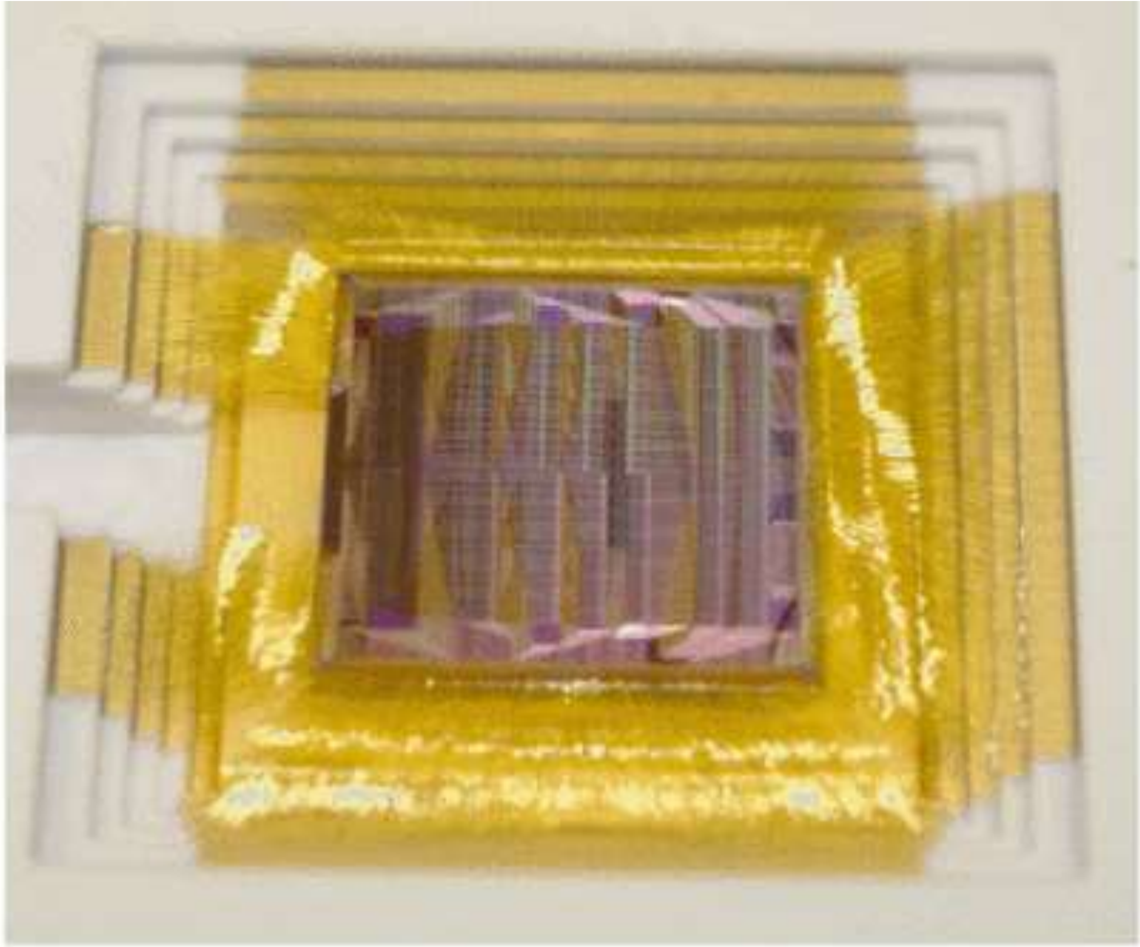
NRC Canada

Compact switch matrices

32 x 32 switch matrix on a 12 x 12 mm^2 chip



b)

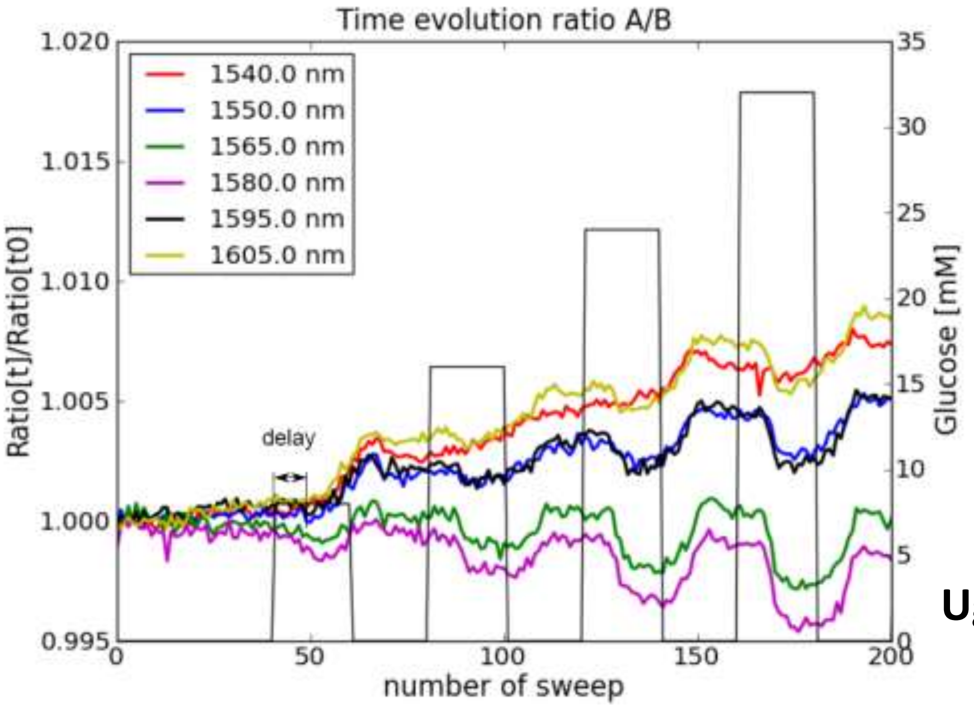


Huawei Canada

SPECTROSCOPIC SENSOR SYSTEMS

E.g. Integrated glucose monitoring

- 4 spectrometers in 4 wavelength regions
- measure clinically relevant glucose concentrations in biological fluids



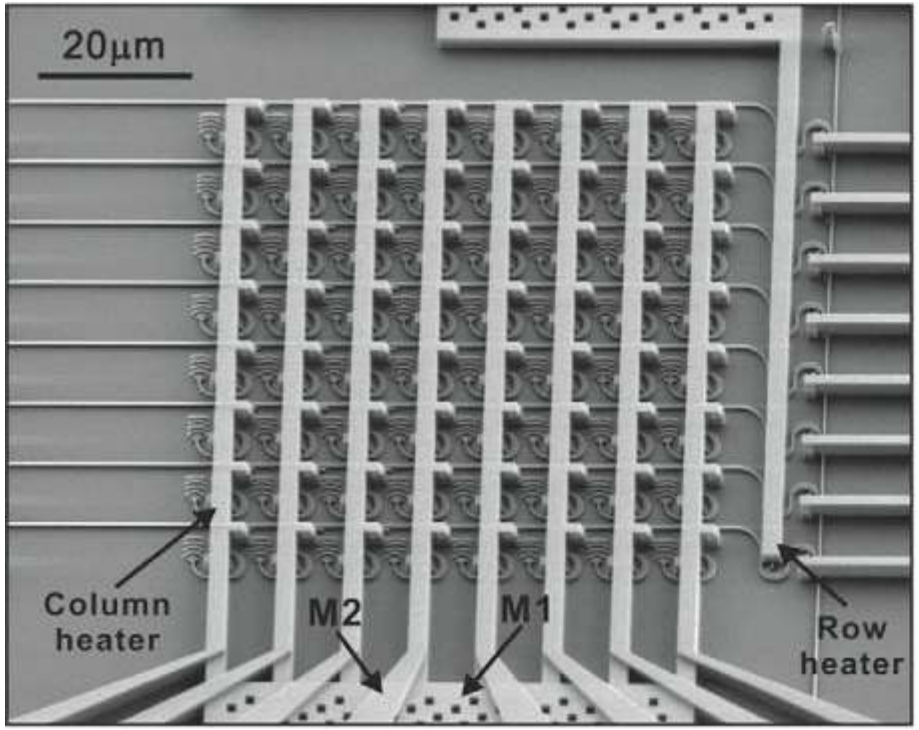
Ugent, IMEC, Indigo Medical

LARGE PHASED ARRAYS

Large arrays of optical “antennas”

Individual phase/amplitude control

Beam steering & forming



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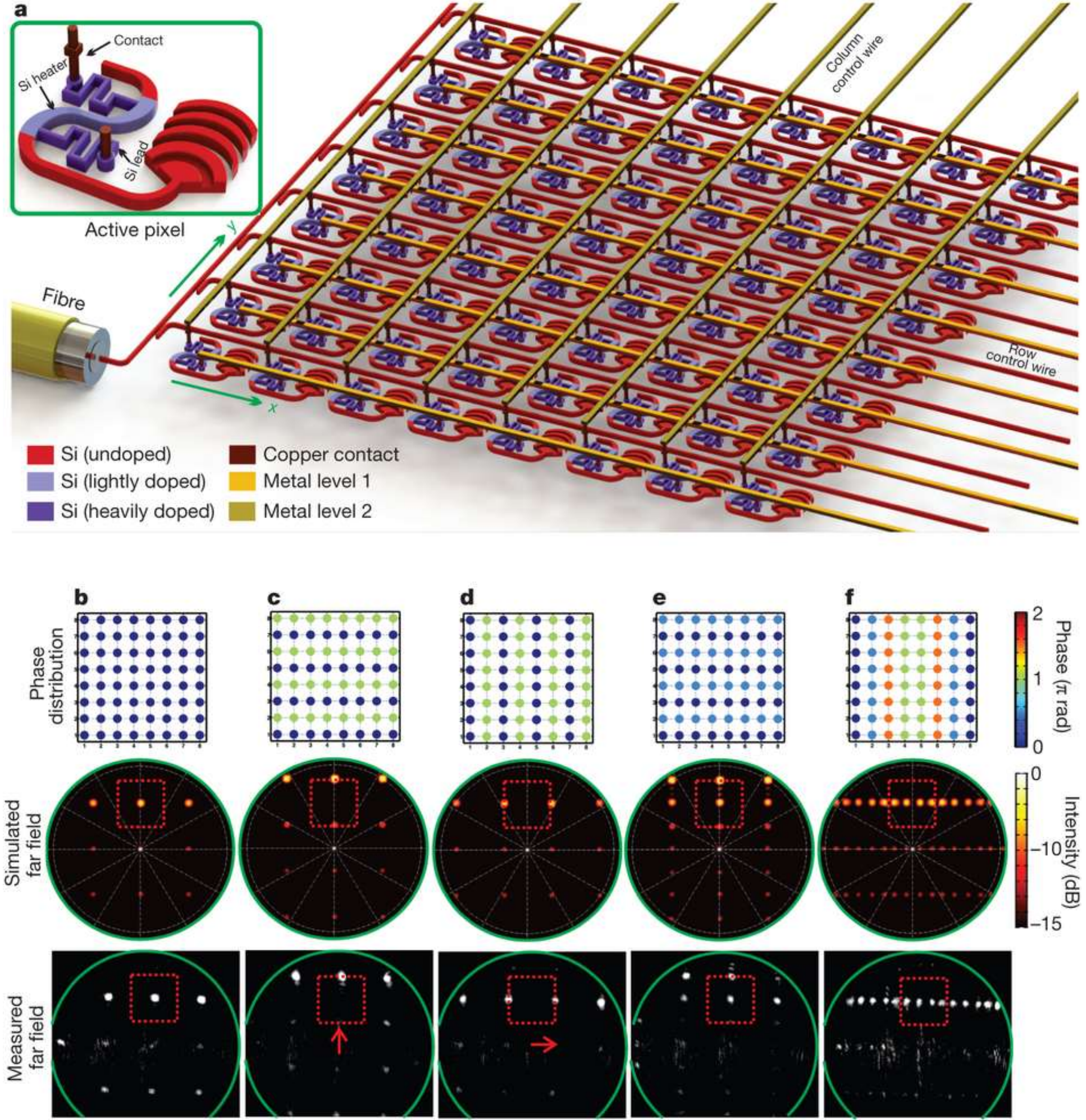

Jie Sun, MIT, INTEL 2016

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Silicon photonics and CMOS

The **STRENGTH** of Silicon Photonics

is that it can make use of CMOS-technology

The **WEAKNESS** of Silicon Photonics

is that it **must** make use of CMOS-technology

CMOS-technology requires insanely expensive infrastructure
but delivers ridiculously cheap chips
with a ludicrous degree of sophistication

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Who owns a Fab for silicon photonics?

Vertically integrated electronics manufacturers

- high-end or specialty electronics (e.g. INTEL, ST)
- Silicon Photonics for own use or select partners

NO ACCESS

CMOS Foundries (TSMC, Global, Silterra, …)

- commodity electronics processes in high volumes
- Silicon photonics for industrial customers
- Need sufficient volume to warrant upfront cost

LARGE VOLUME

Research Fabs

- Already running silicon photonics (IMEC, LETI, IME, IHP, CNSE, …)
- Prototyping services and Multi-project-wafer shuttles
- No capacity or interest in larger volumes?

LOW VOLUME

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TECHNOLOGY PLATFORMS FOR SILICON PHOTONICS

R&D and prototyping platforms:

- Imec, Belgium (MPW-service through ePIXfab / Europractice)
- CEA-LETI, France (MPW-service through Europractice/CMP)
- VTT, Finland (“thick SOI”)
- IME, Singapore (MPW-service)
- AIM-Photonics, USA (MPW service starting 2016)
- AIST (MPW service planned in 2018)

Manufacturing platforms:

- Freescale
- ST Microelectronics
- IBM
- Intel
- **GlobalFoundries**
- **TowerJazz**

MULTI-PROJECT-WAFER (MPW) SERVICE

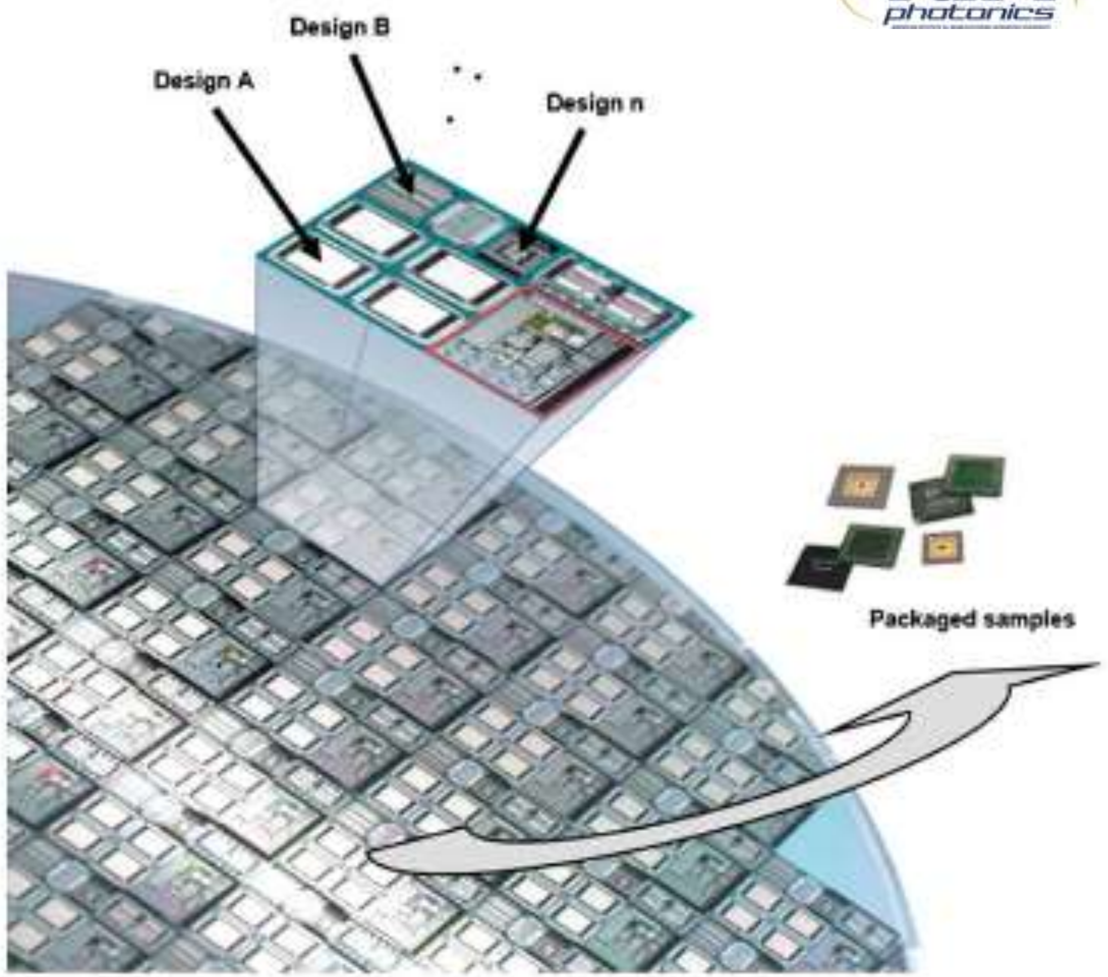
The “reticle” (= basic unit that is repetitively patterned on the wafer) has a maximum size of ~25 x 25 mm.

That equals 25 times a 5x5 mm chip.

On a 200 (300) mm wafer you can fit 50 (110) full fields.

So, let’s get organized.

1. Collect 25 5x5 mm designs from different users.
2. Combine these designs on a single mask set
3. Collectively process the wafers
   (typically 25 wafers in one batch)
4. Dice the wafers down to 5x5 mm chips (!!)
5. Send a few dozens of 5x5 mm chips to each user, together with an invoice.



FABLESS SILICON PHOTONICS

Many fabless Silicon Photonics companies have emerged

- from direct collaboration with fabs (Luxtera, ...)
- starting from MPW (Caliopa, Genalyte, Acacia)

Established players are also partnering

- e.g. Finisar with ST
- Many keep their fab a secret

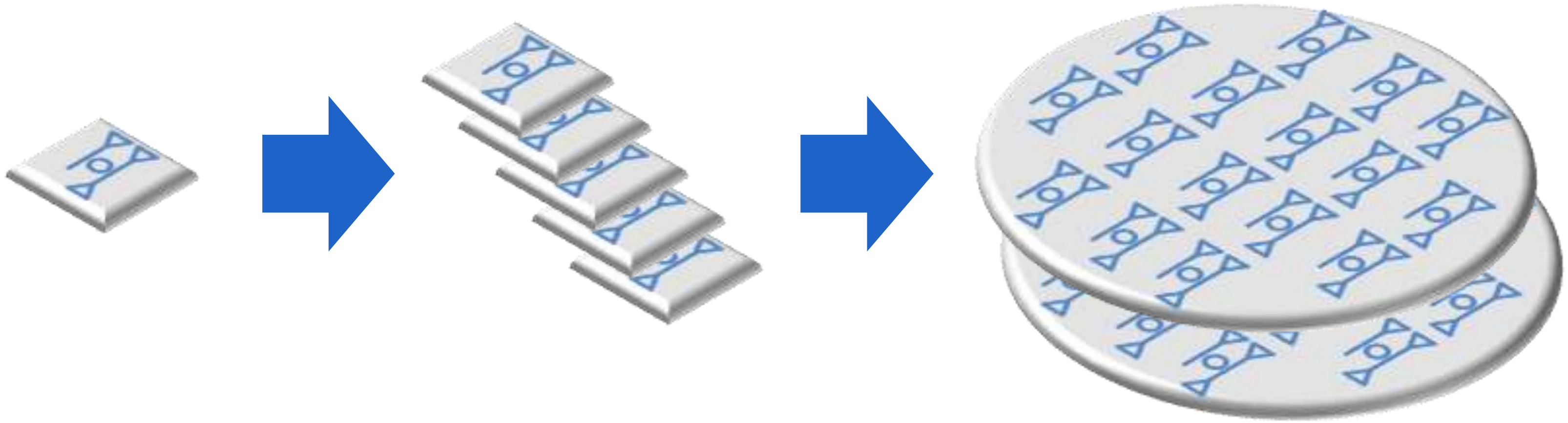
How to enter as a new (fabless) startup?

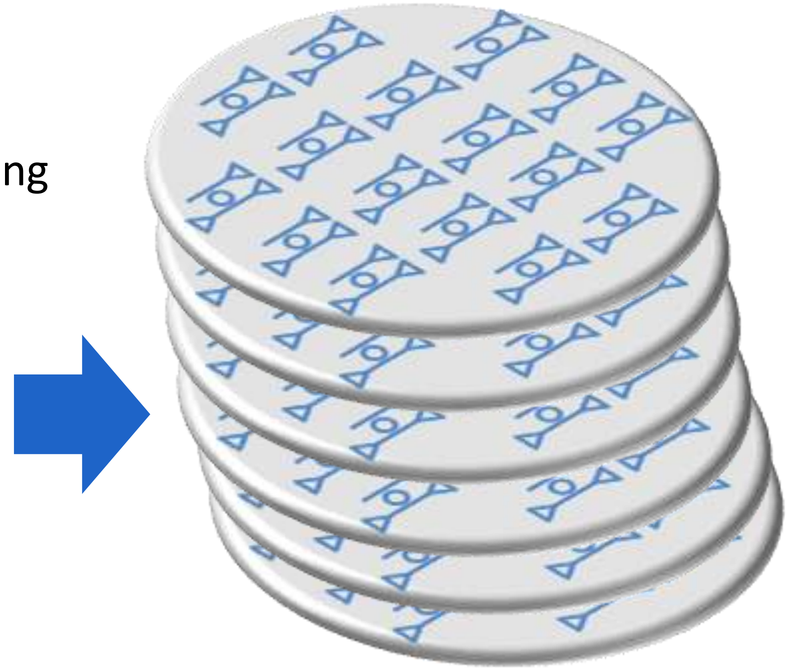
Silicon Photonics: From Idea to Product

What if you do not have a fab?

Test your idea
- prototype in your own clean room
- rapid iteration cycles

Low volume sampling
- Dedicated run in research fab
- Allows qualification testing





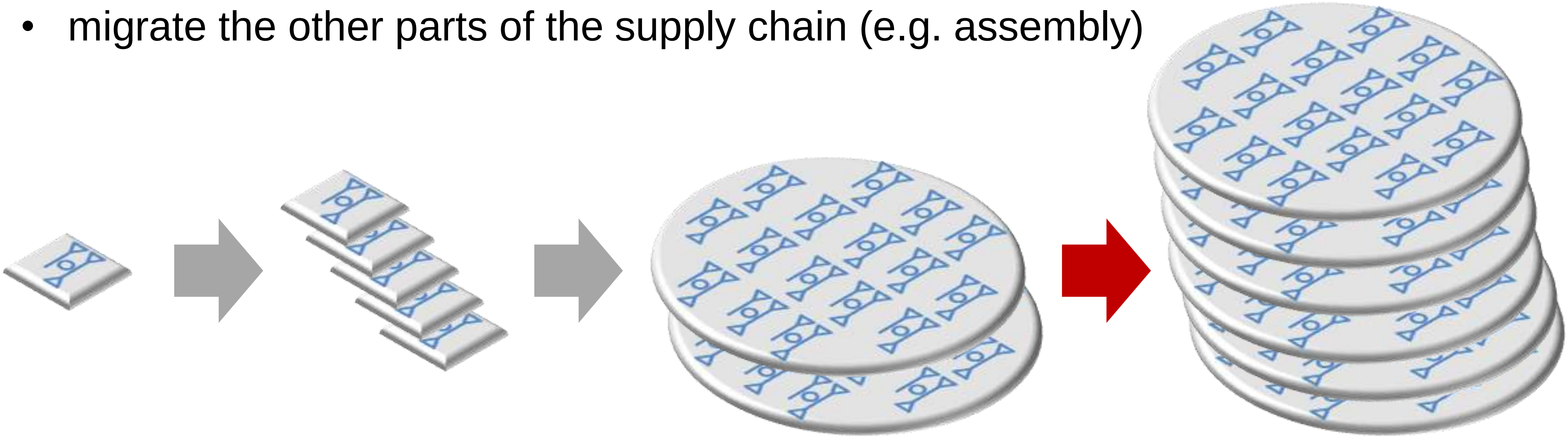
Variational validation
- MPW in research fabs
- multiple samples
- develop packaging

High volume production
- Dedicated run in volume fab

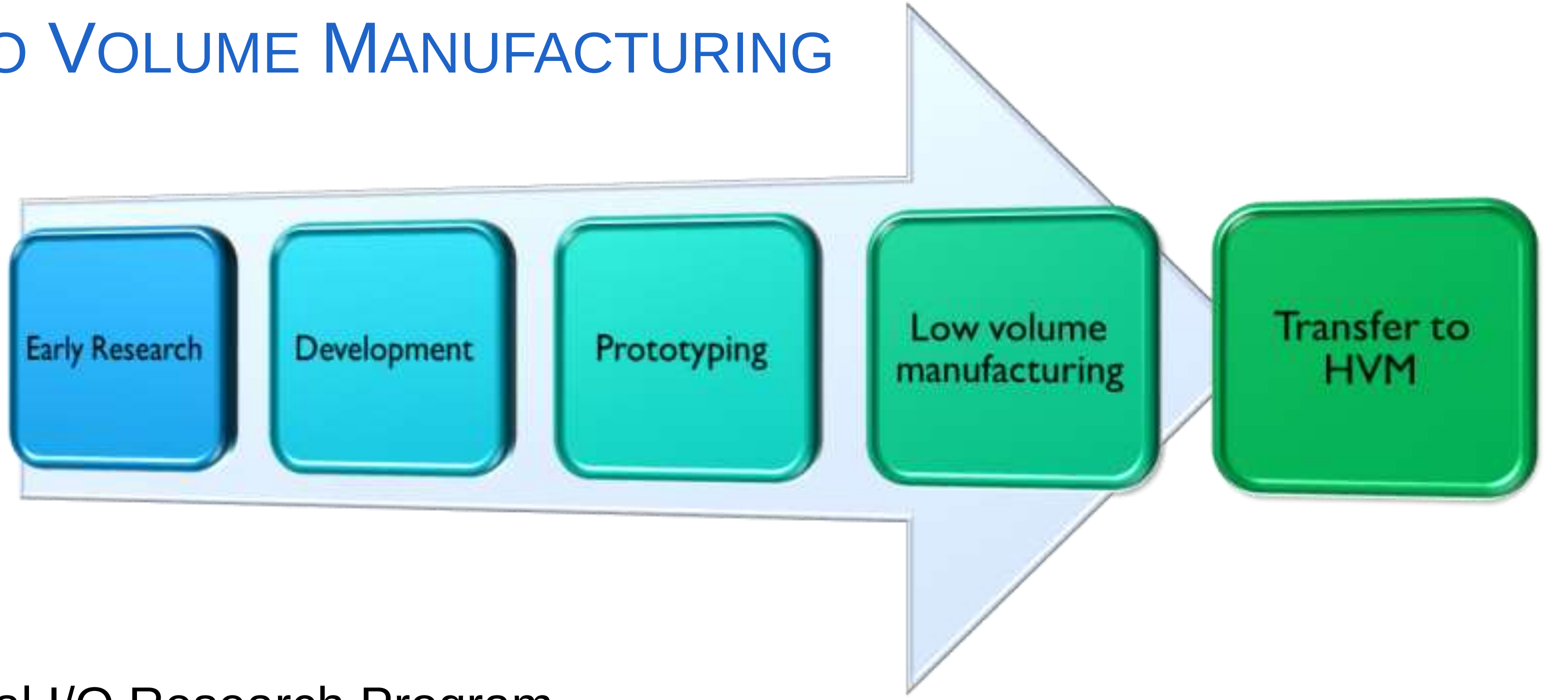
Scaling to High-volume Production

Process transfer from research fab to commercial fab

- match the geometries
- match the performance (including variability)
- match the design kit and models
- migrate the other parts of the supply chain (e.g. assembly)



IMEC SILICON PHOTONICS: FROM R&D PIPELINE TO VOLUME MANUFACTURING



Early Research in imec’s Optical I/O Research Program

Development & Prototyping at imec

- Limited amount of wafers/year
- Reliability qualification ongoing

High-Volume Manufacturing at Commercial Foundry

- imec enables production path at commercial foundry
  - 95% of the flow compatible with CMOS90 technology

FROM SAMPLING TO LOW-VOLUME PRODUCTION

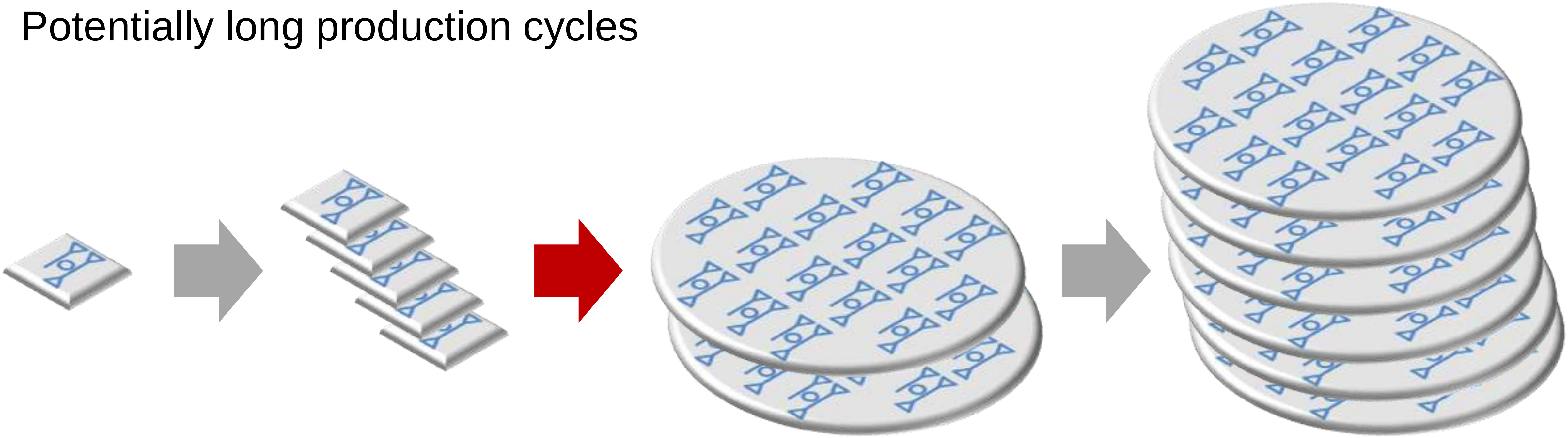
Most Research Fabs (MEC, LETI, IME) offer a LVM model

Low volume (< 1000 wafers / year) can already be enough for first market

Low technology threshold

Potentially high financial threshold (research fabs are expensive per chip)

Potentially long production cycles

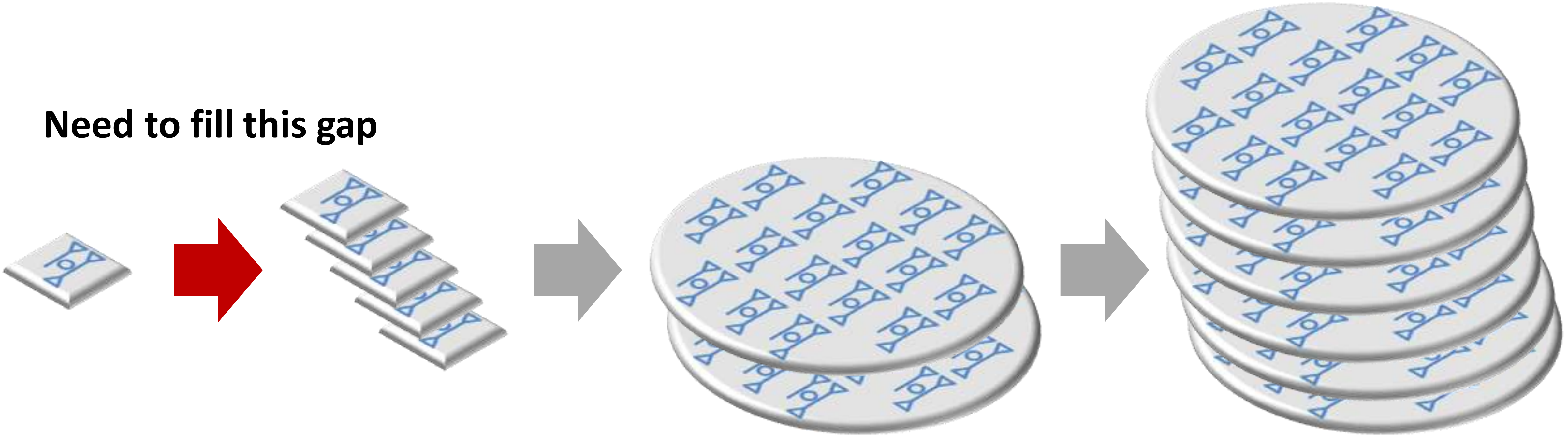


From prototypes to Low-volume sampling

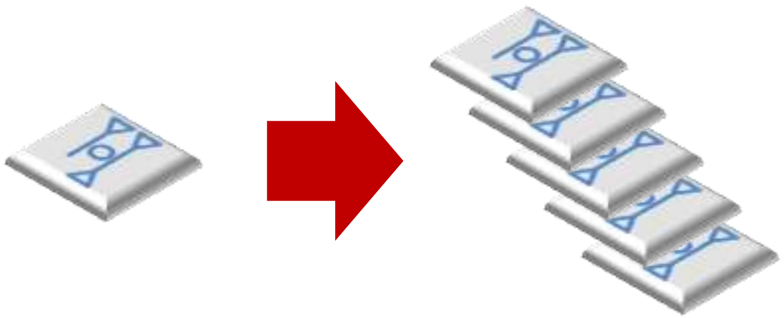
What you need is

1. a quick turn-around time (rapid learning)
2. run-to-run reproducibility
3. realistic expectation for scaling up

Uni lab	MPW
	
	
	



FROM PROTOTYPES TO LOW-VOLUME SAMPLING



Fast prototyping fabs, compatible with MPW fabs

- Fast (days or weeks instead of months)
- Very low volume (1-10 chips)
- Calibrated against an MPW fab
  - Similar processes and specs
  - Similar design flow and design rules
- Consistent quality (monitored process)
- Supported by PDK with models and statistics
- At a similar cost <u>per run</u>

SiP Prototyping services are emerging

IPH, AMO (Germany)

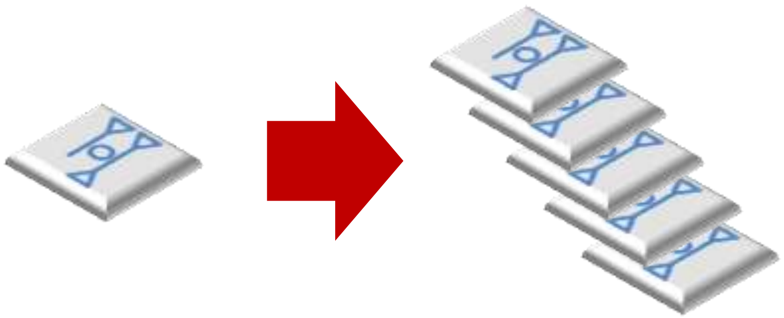
Australia Silicon Photonics

ORC in Southampton (UK)

KIT (Germany)

UBC / UWashington (Canada/US)

Applied NT (Canada)



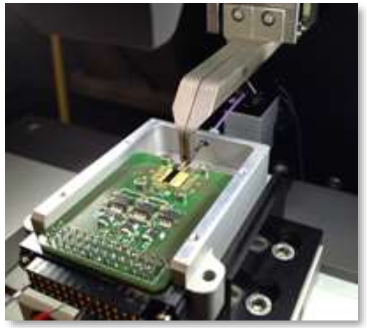
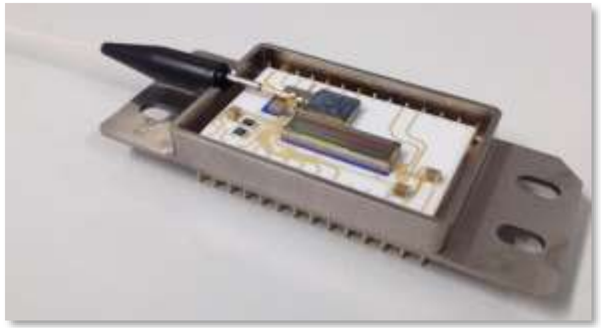
YOU NEED MORE THAN JUST A FAB

- Design and simulation tools (and services): the supply chain is developing

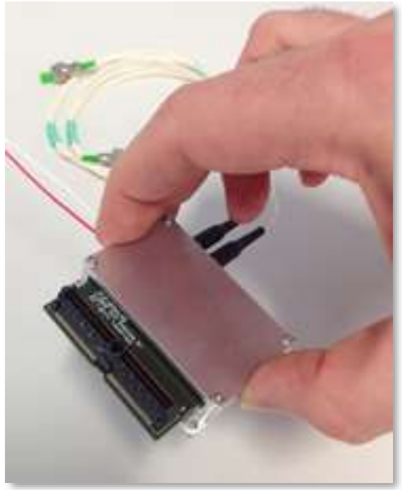
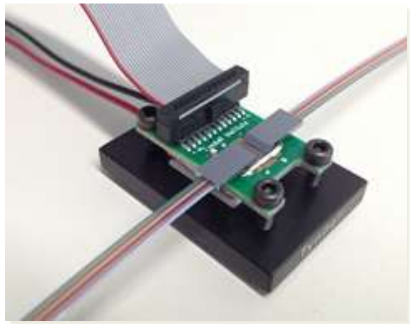
- Packaging tools: rapid progress but still a long way to go

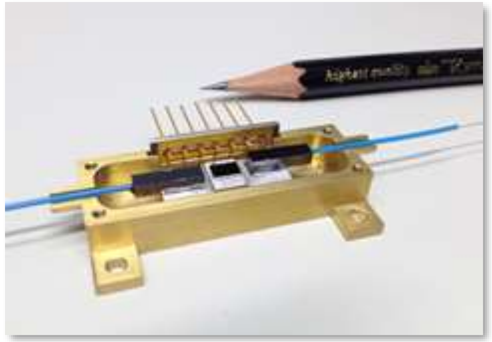
  New H2020 PIC-packaging project will develop the supply chain

PIC PACKAGING @ TYNDALL





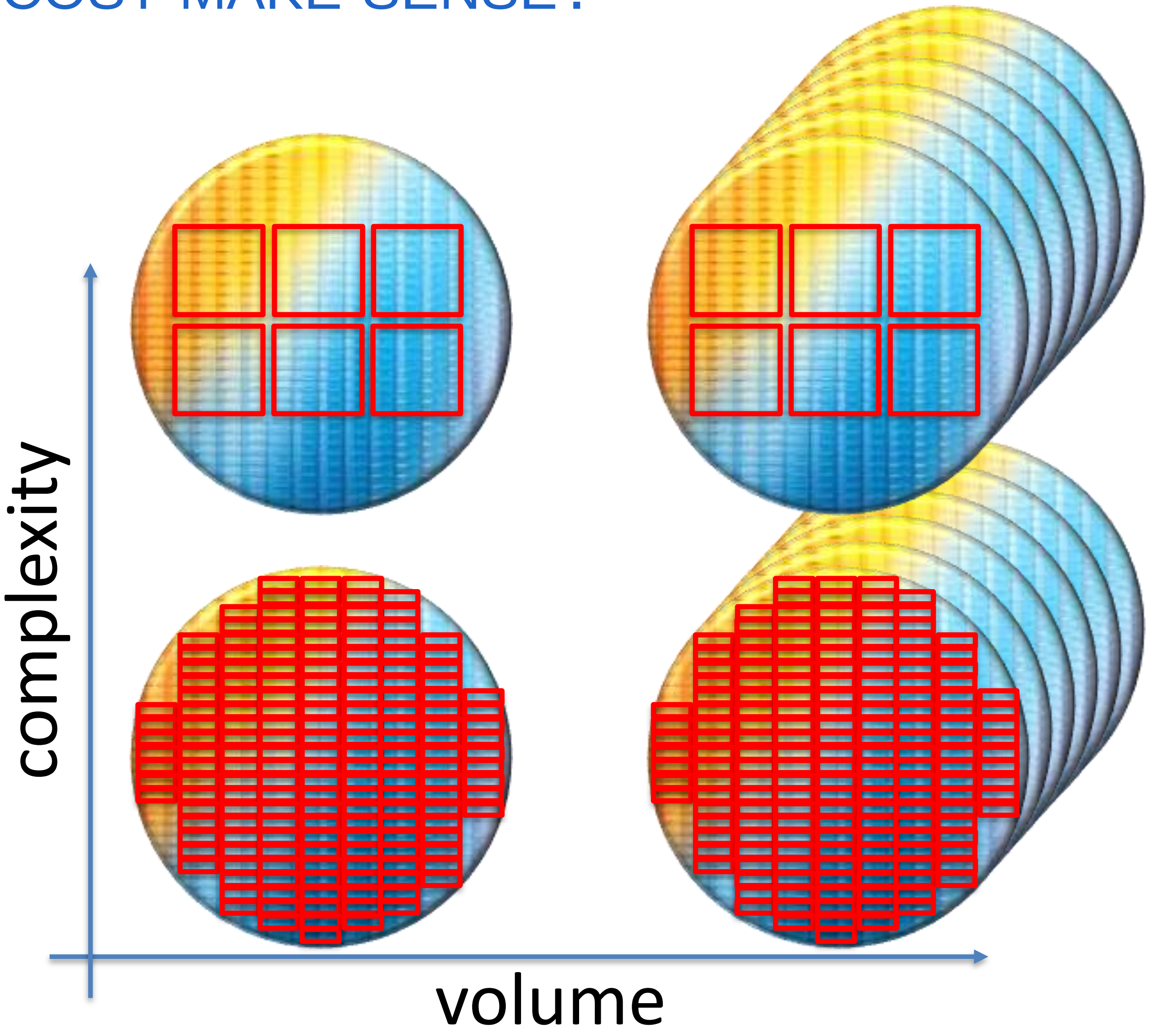

When does this functionality/cost make sense?

Large Volume

- millions of chips
- high yield
- low cost

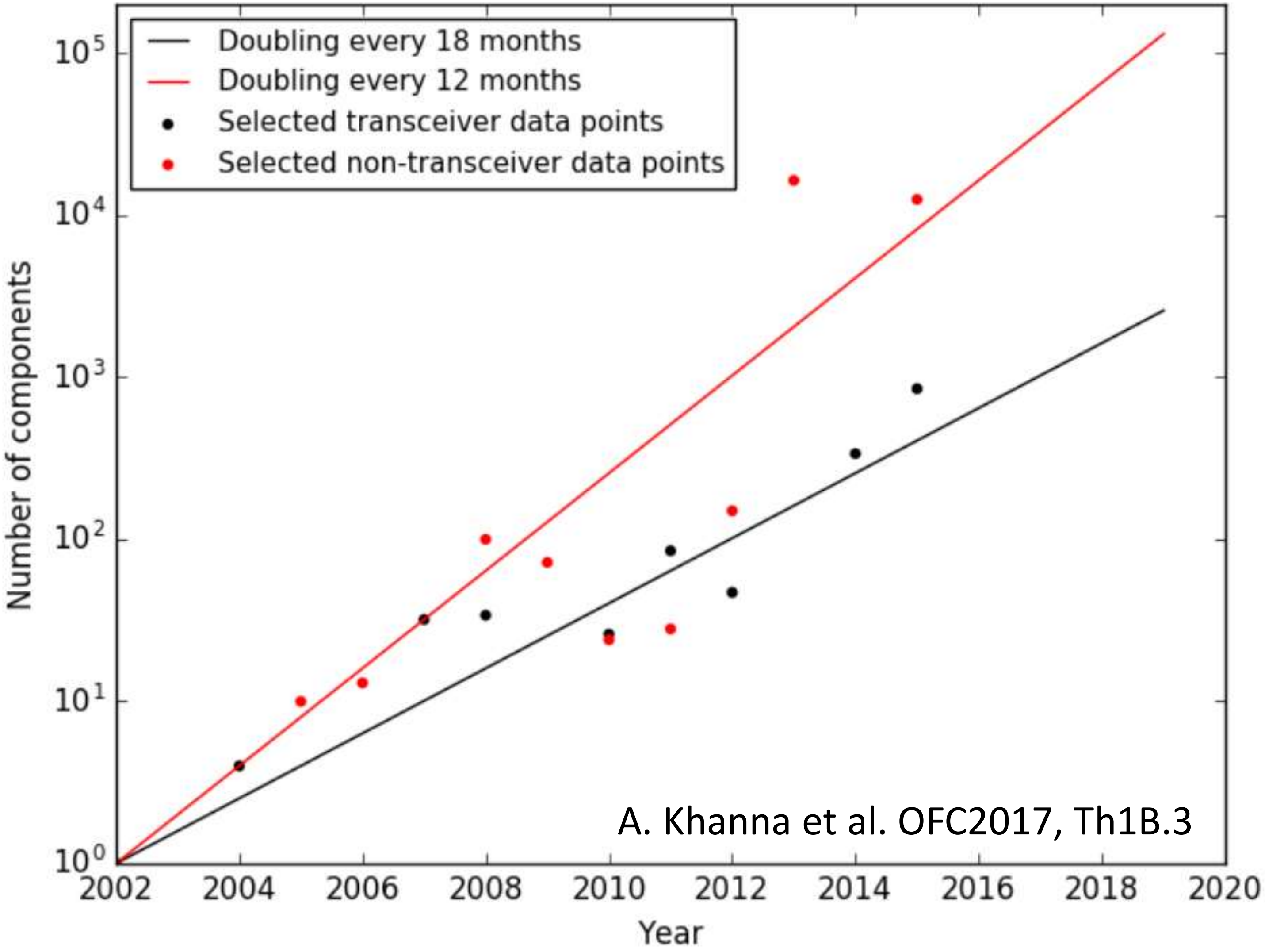
High complexity

- thousands of functions on a chip
- large-scale integration
- high cost
- yield?



COMPONENTS PER CHIP

"Moore's law for Silicon Photonics"

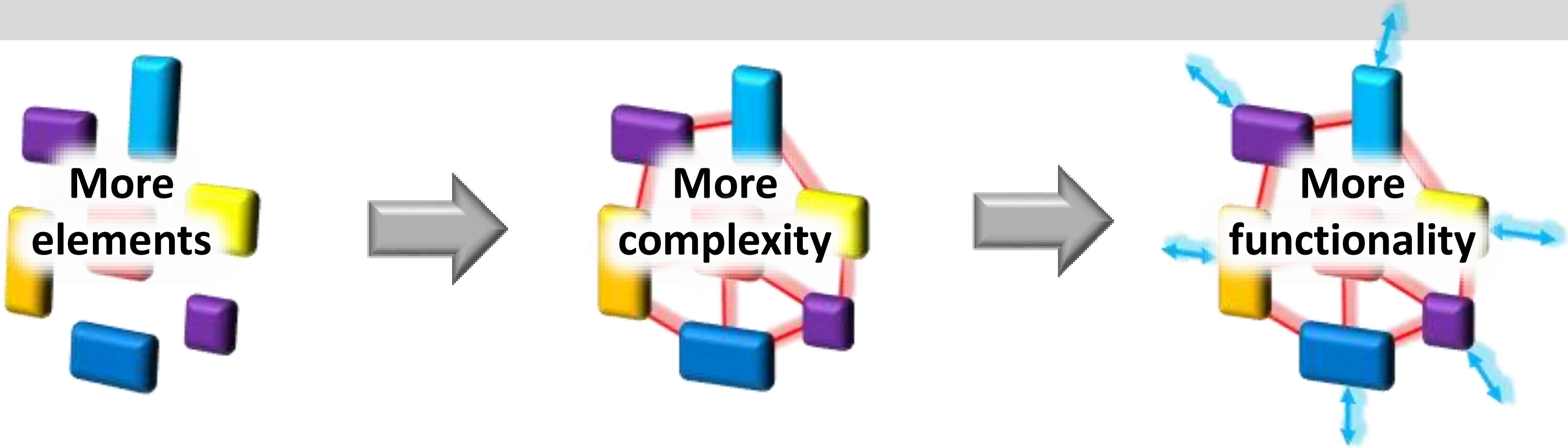


CONNECTIVITY BEGETS COMPLEXITY BEGETS FUNCTIONALITY

Integrated Electronics

- billions of digital gates: unprecedented logic performance
- millions of analog transistors: unprecedented control

(even with imperfect components: enabled by design!)



Integrated Photonics (in Silicon)

- **technological potential** of 10000+ photonic elements on a chip
- not even scratched the surface of what this could do

Needs design and control

SCALING COMPLEXITY

Many components on a chip

Scalable building blocks

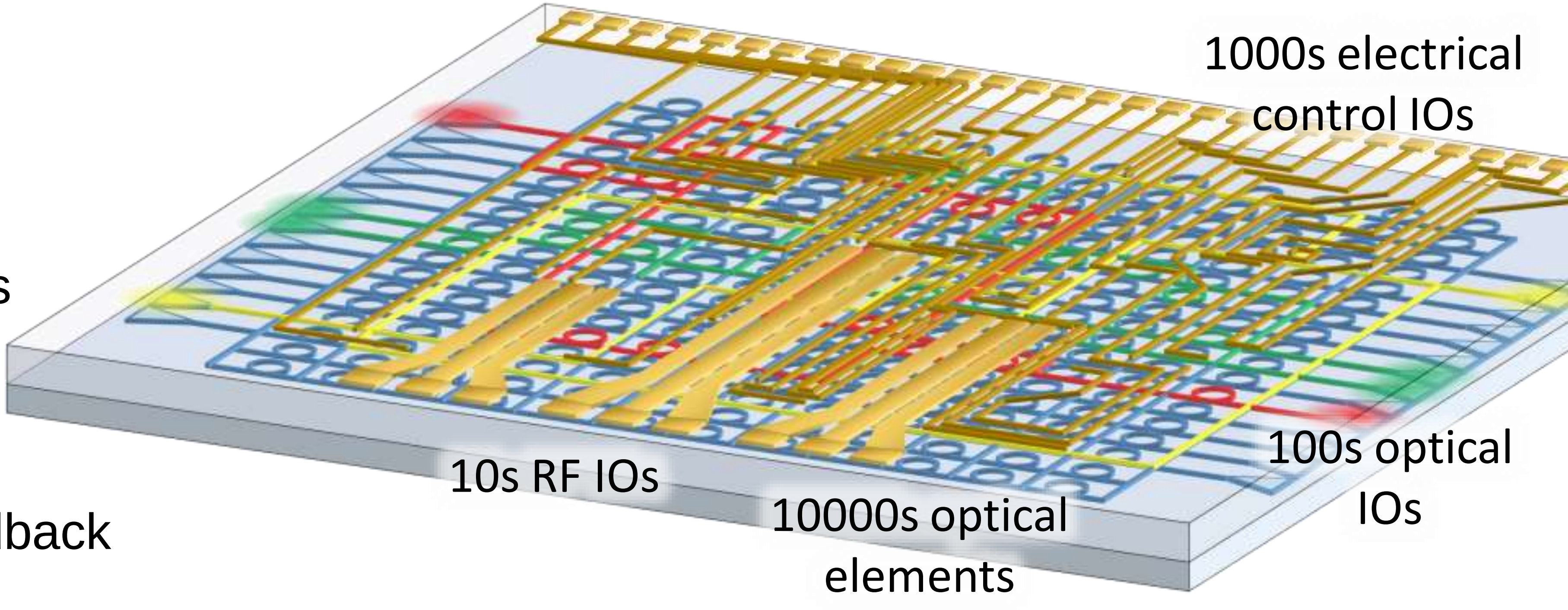
- connectivity
- cascadability
- variability

Design scaling

- synthesis tools
- accurate models
- yield prediction

Operational scaling

- control and feedback



SCALING COMPLEXITY

Many components on a chip

Scalable building blocks

- connectivity
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Design scaling

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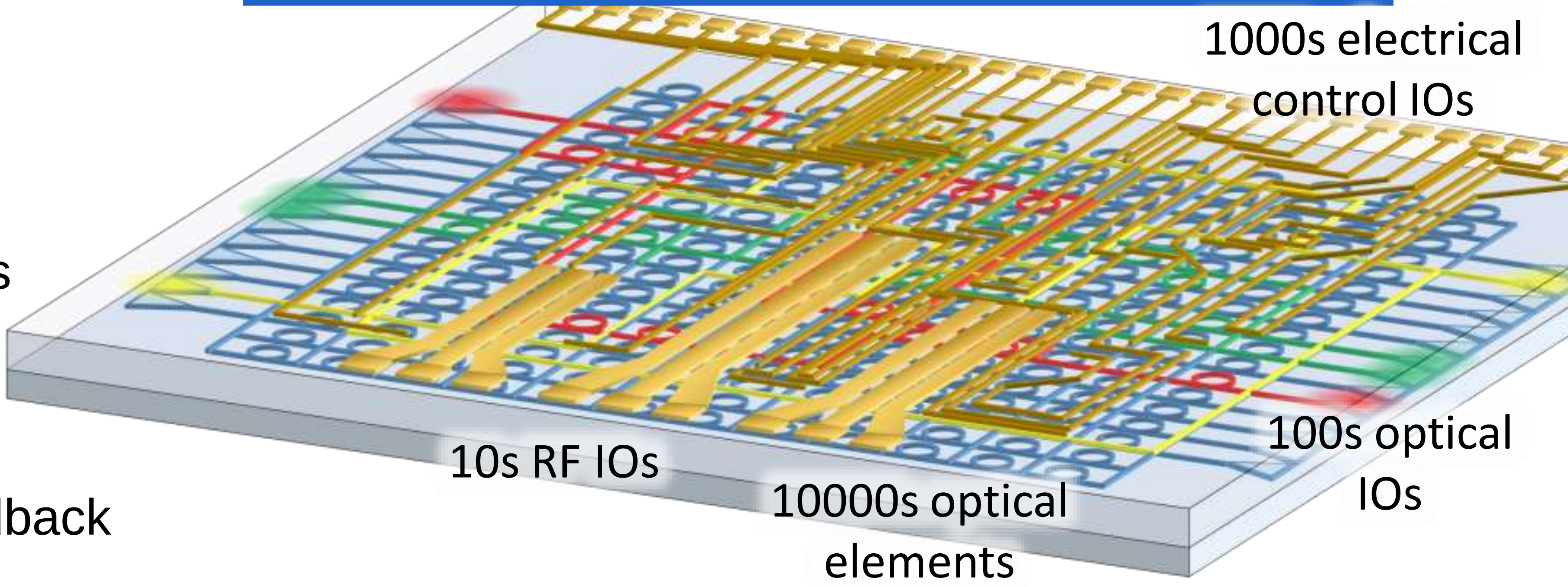
- accurate models
- yield prediction

Operational scaling

- control and feedback

How many devices can we combine in a circuit?

Footprint
Power consumption
Compound losses (or add gain?)
Parasitics and crosstalk



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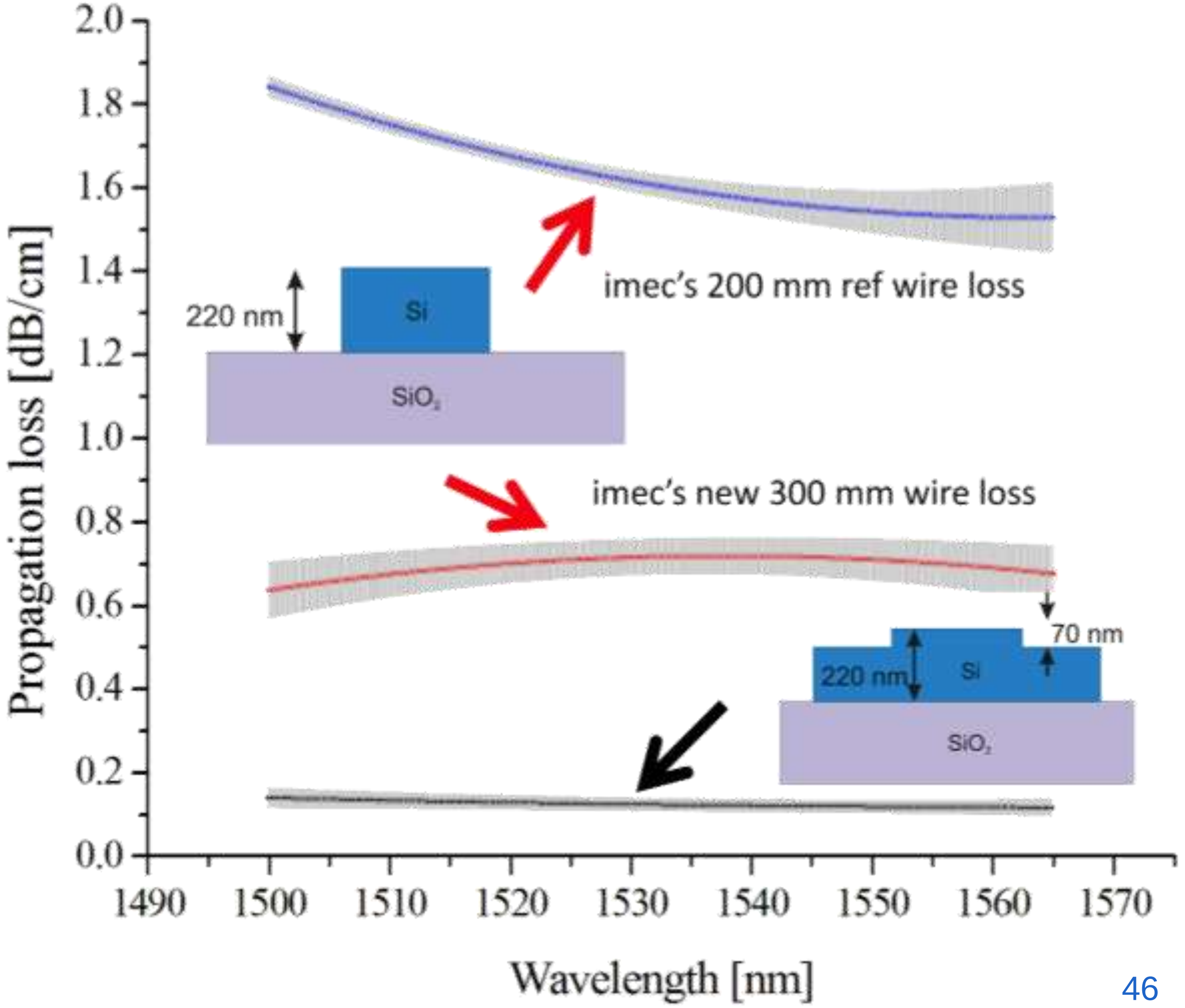
Lower losses.

Better technology

- 300mm wafers and tools give better performance
- immersion lithography gives better linewidth control
- lower sidewall roughtness reduces loss and backreflection

Other geometries and materials

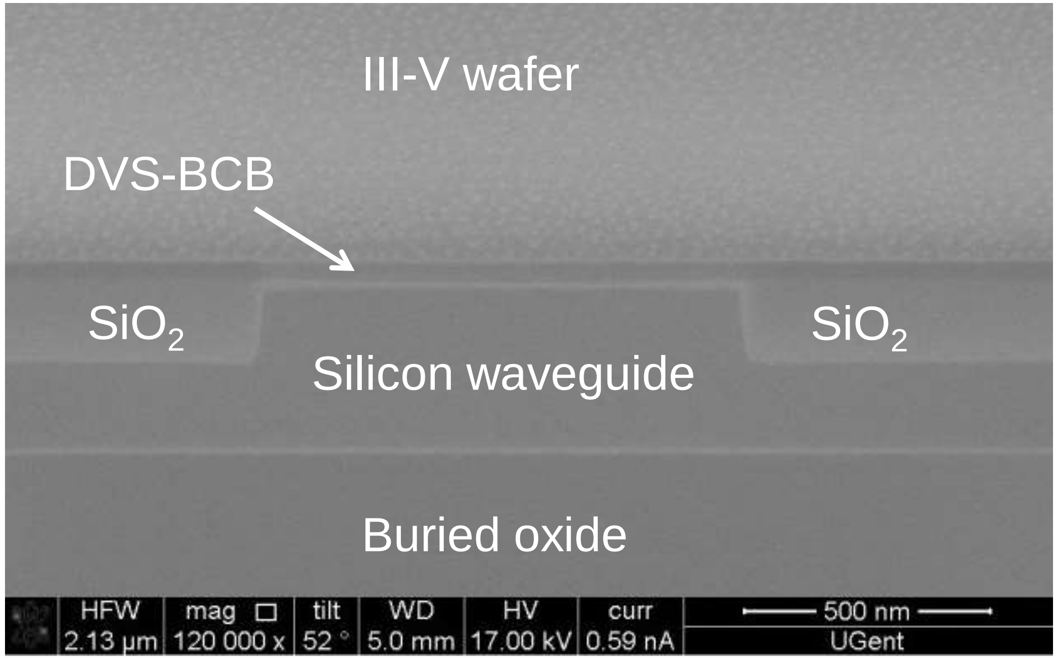
- rib waveguides
- SiN waveguides

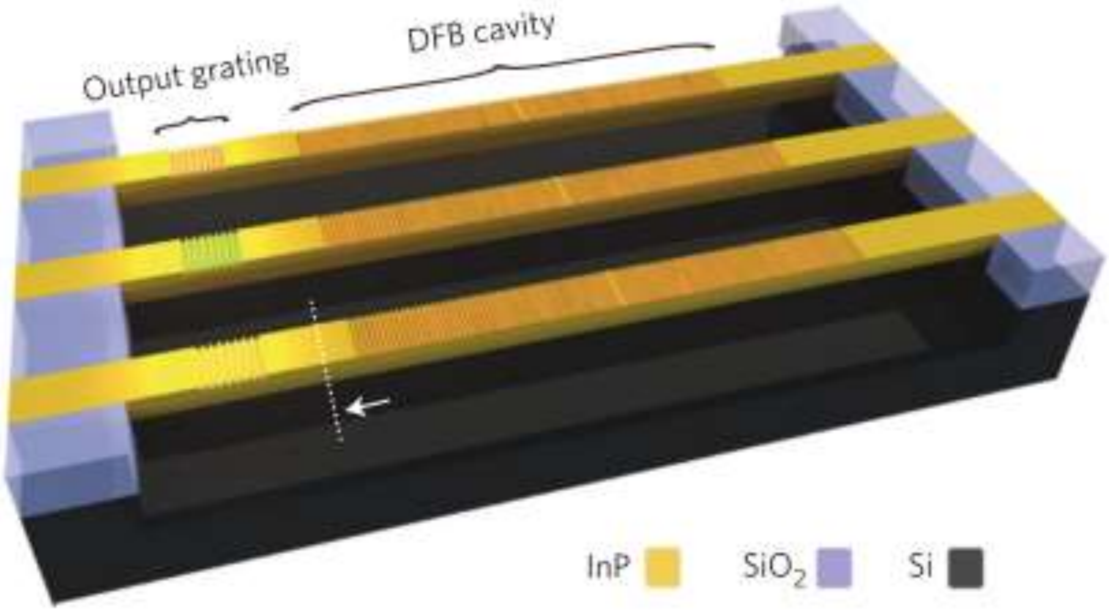


LOSS COMPENSATION

Introduce Gain in silicon photonics

- III-V semiconductors
  - Bonding
  - Epitaxy
- Germanium
- Erbium-doped waveguide amplifiers
- Parametric gain (4-wave mixing)





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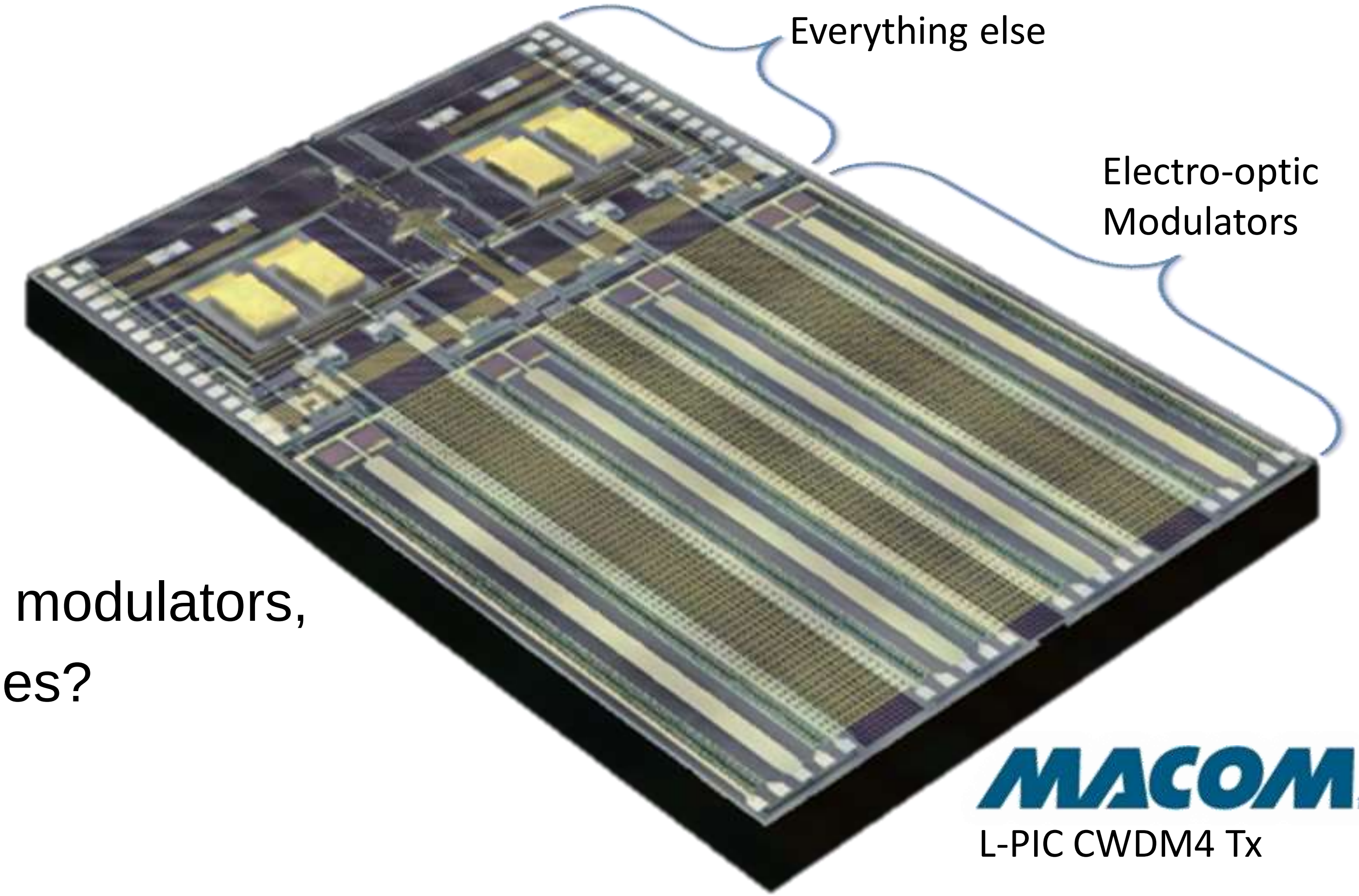
Modulators consume a lot of space

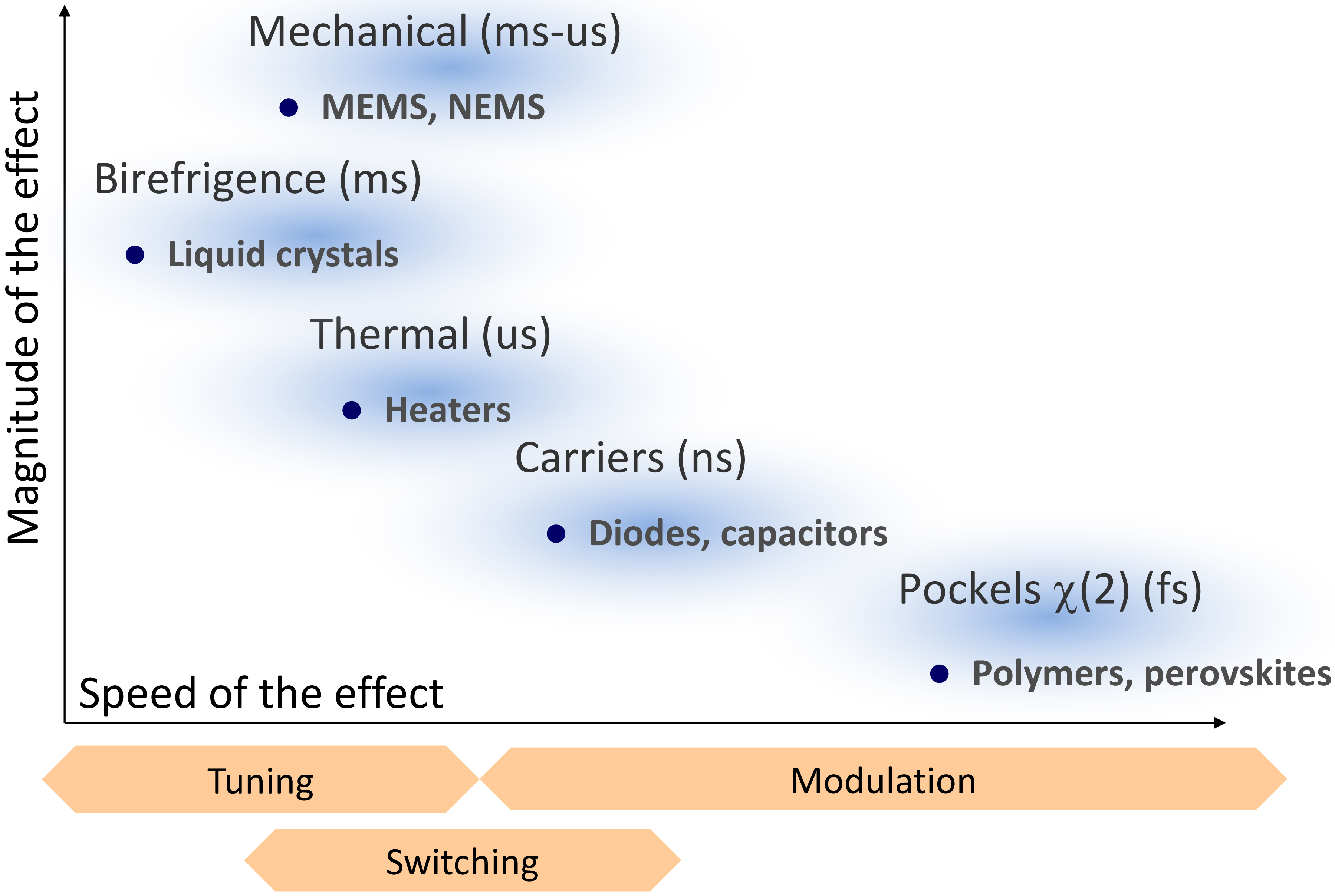
Not really in line with 'submicron' Silicon Photonics



Alternative phase modulators, tuners and switches?

MACOM
L-PIC CWDM4 Tx

EFFECT MAGNITUDE VS. SPEED



Alternative Modulator and Switch Technologies

Modulators

Electro-Optic Polymers in Slot Waveguides

- Very good performance, but ready as a platform?

Ferro-Electrics on Silicon

- Pure phase modulation
- difficult material integration
- Recent breakthroughs in loss

Germanium-EA Absorbers

- Direct intensity modulation, but no phase modulation
- High speed, low power demonstrated

Graphene on Silicon

- Direct intensity modulation
- Much work needed

Switches

Large-Scale MEMS Fabrics

- Up to 50x50 switch matrices demonstrated
- Large bandwidth and high XT

Liquid Controlled Adiabatic Switches

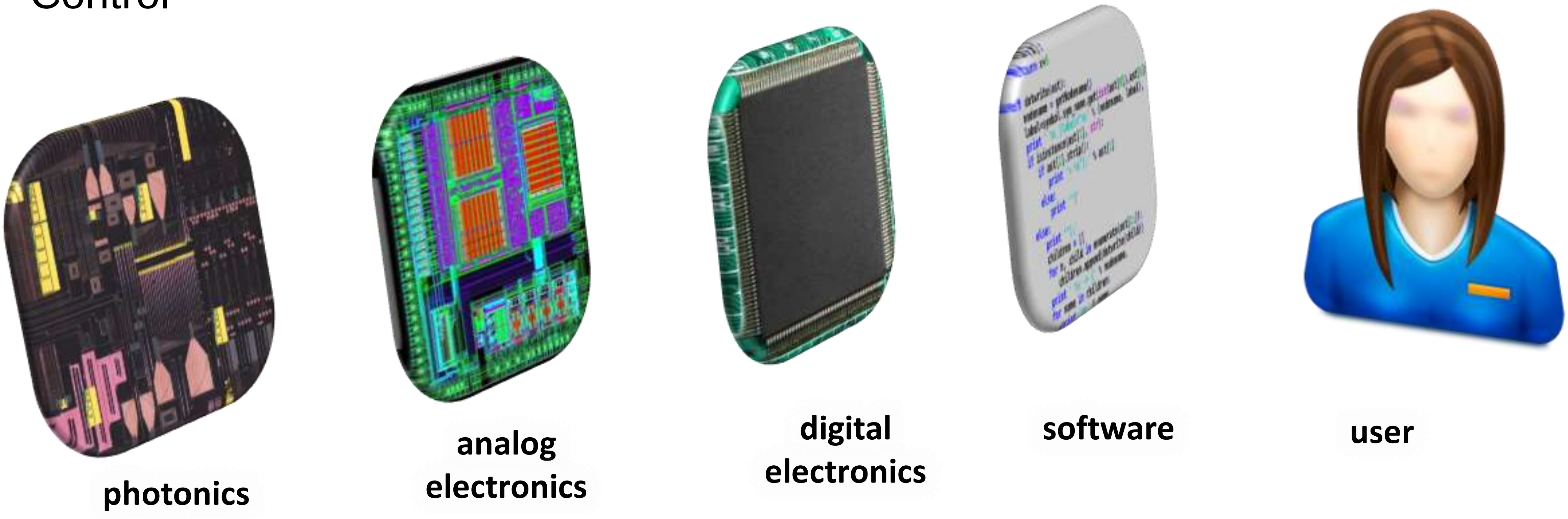
- Towards no static power consumption
- Broadband low loss operation

Liquid Crystal based switches

Photonics is just one part of the system

Large-scale photonics requires integrated electronics

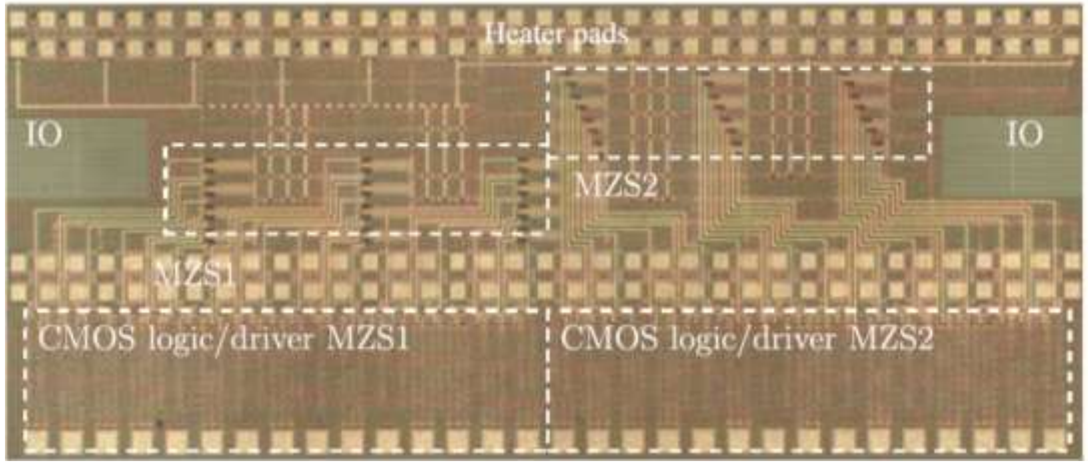
- Logic
- Control



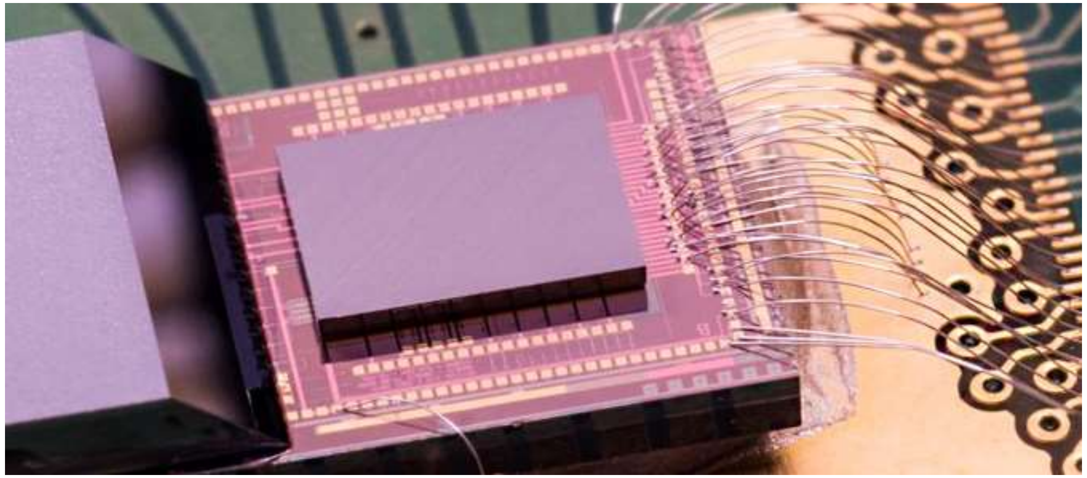
INTEGRATION WITH ELECTRONICS: SCALING

Photonics interfaced with electronics

- Monolithic
    - Low parasitics. all-in-one process.
    - Not the optimal process for either.
    - Feature size mismatch
- Flip-chip
    - Large bond-pads, density limited
    - Parasitics
- 3D stacking
    - Best process for both
    - Co-design and yield?



IBM



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SCALING COMPLEXITY

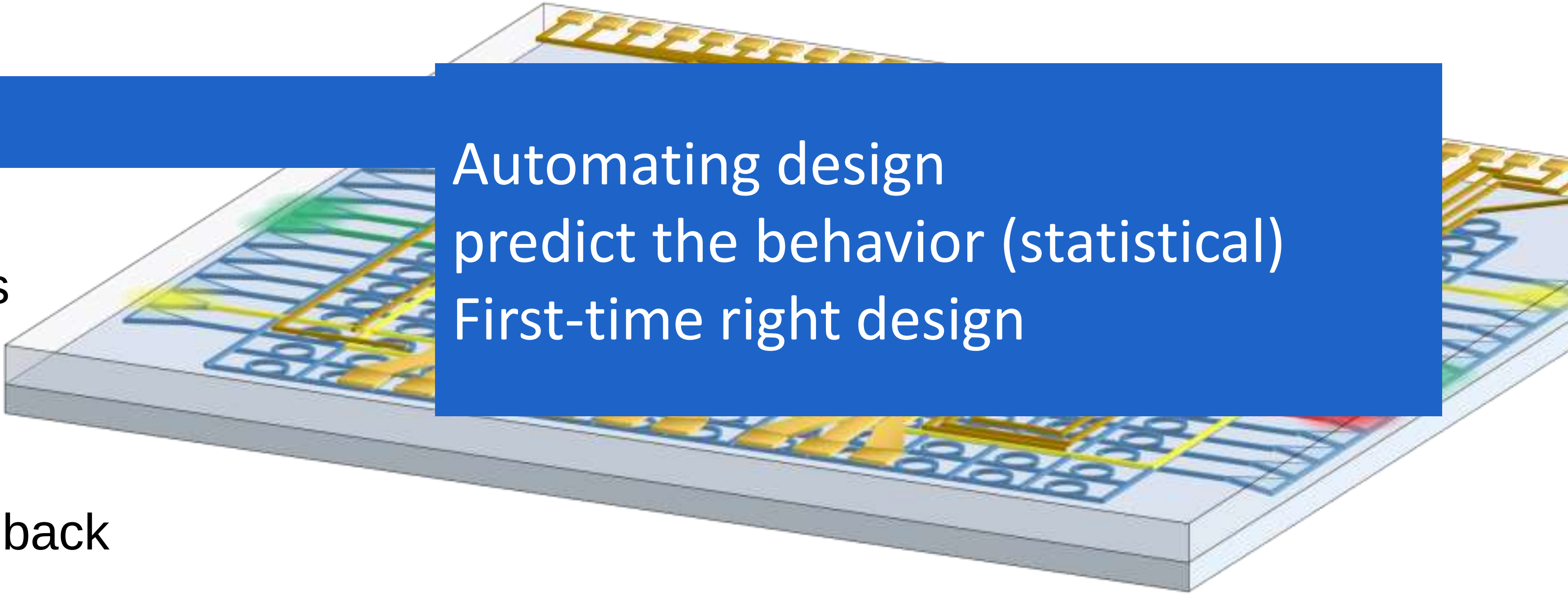
Many components on a chip

Scalable building blocks

- connectivity
- cascadability
- variability

Design scaling

- synthesis tools
- accurate models
- yield prediction



Automating design

predict the behavior (statistical)

First-time right design

Operational scaling

- control and feedback

DESIGNING PHOTONIC INTEGRATED CIRCUITS

Can we learn from electronic ICs?

- Millions of analog transistors
- Billions of digital transistors
- Power, timing and yield
- **First time right designs**

- Very mature Electronic Design Automation (EDA) tools!
- A well established design flow

Does this apply to photonics?

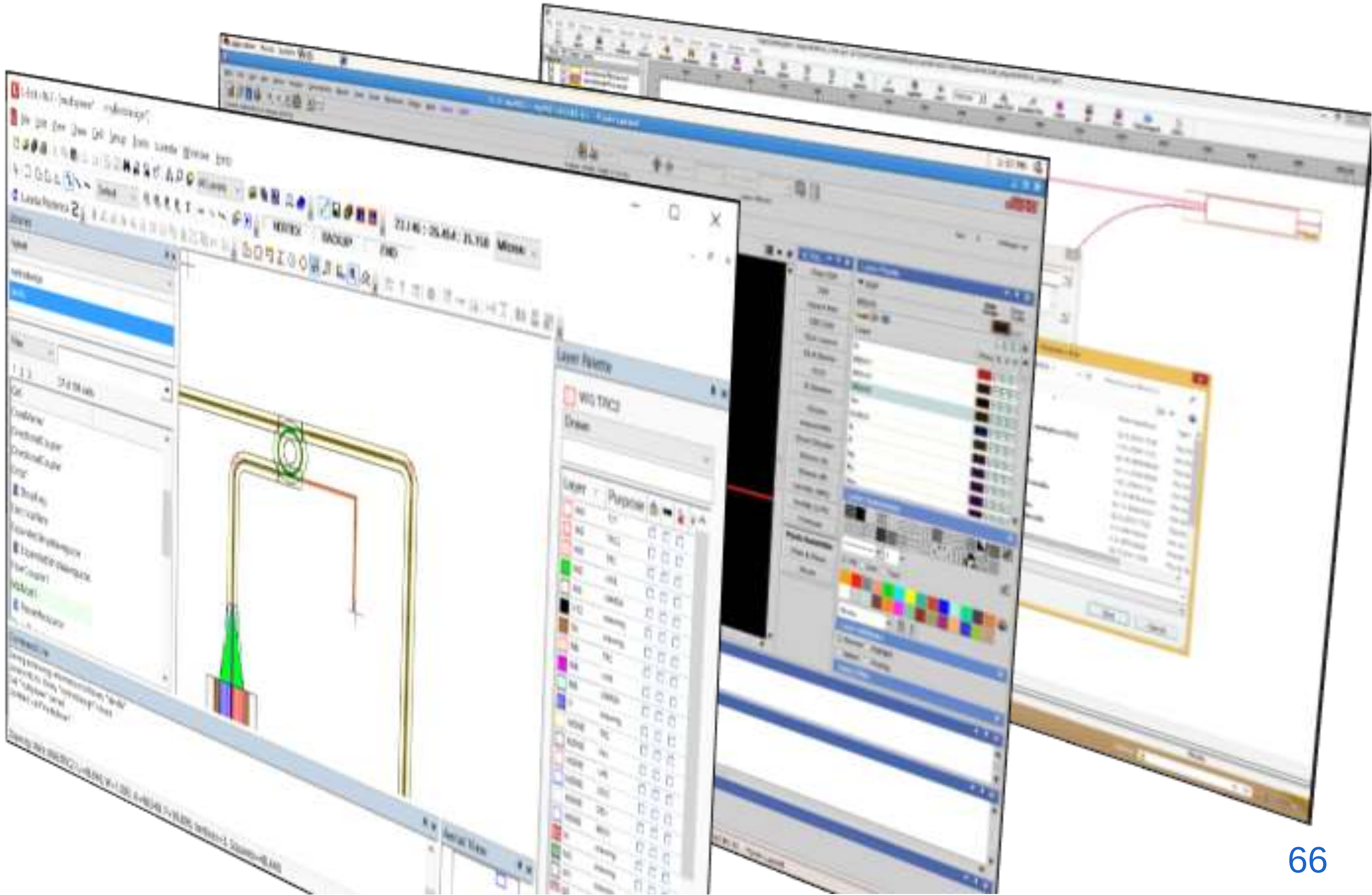
Design Environments are Emerging

Combinations of Photonics Design and EDA

Physical simulation combined with circuit design

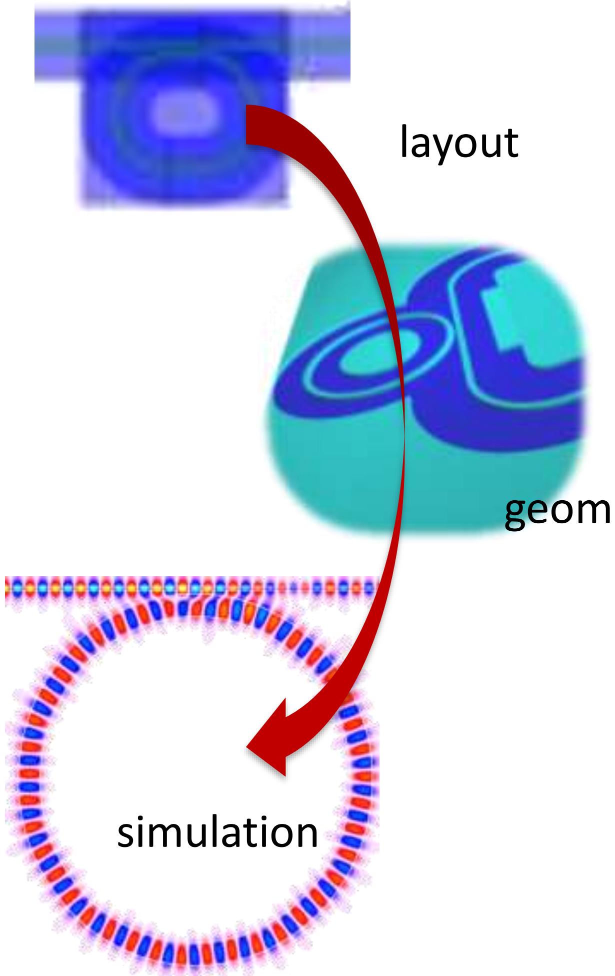
Physical and functional verification

First PDKs with basic models



COMPONENT DESIGN VS. CIRCUIT DESIGN

10 years ago: Component Design



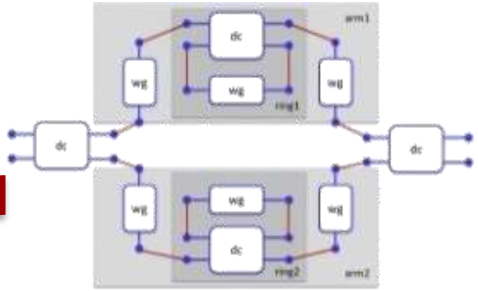
layout

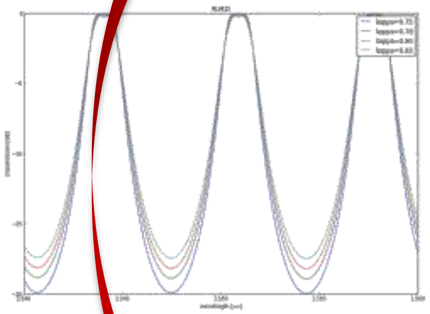
geometry

simulation

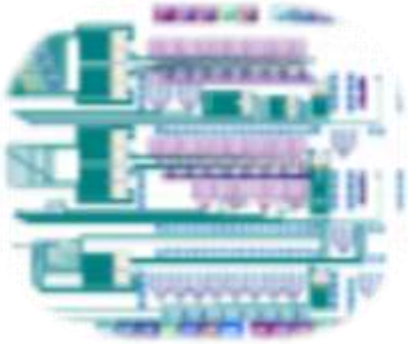
Now also: Circuit design

Circuit capture





simulation



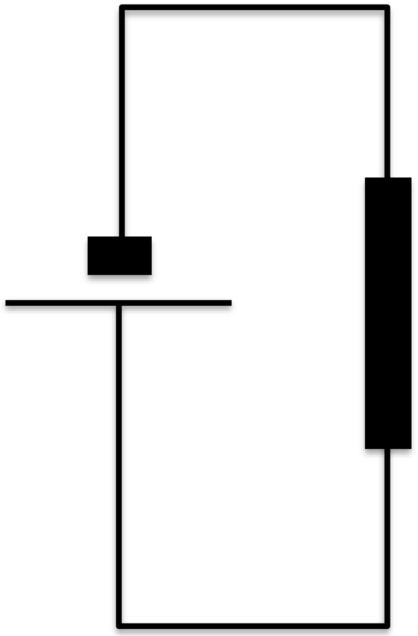
layout

PHOTONIC+ELECTRONIC CIRCUIT SIMULATION

Photonics does not fit in Spice

Effort-flow systems

Electrical	Voltage	Current
Fluidic	Pressure	Flow
Thermal	Temperature	Heat Flow*
Mechanical	Force	Motion
Photonic?	-	-

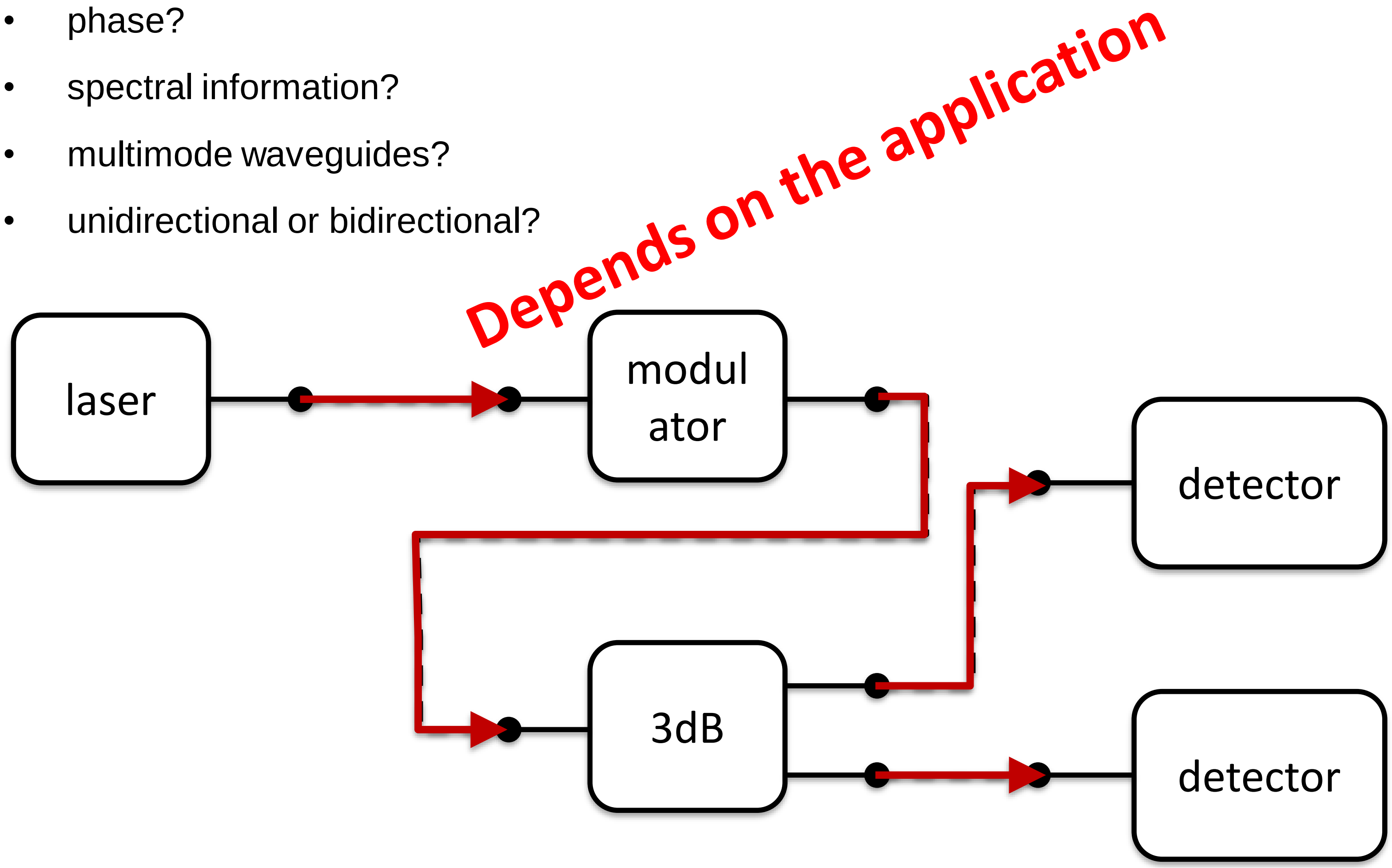


Photonics used other formalisms (more like RF waves)

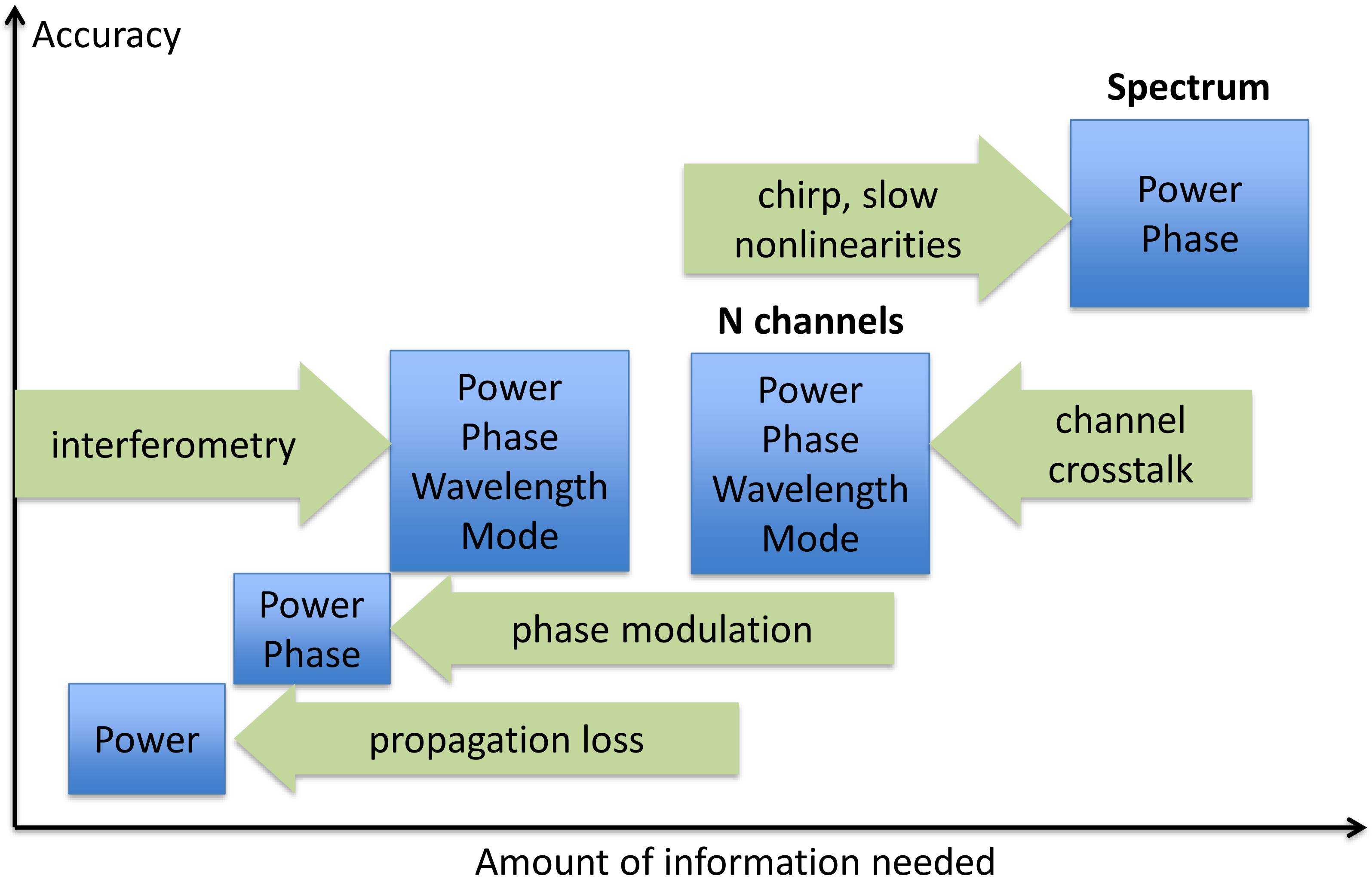
SIGNALS IN A PHOTONIC CIRCUIT

How much information needs to be exchanged per time step?

- phase?
- spectral information?
- multimode waveguides?
- unidirectional or bidirectional?



SIGNAL REPRESENTATION: EFFECTS CAN BE MODELED



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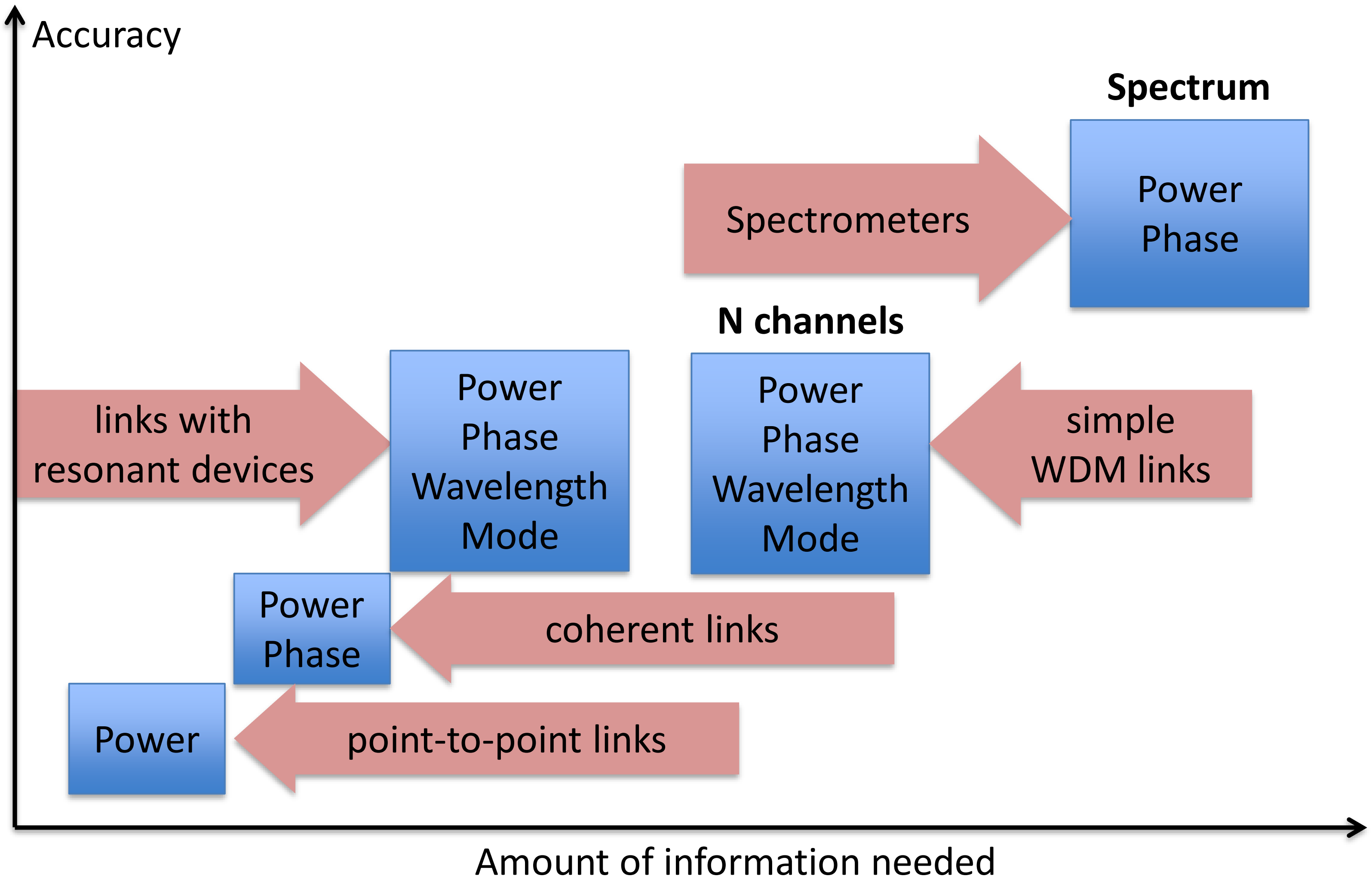
SIGNAL REPRESENTATION: APPLICATION DESIGN

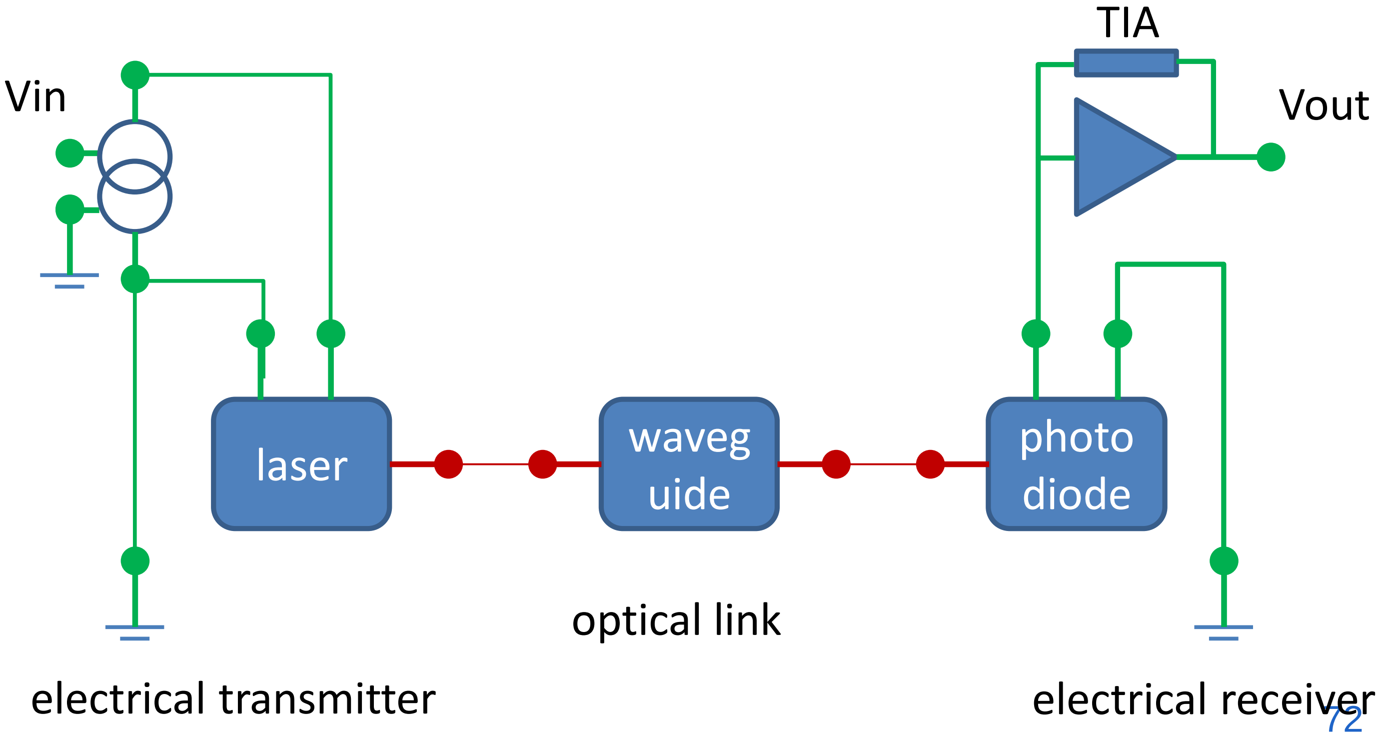


Integrate Photonic and Electronic circuit simulation

Photonics = Optics + Electronics.

We need to combine the two in the design process.

- Verilog A: Represent Optical Signals as ‘Voltages’ or ‘Power’
- Use busses for power, phase (real/imag) and wavelength
- Cosimulation with Photonic Circuit simulator

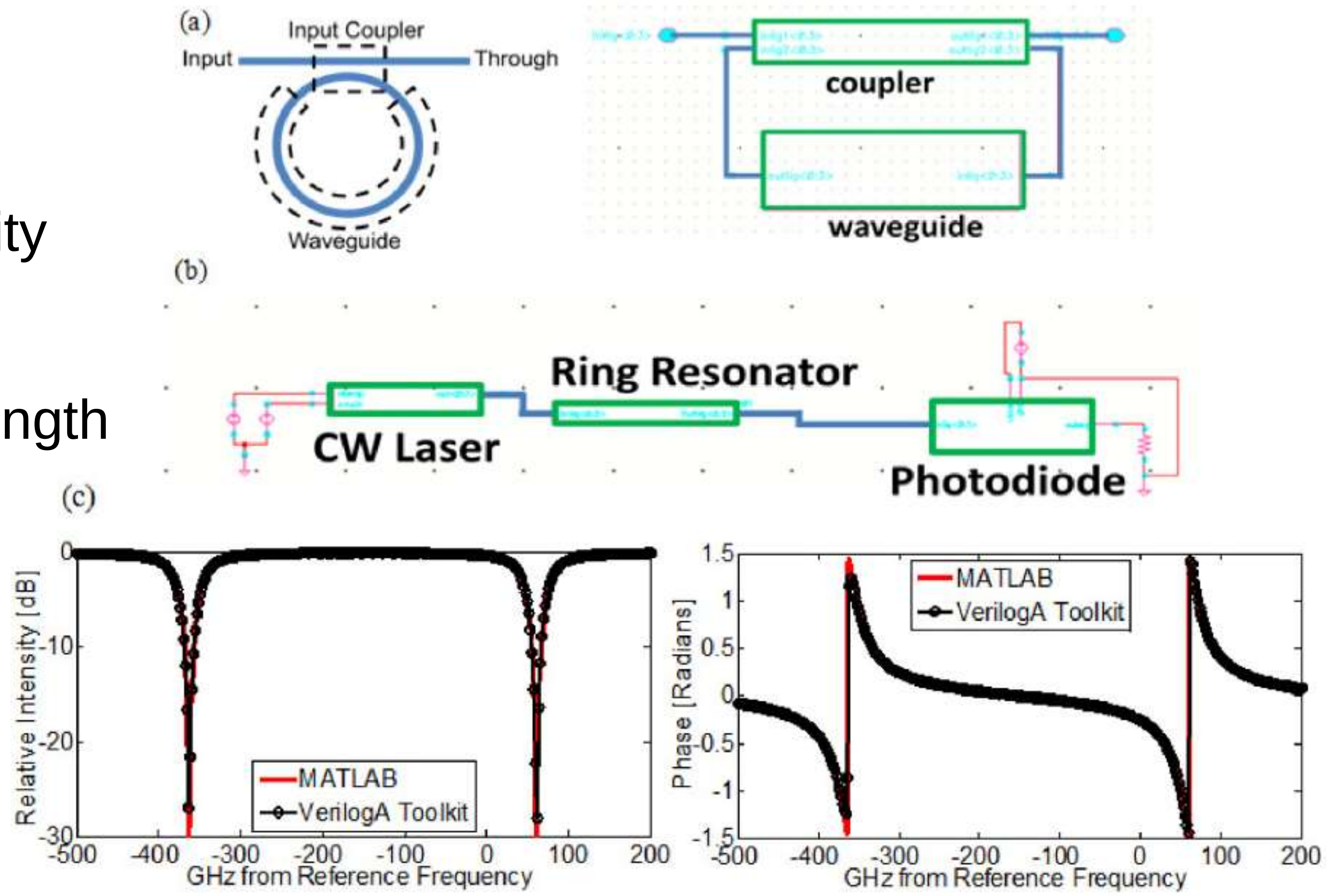


Photonics in VerilogA

Encode time signals as 'analytical' signals (complex numbers)

Bus of two lines for bidirectionality

Modulation on an optical wavelength

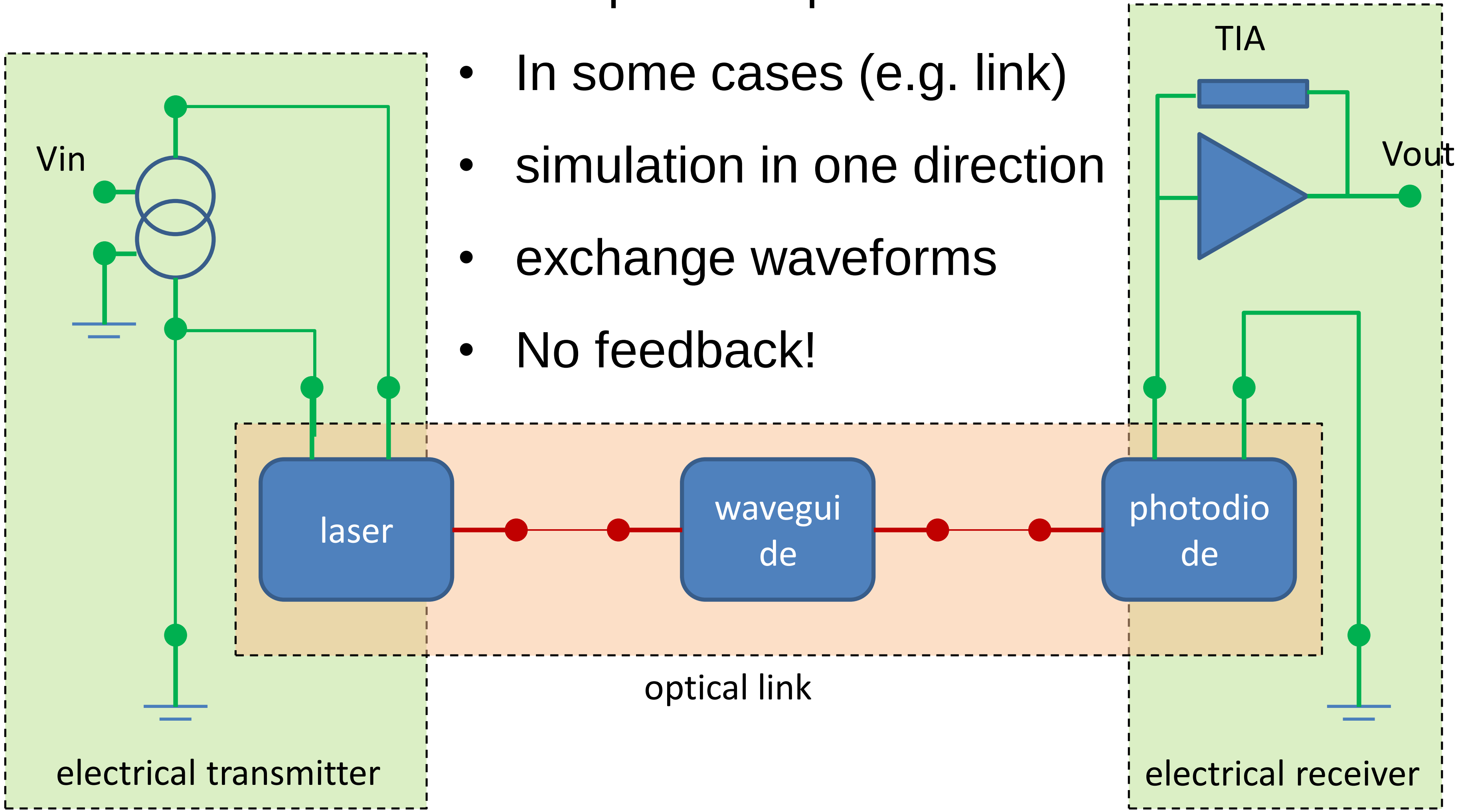


C. Sorace-Agaskar, OpEx 23(21), 2015

PHOTONIC-ELECTRONIC COSIMULATION

Full separation possible?

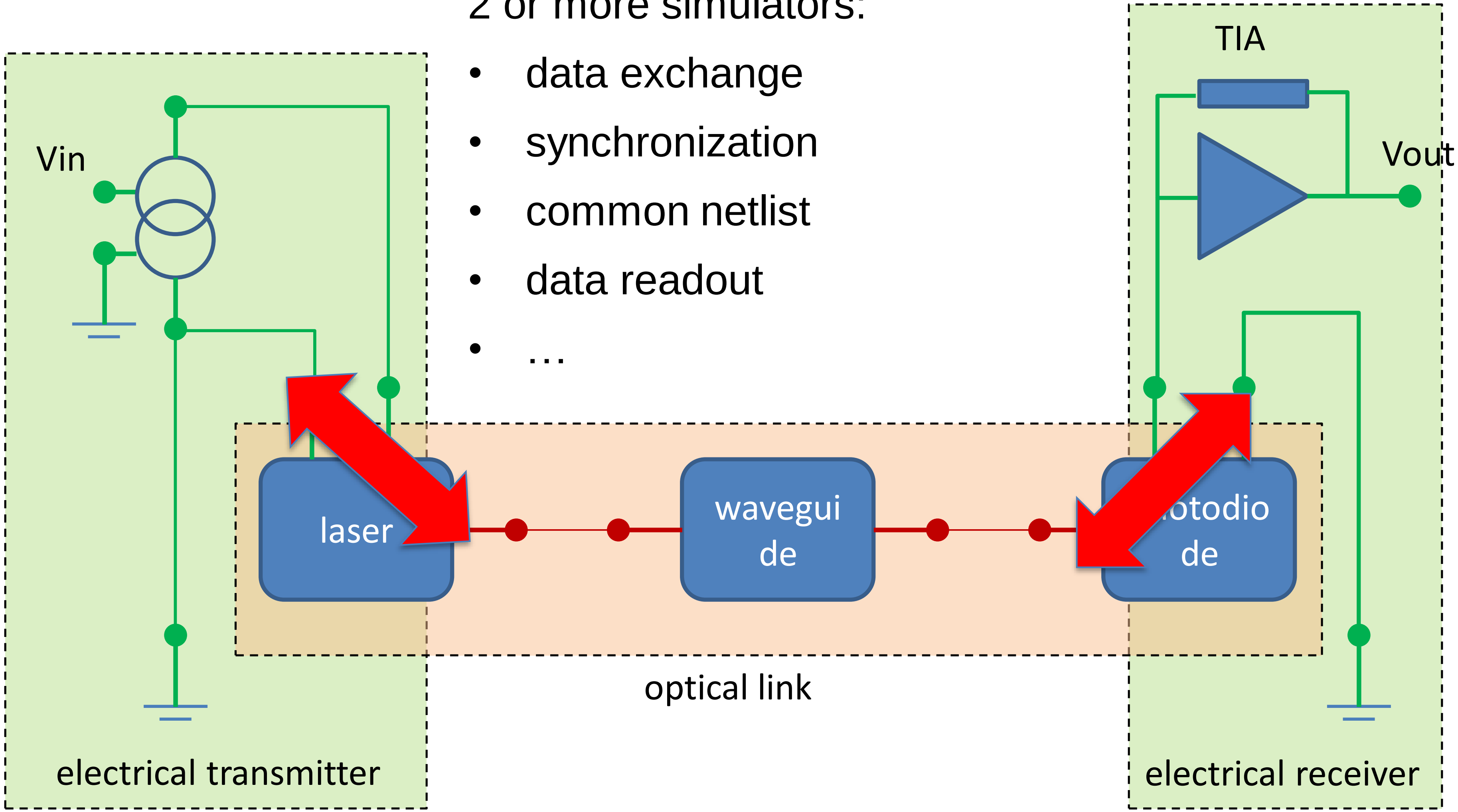
- In some cases (e.g. link)
- simulation in one direction
- exchange waveforms
- No feedback!



Future: Mixed-signal co-simulation

2 or more simulators:

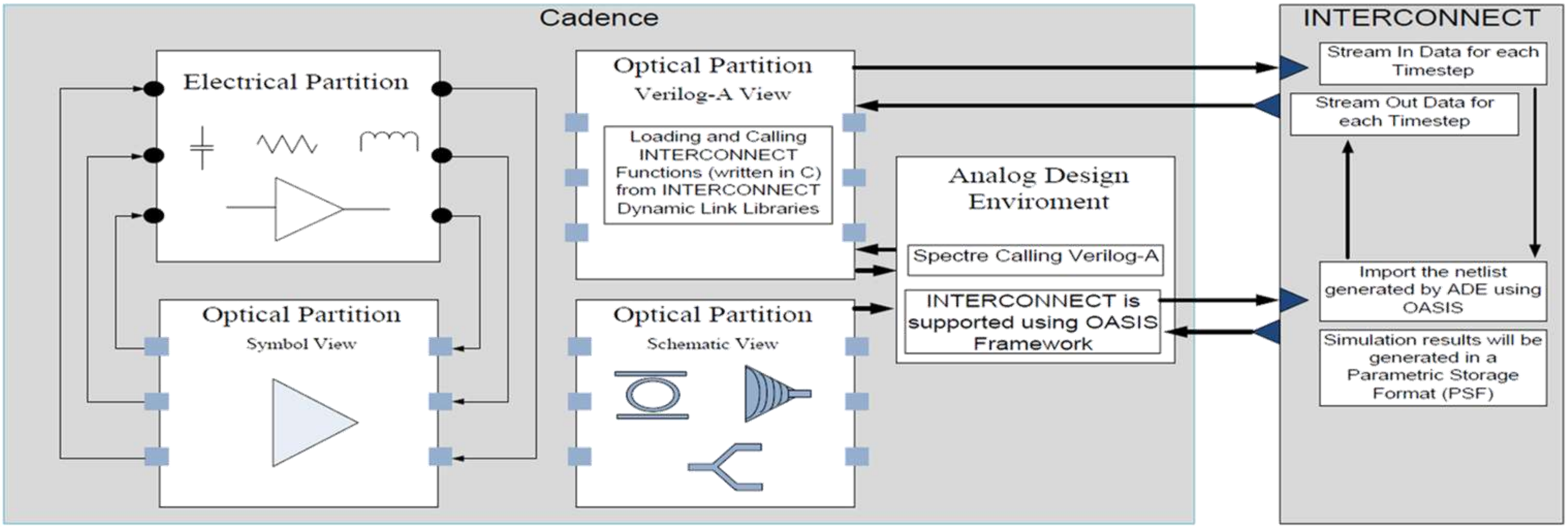
- data exchange
- synchronization
- common netlist
- data readout
- …



CO-SIMULATION

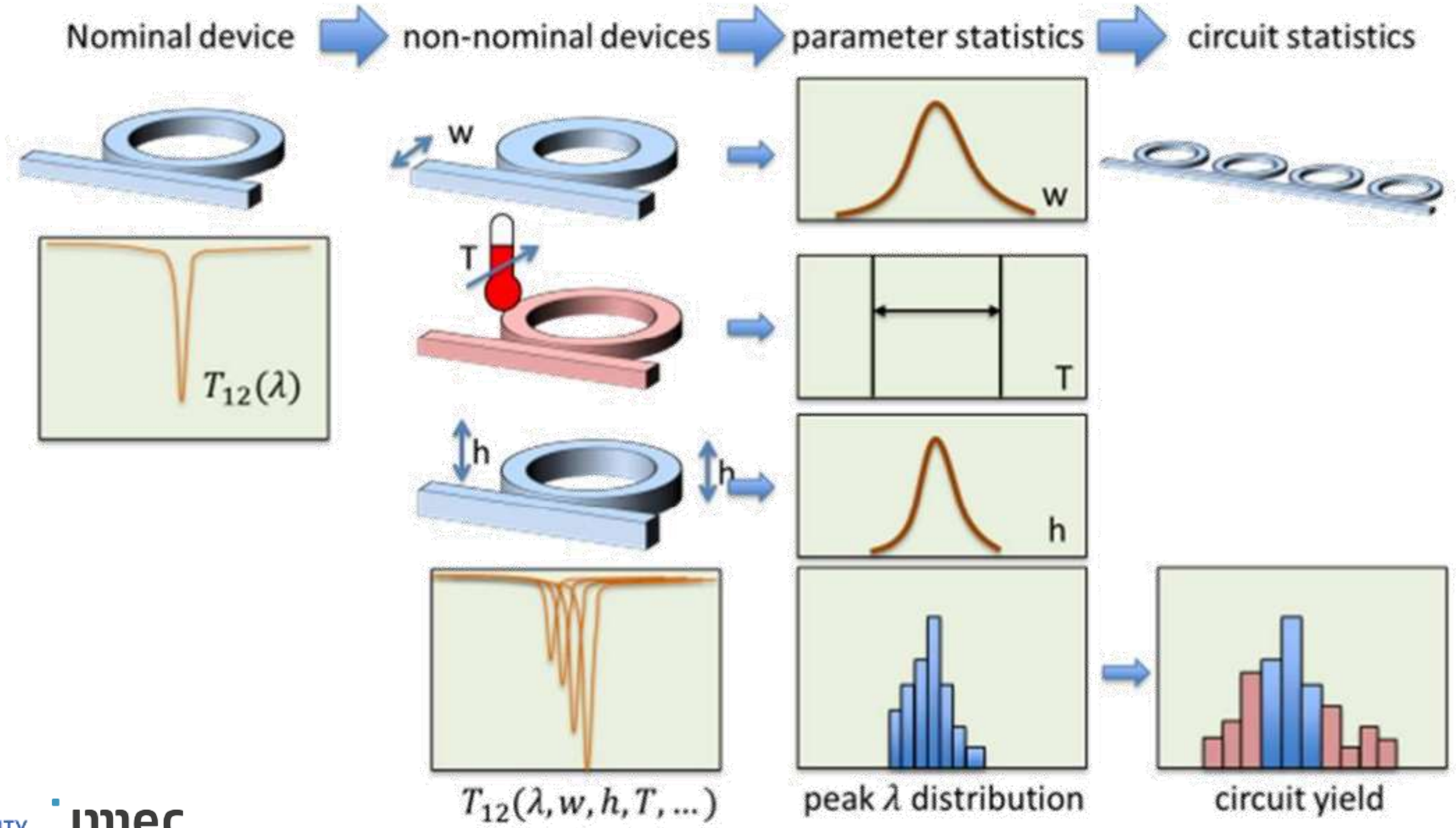
Optical and electrical co-design in Virtuoso Schematic

Photonic simulation in Lumerical Interconnect



A. Farsaei, APC 2016, JTu4A.1

Variability: Predicting circuit yield



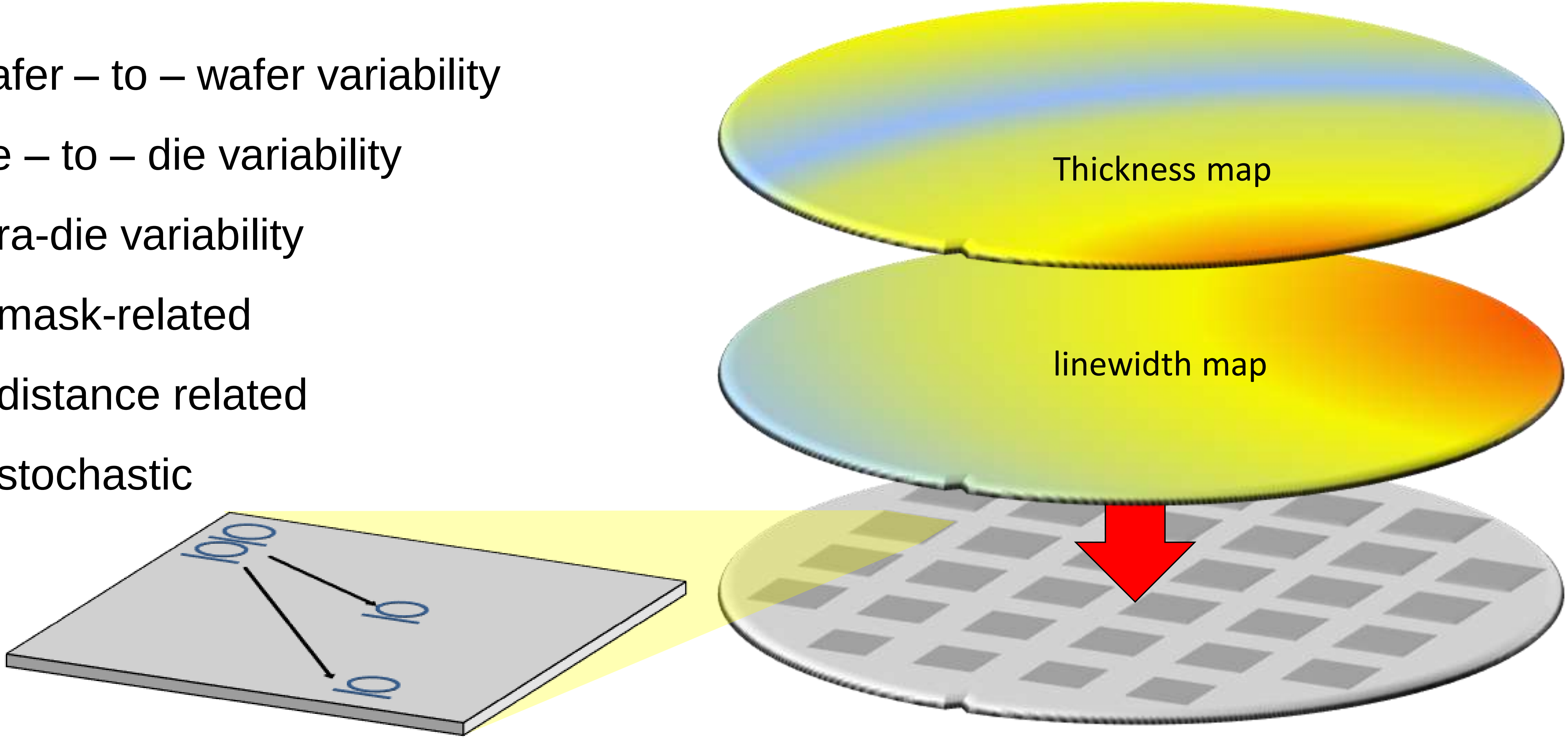
VARIABILITY ≠ VARIABILITY

Wafer – to – wafer variability

Die – to – die variability

Intra-die variability

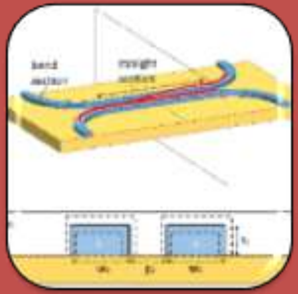
- mask-related
- distance related
- stochastic



Device variability analysis

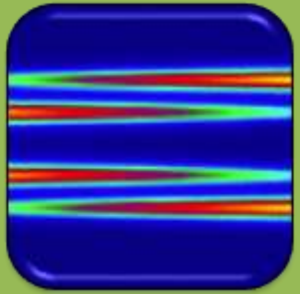
Standard technique: Monte-Carlo simulations

Requires many expensive simulations



Device error

- Fabrication
- Operation



Monte-Carlo

- Simulation
- Measurement
- Expensive

Statistics

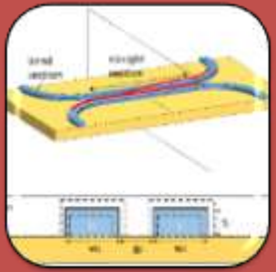
- Standard deviation
- Probability density
- Yield prediction

Y. Xing, Photon. Res. 2016

DEVICE VARIABILITY ANALYSIS

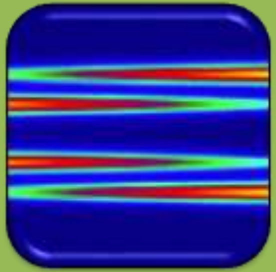
Build stochastic model from small set of simulations

Use Monte-Carlo on Stochastic model



Device error

- Fabrication
- Operation



Stochastic model

- Limited number of Simulation or Measurement

$$\langle Y(\xi)\rangle = \int_{\Omega} \sum_{i=1}^{Q} Y(\xi_i) L_i(\xi) W(\xi)\, d\xi$$

Monte-Carlo

- With stochastic model of the device (analytical functions)

Statistics

- Standard deviation
- Probability density
- Yield prediction

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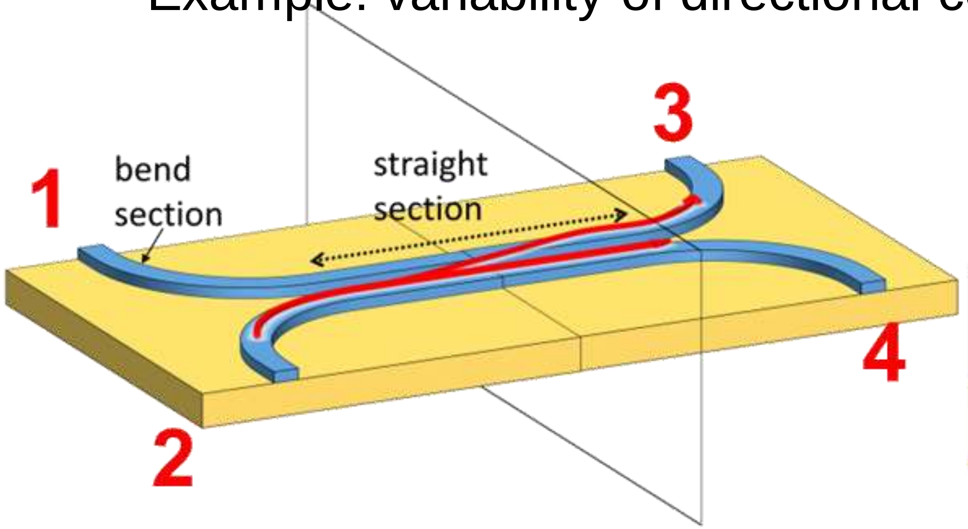
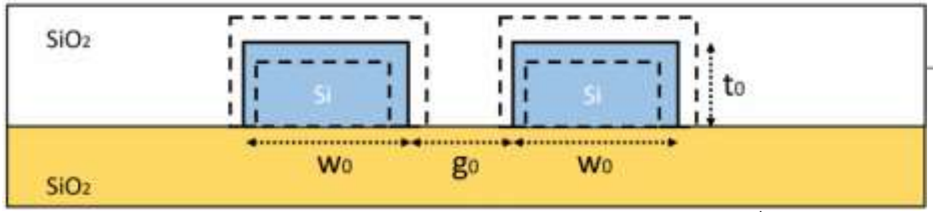
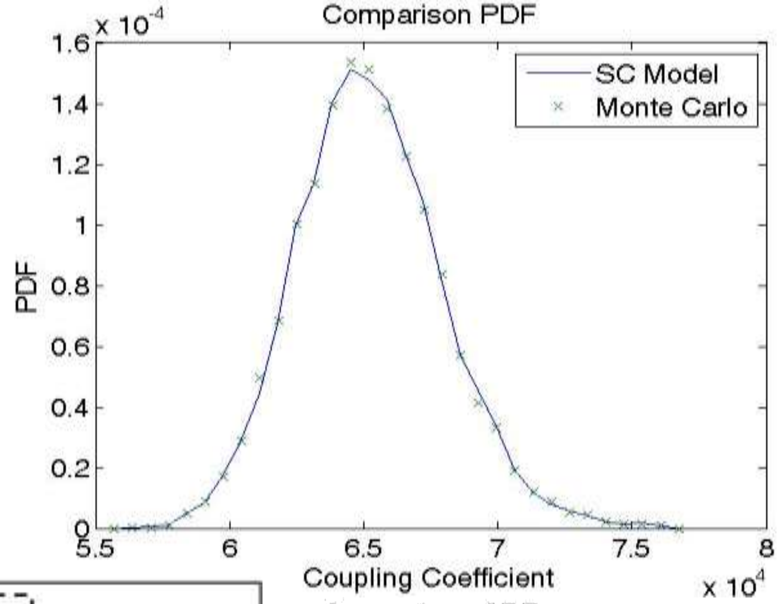
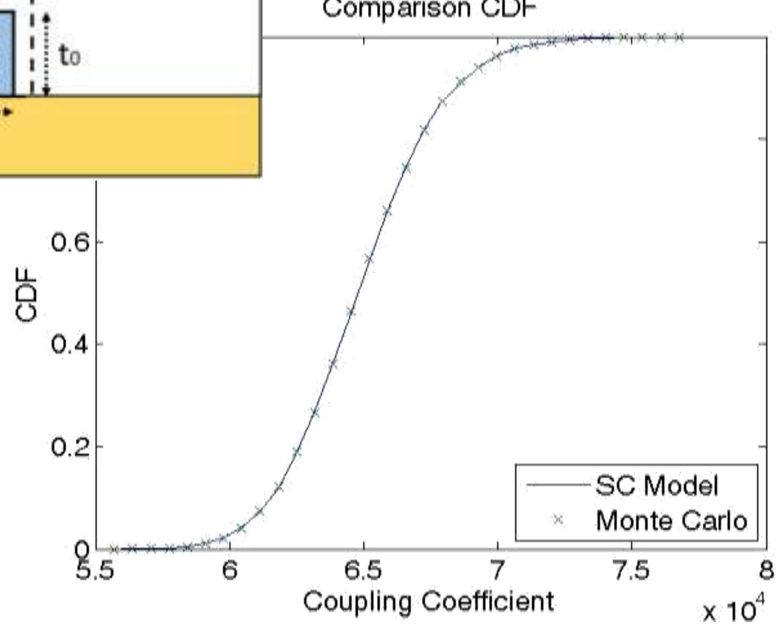
DEVICE VARIABILITY ANALYSIS WITH STOCHASTIC COLLOCATION

- Sampling-based interpolation modelling technique
- Random variables with arbitrary distribution
- Example: variability of directional coupler









Technique	Mean value of field coupling	Standard Deviation of field coupling	Computational time
MC via Fimmwave	65229.29	2716.5	22h 1min
SC modelling + MC via SC	65236.43	2720.04	9 min 50.52 s

Y. Xing, Photon. Res. 2016

Scaling complexity

Many components on a chip

Scalable building blocks

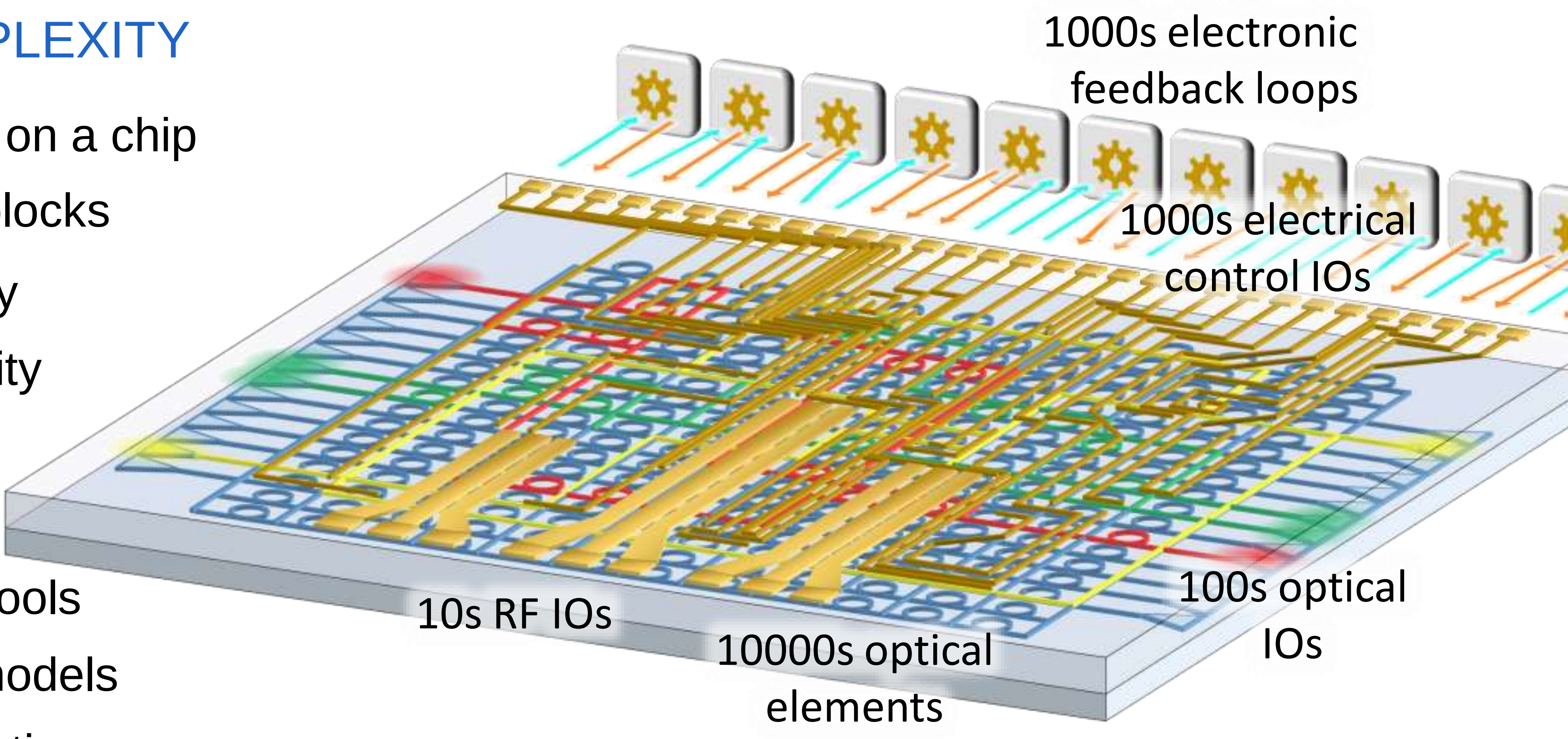
- connectivity
- cascadability
- variability

Design scaling

- synthesis tools
- accurate models
- yield prediction

Operational scaling

- control and feedback



Even with today's technology:
Perfection is achievable

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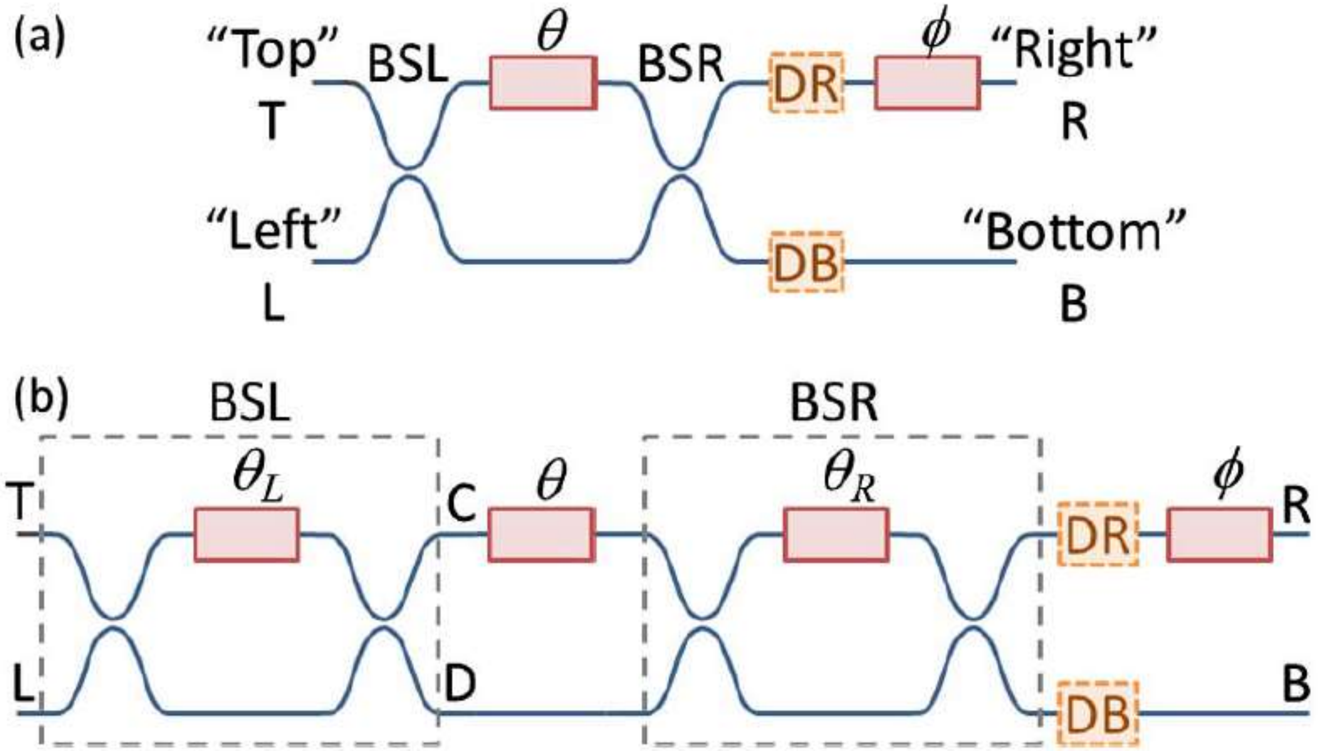
MAKING PERFECT OPTICS WITH IMPERFECT COMPONENTS

Replace specialty optical component with a more complex circuit

- Simple building blocks
- (Many) tunable elements
- Simple feedback loops



e.g. Linear N×N circuit

- tunable 2×2 couplers
- tunable delay lines
- monitor detectors

D.A.B. Miller, Optica 2, 747-750 (2015)

Photonic-Electronic Control Algorithms

Global Algorithms

All system data is available

Less monitors needed

More complex logic -> instabilities?

Less reuse

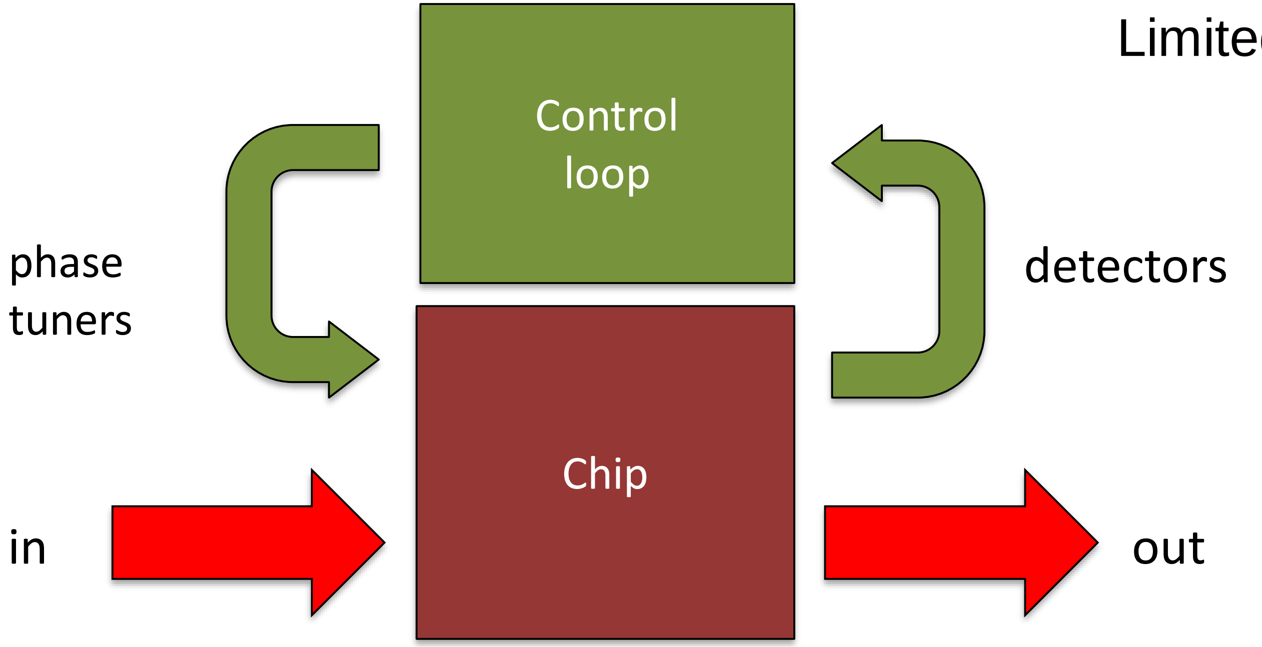
Local Algorithms

Simple logic, more stable

Reusable in larger circuits

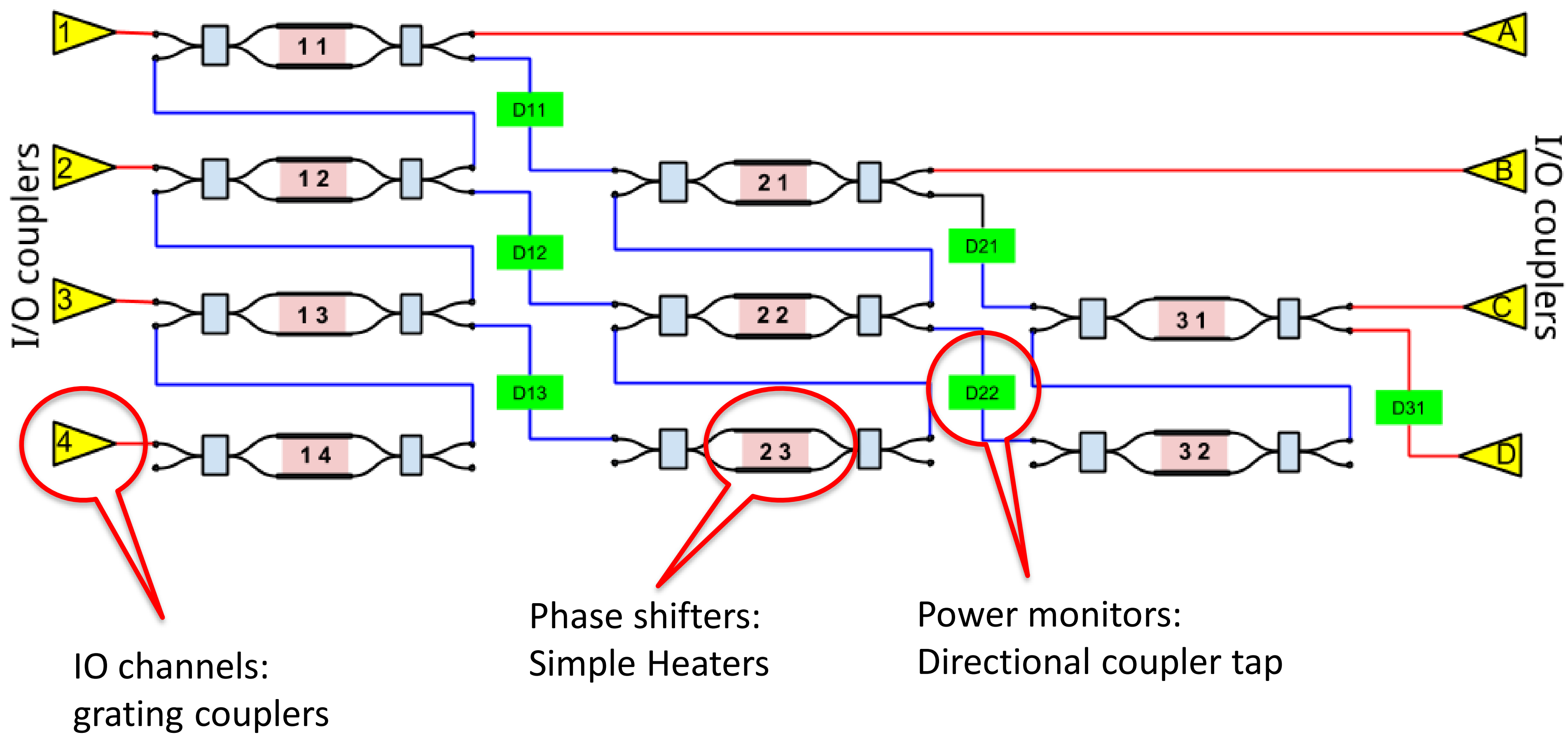
More monitors needed

Limited data available



UNIVERSAL LINEAR CIRCUIT IN SILICON

Beam splitters = MZI

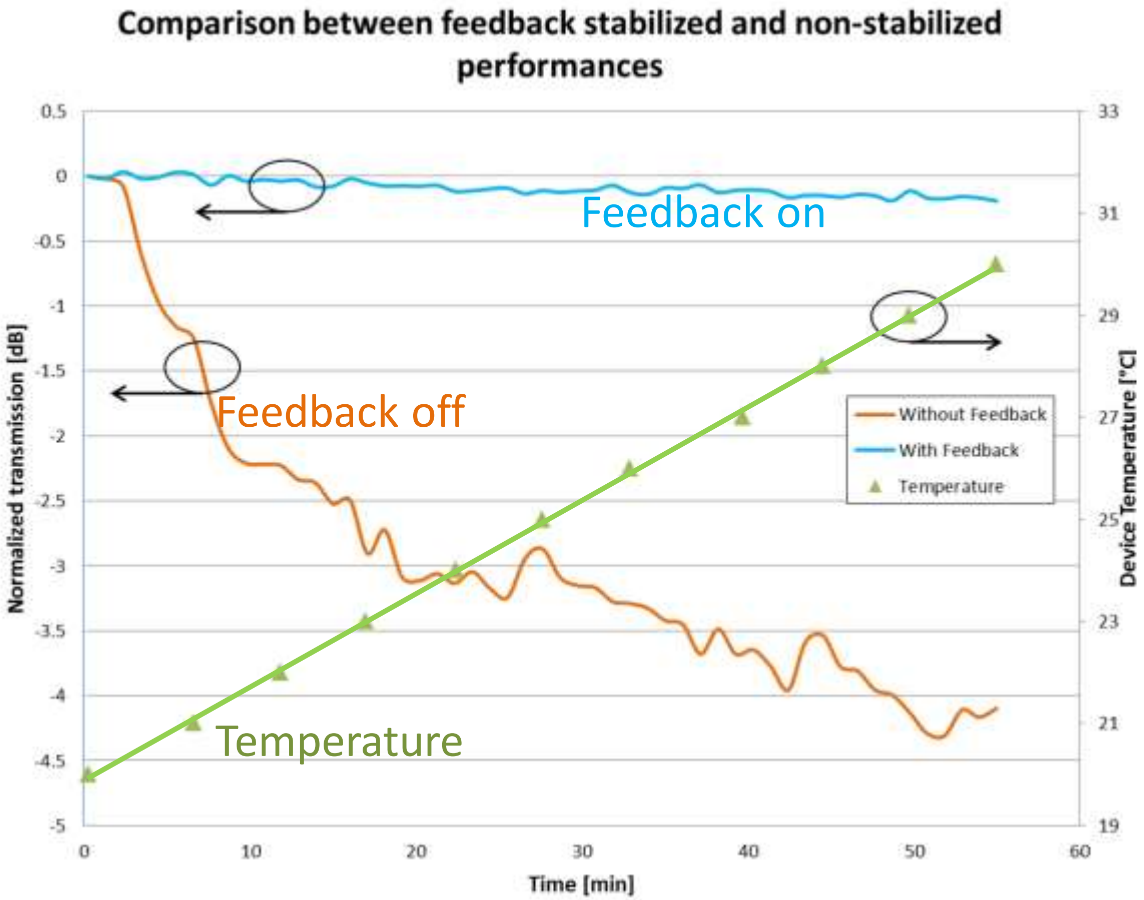


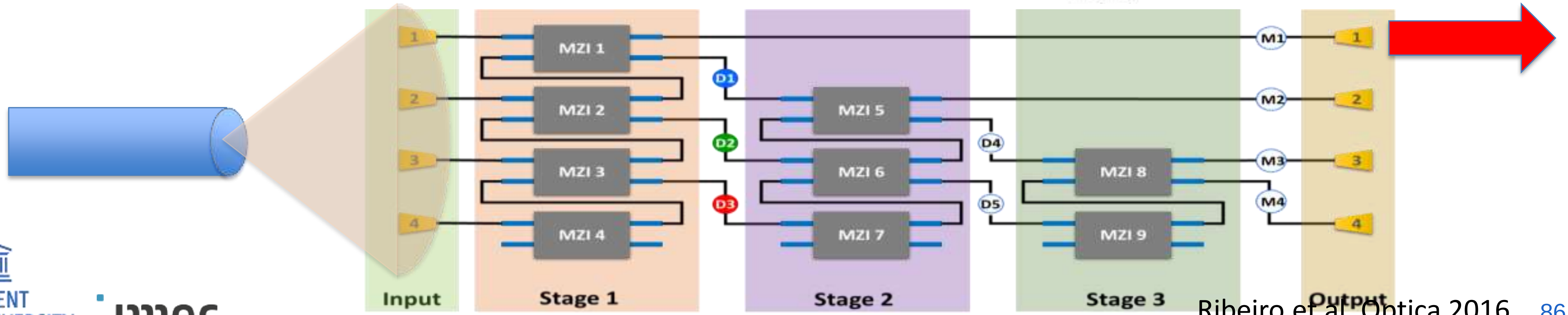
Ribeiro et al, Optica 2016

ADAPTIVE BEAM COUPLER

Circuit adapts itself to maximize output to a single mode waveguide

Local feedback loops stabilize the entire circuit.

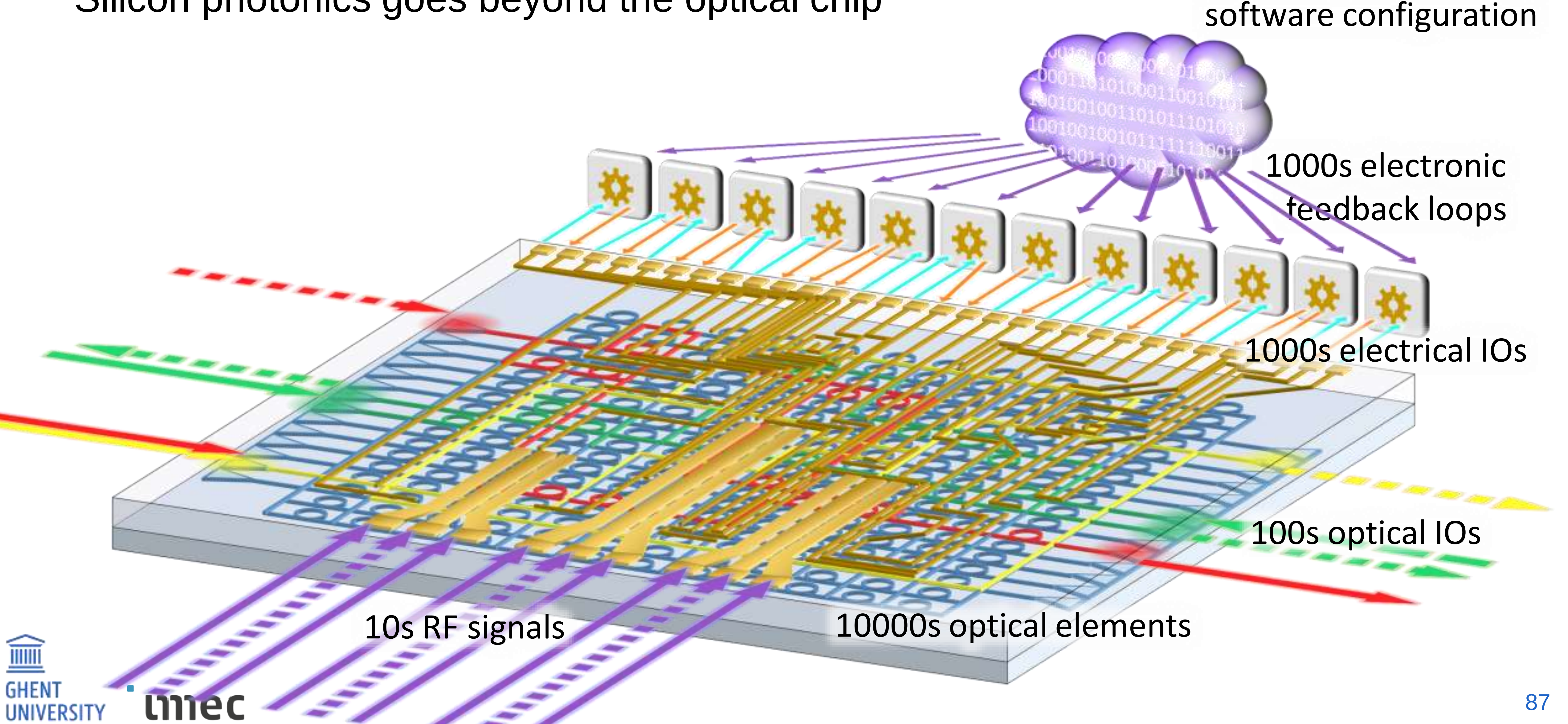




Ribeiro et al, Optica 2016

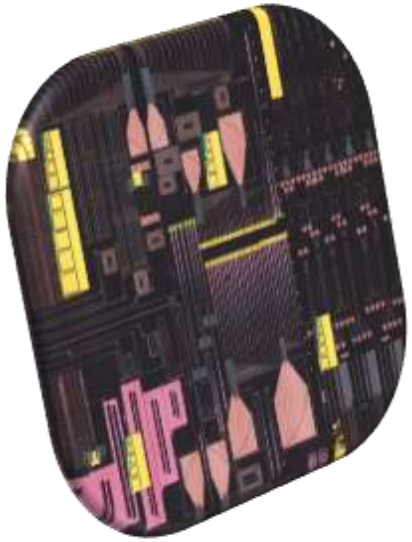
More than just photons

Silicon photonics goes beyond the optical chip

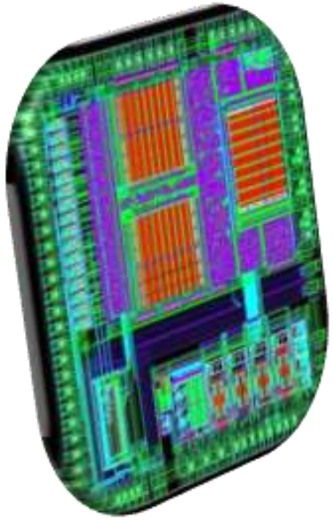


PHOTONICS IS JUST ONE PART OF THE SYSTEM

Just good enough photonics technology
Fairly simple silicon photonic circuits (e.g. simple transceiver)
Electronics and software is added to make a system
Existing electronic techniques are used to compensate for photonics



photonics



analog electronics

digital electronics

software

user

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SUMMARY

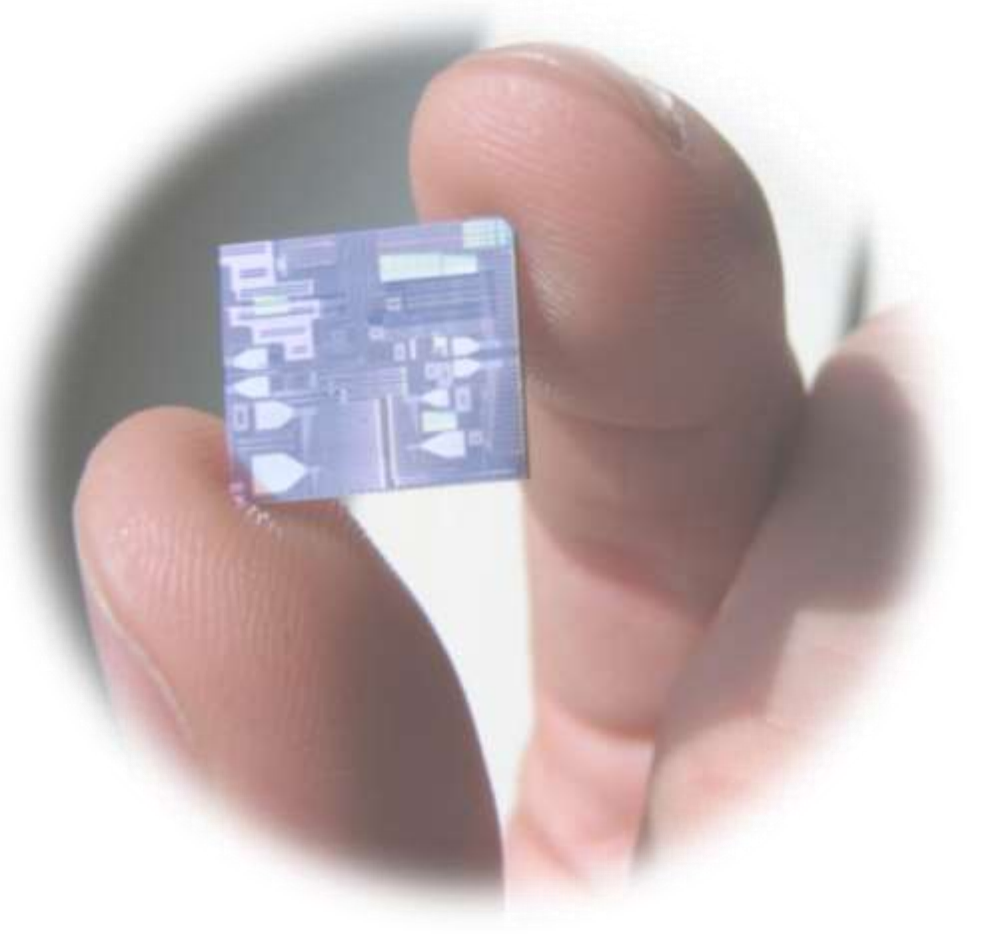
Economic Scaling in Silicon Photonics

- Based on CMOS fabrication models.
- Large volumes or uniquely large value (complexity)
- New routes emerging for R&D

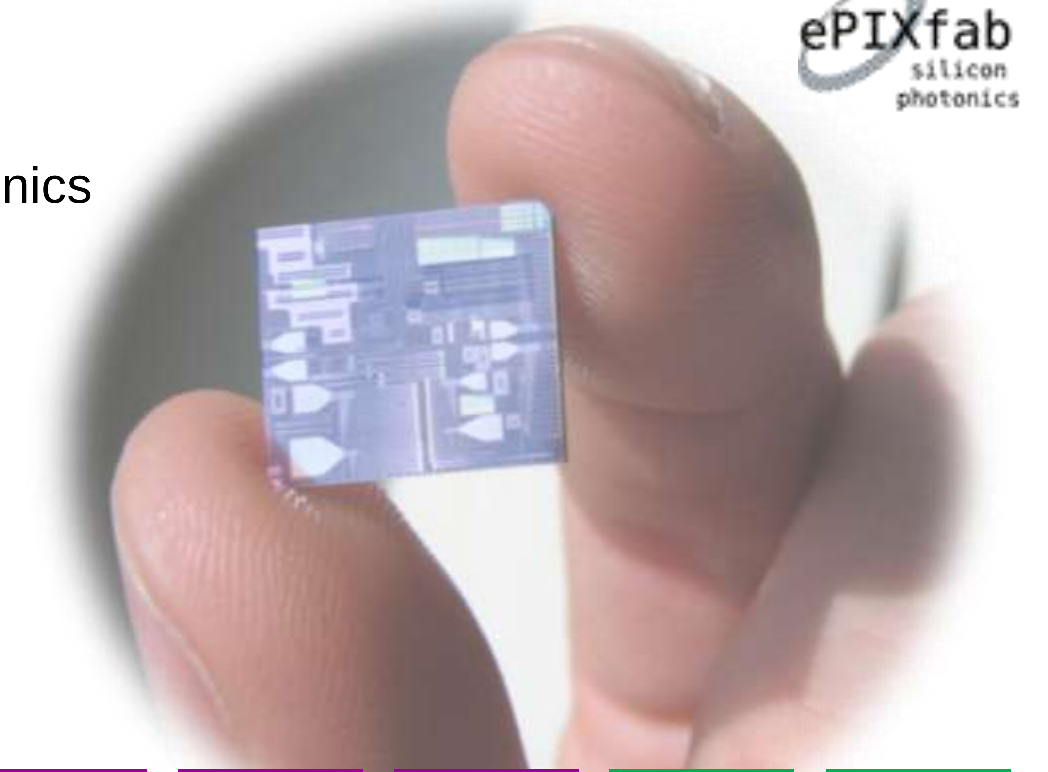
The only technology to allow complexity scaling (circuit density and connectivity)

Process technology is ‘good enough’ today, but

- Complexity scaling is limited by the design process
- Complexity scaling is limited by the control logic



SILICON PHOTONICS DESIGN COURSE



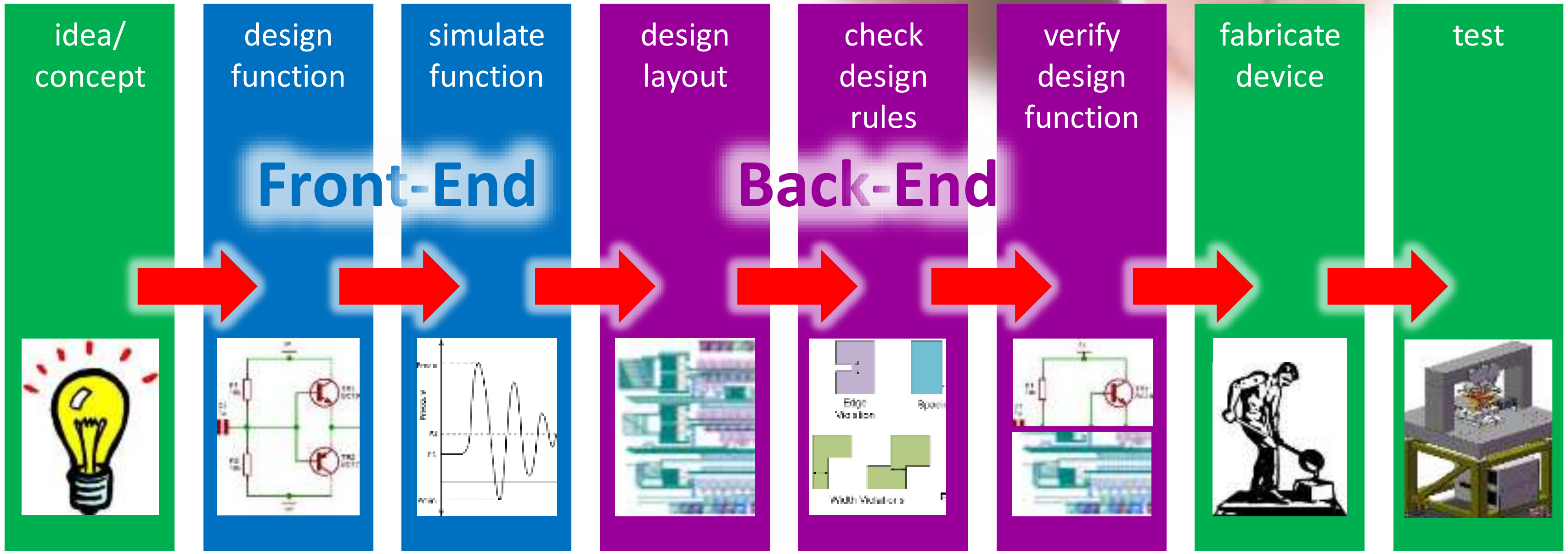
Gain a deep understanding of the design flow for silicon photonics

— circuit design and simulation
— component design and simulation
— parametric mask layout and verification

You will design a small chip that will
be actually fabricated and characterized

Ghent University

— 19-23 June
— 4-5 September



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The Ecosystem

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Volume Fabs

GLOBALFOUNDRIES
freescale semiconductor
IBM
intel
ST
TowerJazz

Design houses

ANALOG PHOTONICS
VLC PHOTONICS
BRIGHT Integrated PHOTONICS

Proto-Fabs

AUSTRALIAN SILICON PHOTONICS
IPH INTEGRATED PHOTONICS
UBC
ANT APPLIED NANOTOOLS INC.
UNIVERSITY OF Southampton

Brokers

CMC MICROSYSTEMS
ACT PHAST
EUROPRACTICE
AIM photonics
博微
The MOSIS Service
ePIXfab
The silicon photonics platform

Packaging

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PHOTONICS RESEARCH GROUP

Wim Bogaerts

Professor in Silicon Photonics

E wim.bogaerts@ugent.be

T +32 9 264 3324

@PhotonicsUGent

www.photonics.intec.ugent.be

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