

Opportunities and Obstacles of Monolithic III-V Integration on Silicon

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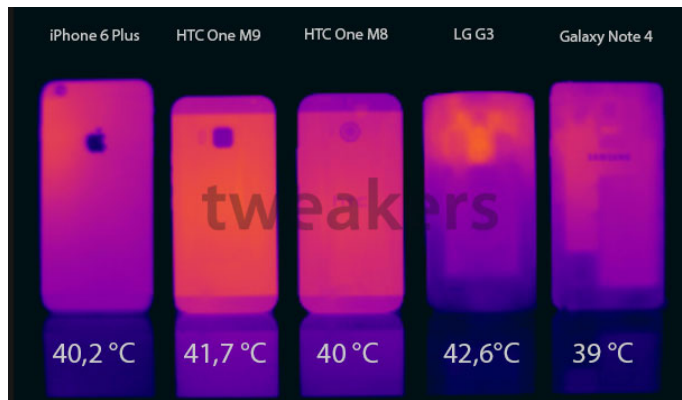


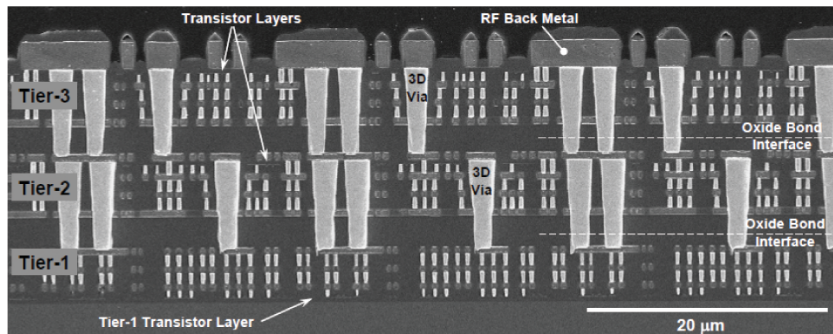
◦ Cisco Trends:

- The amount of VoD traffic in 2020 will be equivalent to 7.2 billion DVDs per month.
- Virtual reality traffic quadrupled in 2015
- The number of devices connected to IP networks will be more than three times the global population by 2020

◦ Energy sustainability

- Heat losses in datacenters
- Heat losses in smartphones and computers





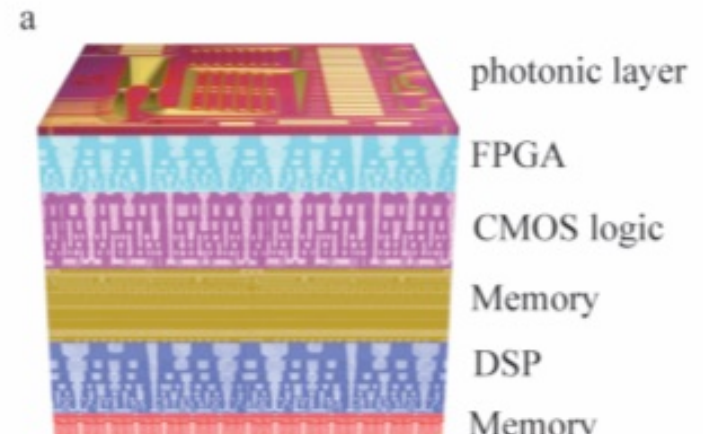
3D electronic architectures Substrate removal integration (coming from GPU)

MIT Lincoln lab (2013)

Hardware and functional hybridization

- different functionalities(memory, routing, computing)
- different technologies (photonics?)
- different computation paradigms

Integrated lasers on Silicon, Elsevier 2016



- on-chip optical waveguides for visible and IR wavelengths
- detectors
- modulators
- advanced components (filters, AWG etc...)
- on chip lasers



➡ III-V is the only mature laser platform



Xiophotonics.com

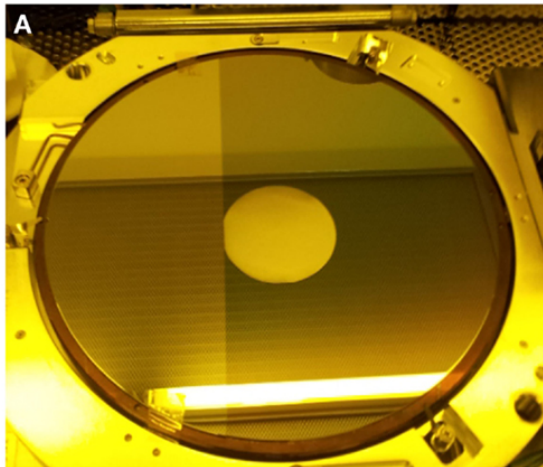
Wafer bonding

Fastest time to market?

Full wafers

Scalability issue

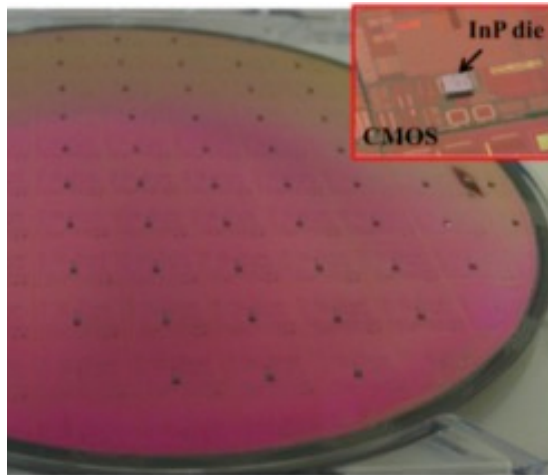
Gas by-products evacuation



Luo et al. Front. Mater. 2015

Small die bonding

Reproducibility



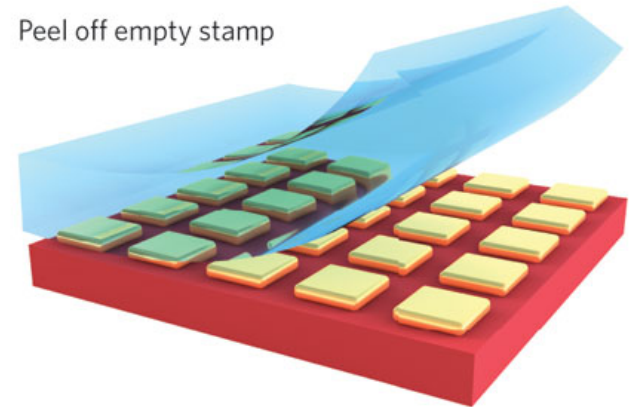
CEA-Leti

Massive transfer Printing

III-V coupons on Stamps

Scalability and accurate positioning

d Peel off empty stamp

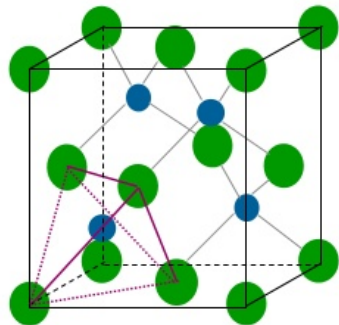


B. Corbett's group

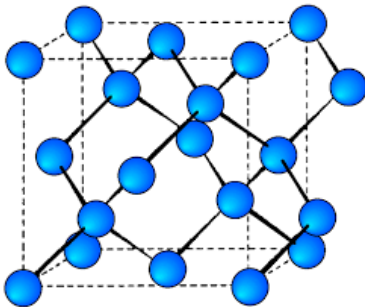
Monolithic integration: direct growth of III-V on Si

Cheaper,
Straightforward scalability
But can it be mature?

- Polar on non-polar crystals

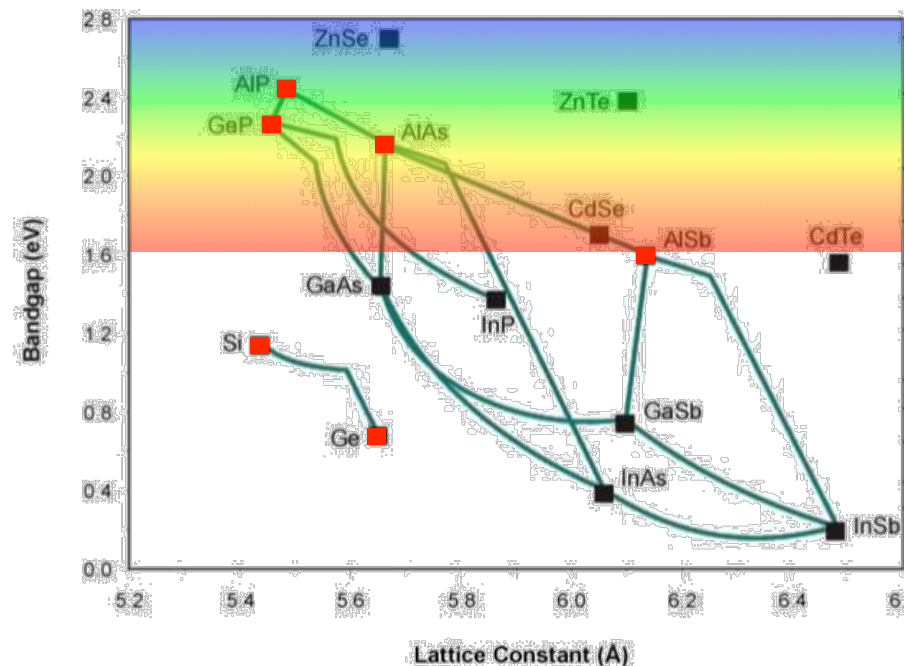


III-V
(zinc Blende)



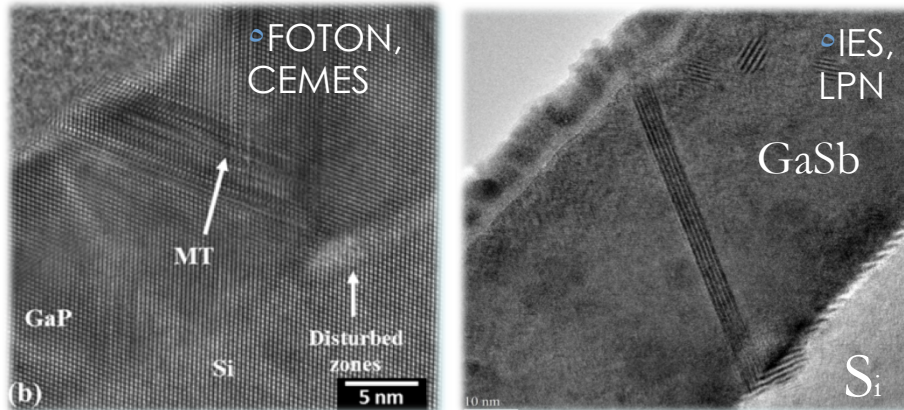
Silicon
(diamond cubic)

- Lattice mismatch



➤ Surface preparation

Cross TEM



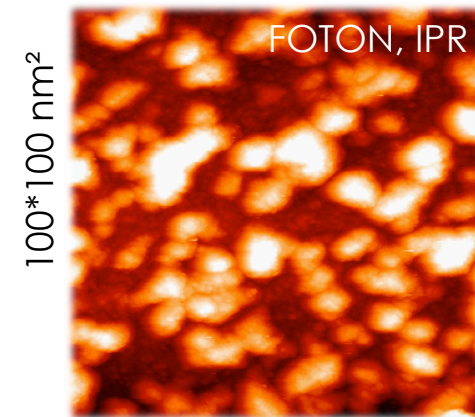
Y. Ping Wang et al., Appl. Phys. Lett. 107, 191603 (2015)

- Defects induced by pollution of the substrates
- Advanced substrate preparation
- microtwins: rotations of the III-V crystal
- no optoelectronic characterization

- Huge roughness
- not the only problem

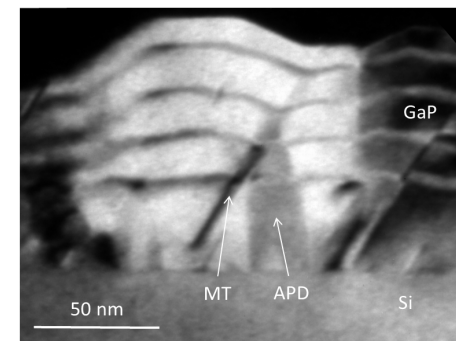
➤ 3D nucleation

STM of the nucleation layer



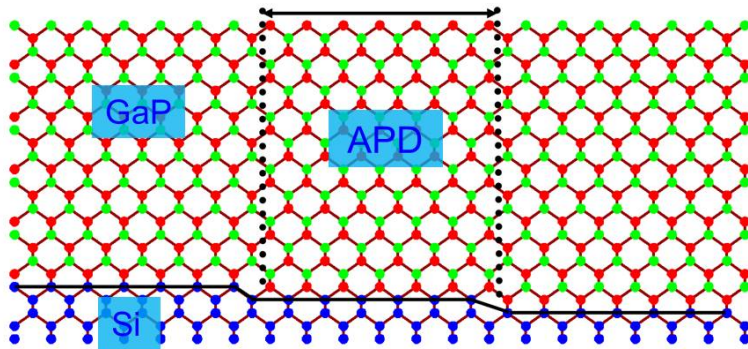
3nm GaP/Si-6°off

Cross TEM after 100nm of non-managed growth



➤ Antiphase domains

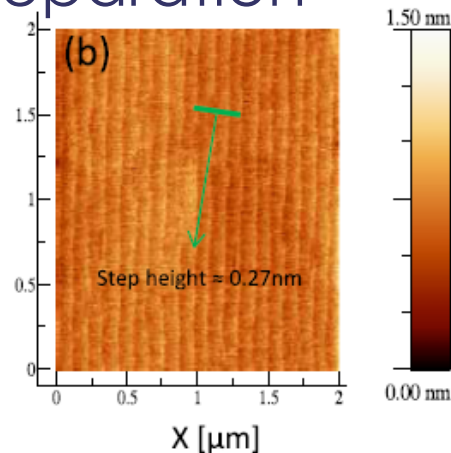
- bi-stepped surface -> vicinal substrates
- Initial Ga or P coverage



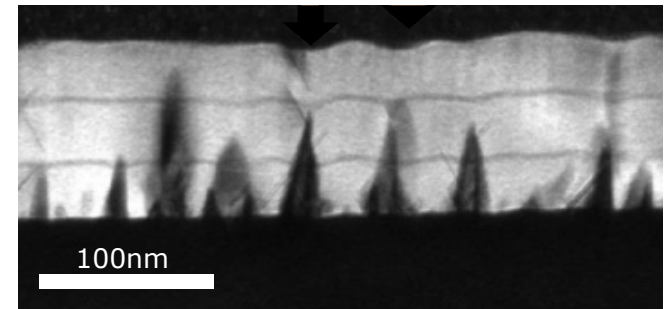
➤ Wafer preparation

- LTM
- GaAs/Si
- Vicinal to nominal

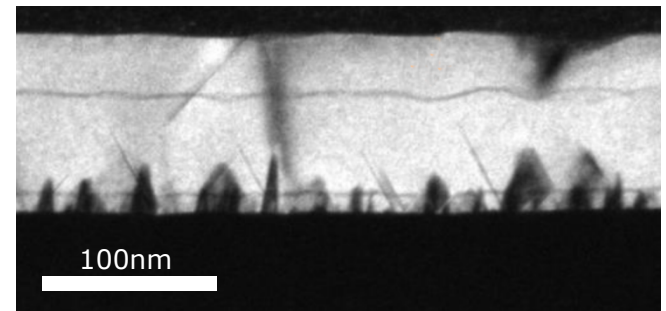
Alcotte et al. APL Mater. 2016



➤ Annihilation layers



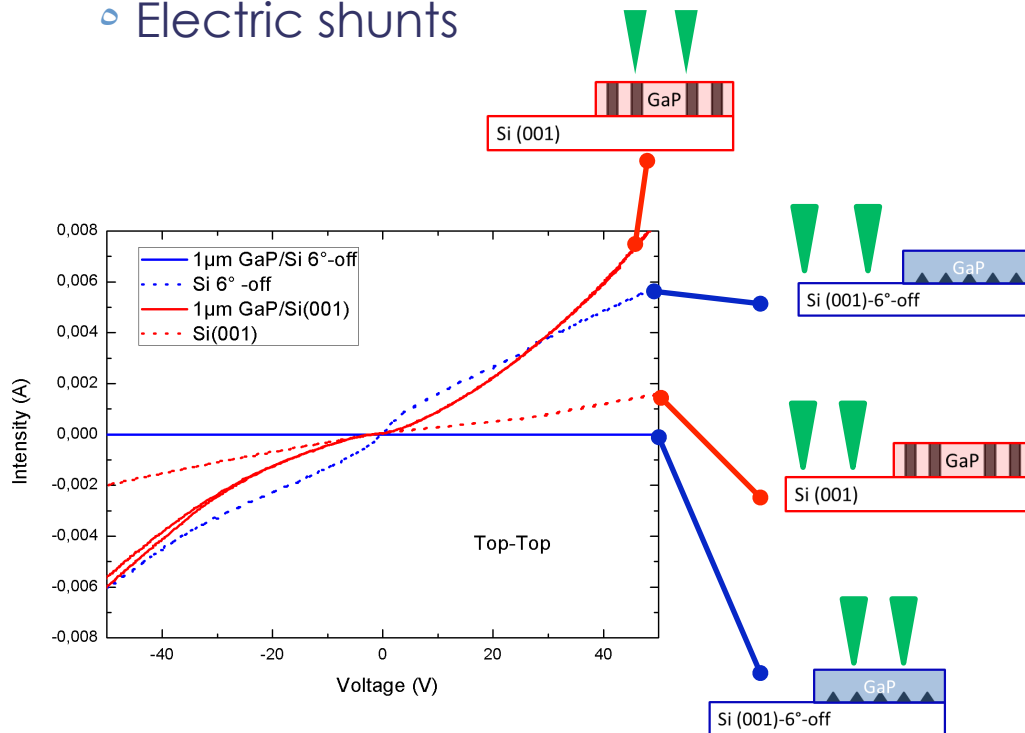
- GaP/Si
- Al-Rich layers to control the annihilation height



Antipode ANR

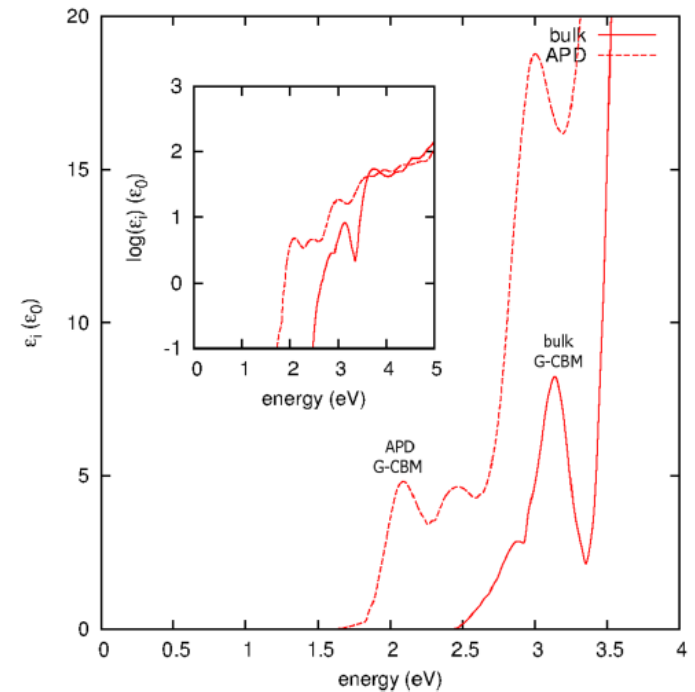
Antiphase domains opto-electronic impact

Electric shunts



Antipode ANR

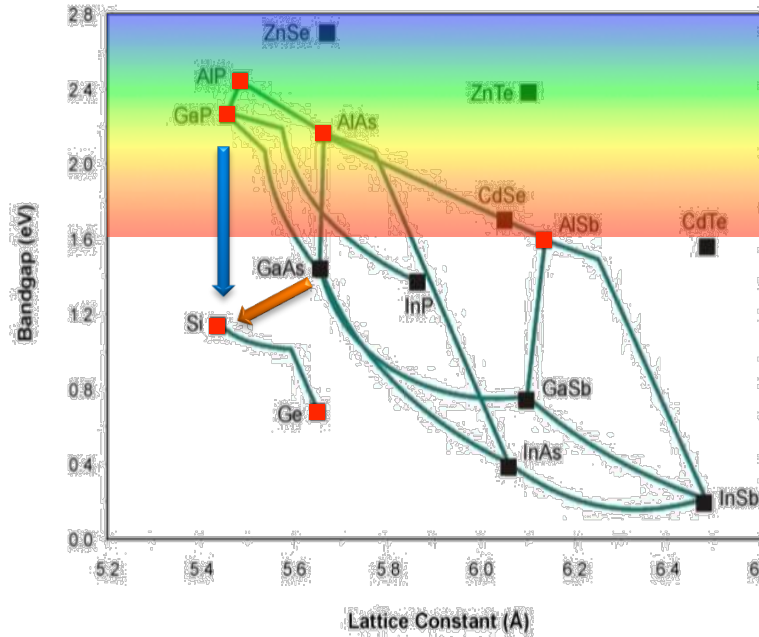
Induced absorption



Tea et al. J. Appl. Phys. 2014

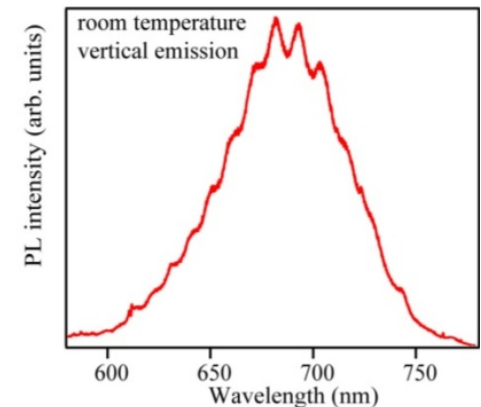
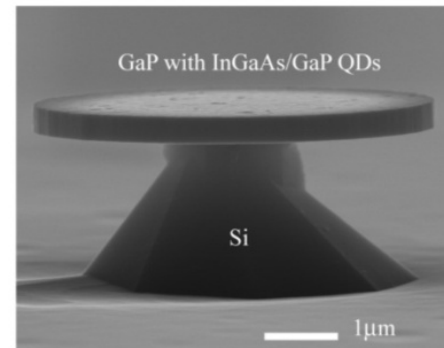
interesting for nonlinear optics

► pseudomorphic and metamorphic growth



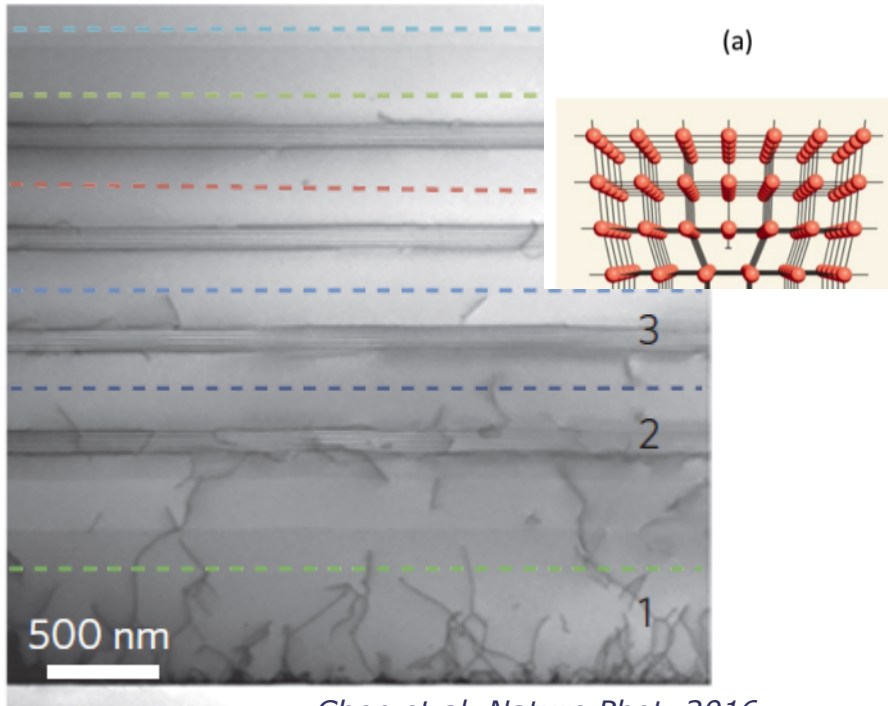
► GaP/Si emitters

- QDs 100nm above Si interface
- room temperature emission



► Huge advances on GaAs/Si devices !

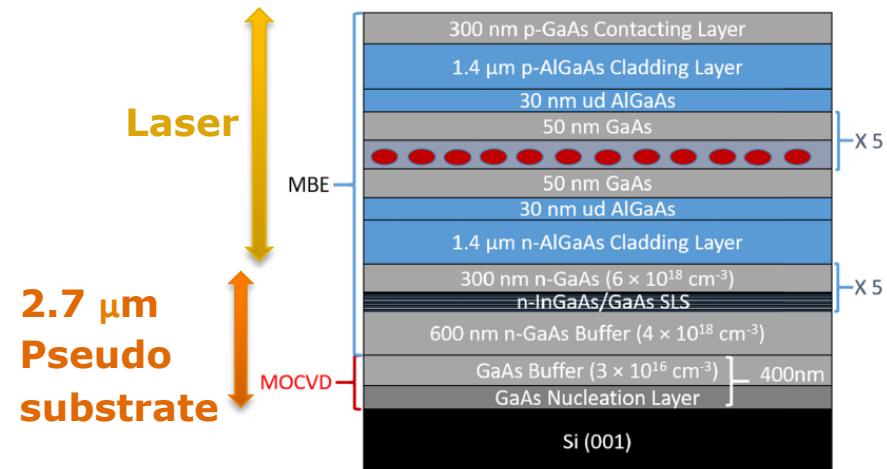
Threading dislocation management



Chen et al. Nature Phot. 2016

- Strained layer Superlattice
- Requires a thick buffer
- Lifetime issue

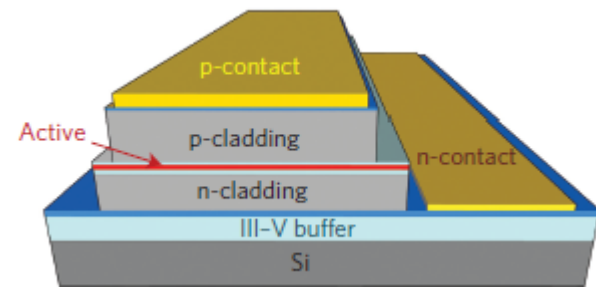
CMOS compatible design

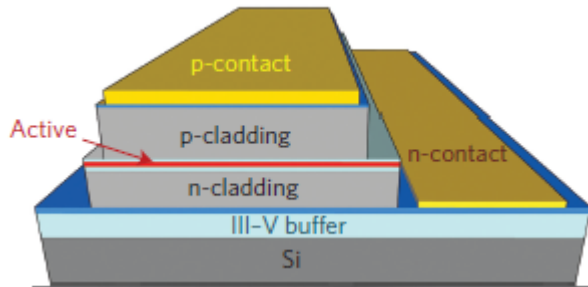


300mm Si substrate

Chen et al. Opt. Express 2017

Top-top ridge laser

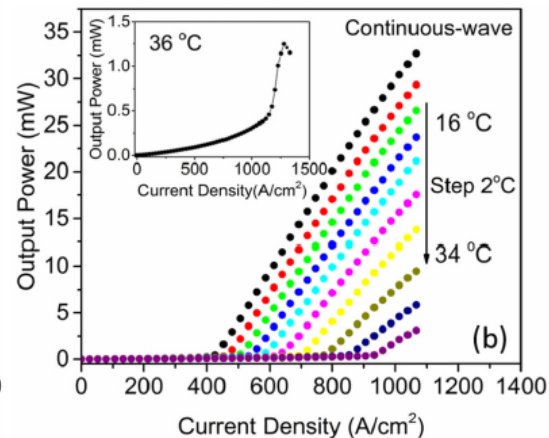
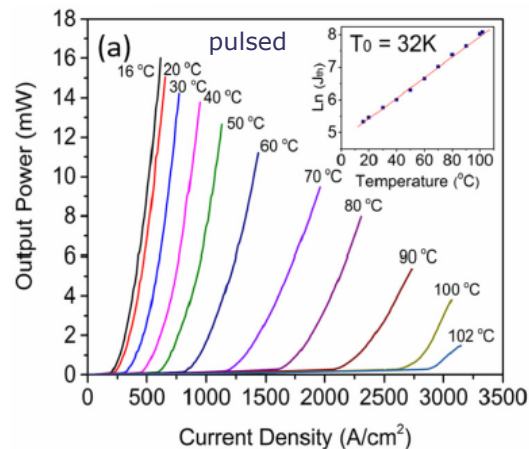




- Large temperature span
- state-of-the-art thresholds
- long lifetime

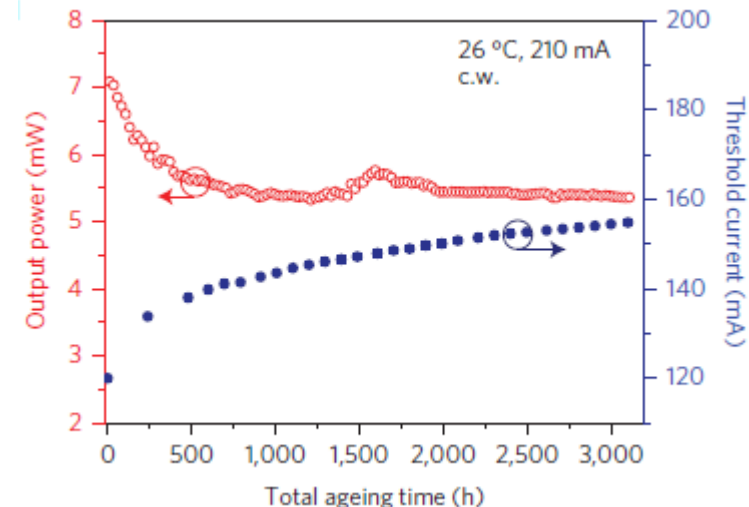
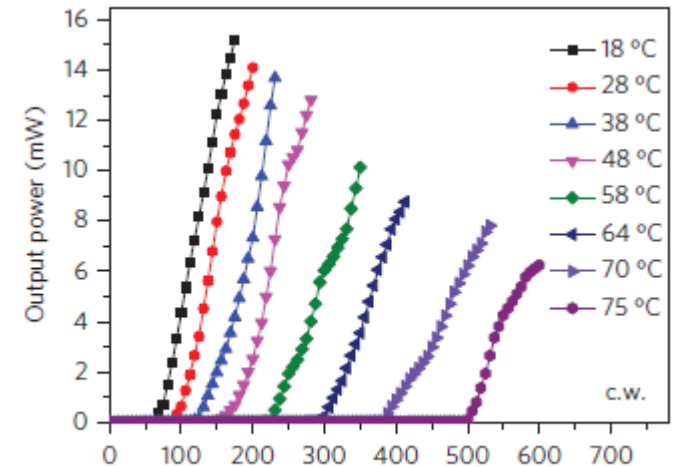
On nominal 300mm Si

Chen et al. Opt. Express 2017



On vicinal Si

Chen et al. Nature Phot. 2016



- Defect management for III-V/Si integration becomes mature
- GaAs/Si lasers reach state-of-the-art performances
 - smaller consumption than InP-based lasers
 - Si transparency emission
 - promising lifetimes
- Remaining issue of the pseudo-substrate
 - Interest of SOI integration?
 - 3D integration (substrate removal)

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◦ Colleagues from 3D core:

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