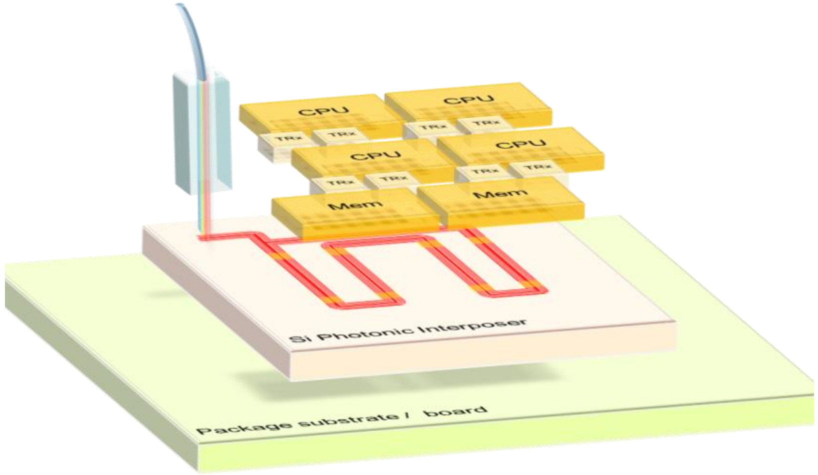


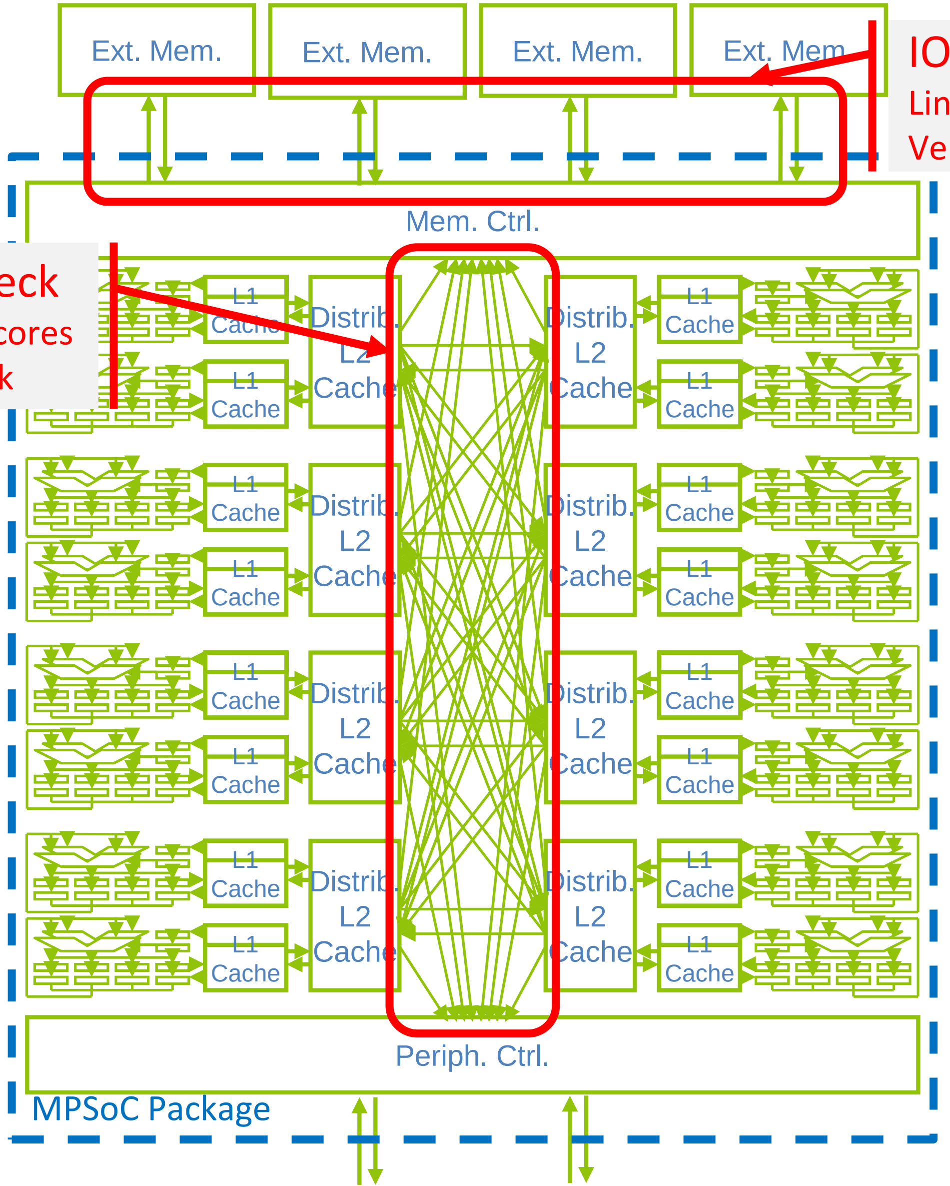
ON THE WAY TO PHOTONIC INTERPOSERS, BUILDING BLOCKS FOR USR-OPTICAL COMMUNICATION

OPTICS Workshop – DATE 2017 | Yvain THONNART | Mar. 31st 2017

OUTLINE

1. Motivations – Interposer technologies for manycores
2. Our goal – An optically interconnected manycore on interposer
3. Silicon photonic links – Optical and electrical elements
4. Optical routing – SWMR link and protocol, ONoC topology
5. Electrical drivers – Transmission & tuning
6. ONoC Architecture – Performance metrics

COMMUNICATION BOTTLENECKS IN MANYCORES



IO Bottleneck

Linear BW increase w. #cores

Very high throughput muxed links

Internal Com. Bottleneck

Quadratic BW increase w. #cores

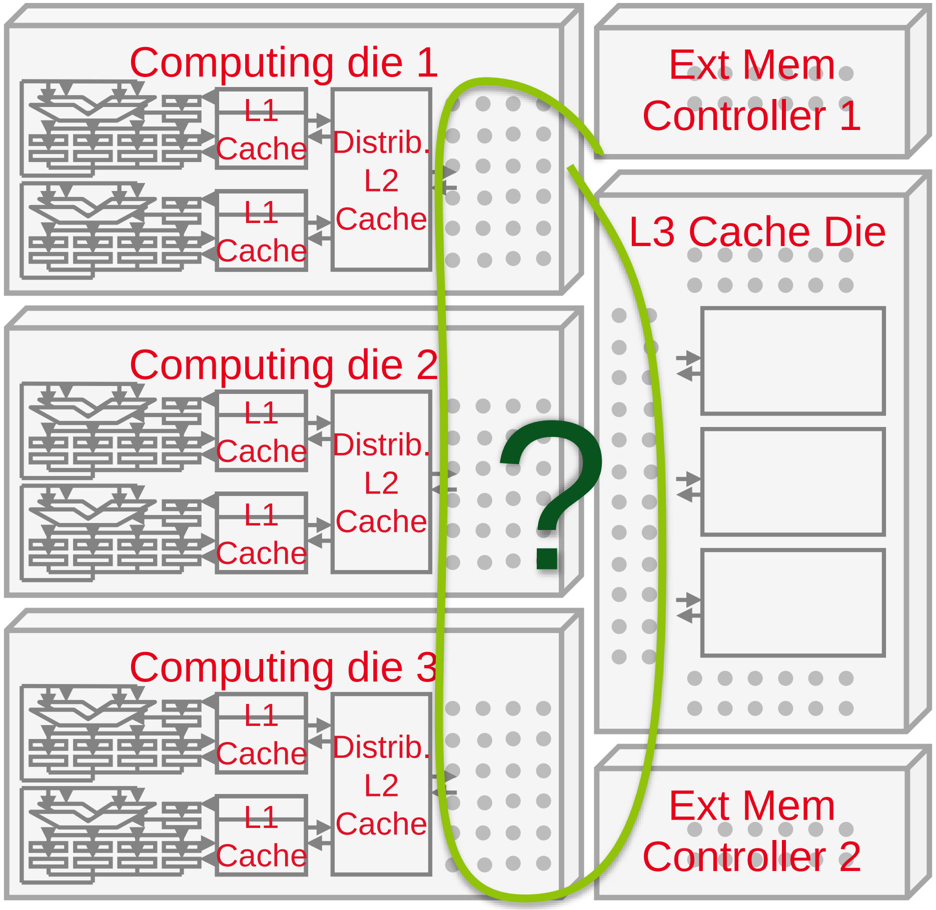
Constant throughput per link

(2015)[NOCS] Thonnart, Y.

CHIPLET PARTITIONING ON INTERPOSERS TO INCREASE YIELD

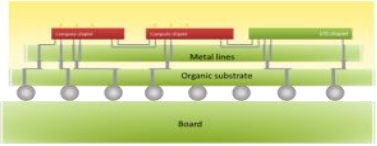
- **Higher manufacturing defects per cm² in advanced CMOS nodes**
  - Very-low yield on large monolithic dies
- **Options:**
  - Design 4–6 cm² dies, deactivate processors, sell as lower grade
  - Design ≤**1 cm²**, and stack on variability tolerant interposer

➔ **Need an efficient and scalable interconnect solution**



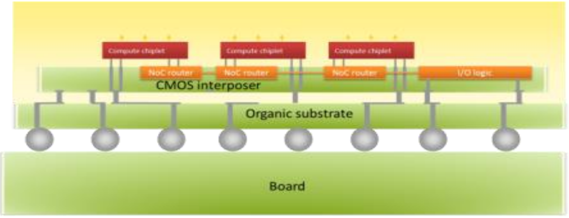
(2015)[NOCS] Thonnart, Y.

PHOTONIC INTERPOSER:
THE SCALE-UP/SCALE-OUT TECHNOLOGY…



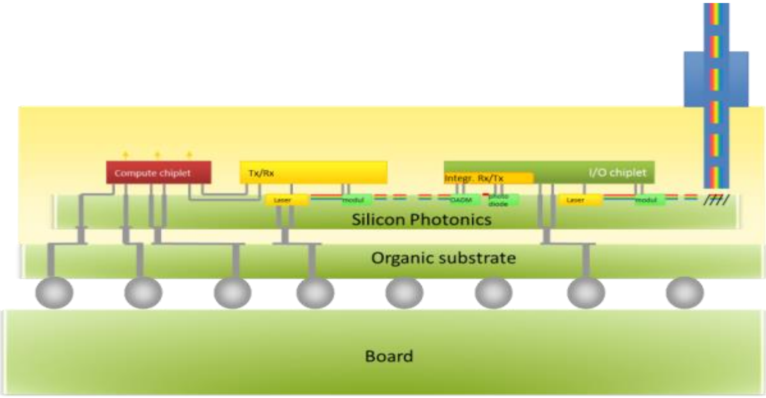
Metallic interposer

1-4 chiplets



Active interposer

6 chiplets



Photonic interposer

6-10 chiplets

2015 → **2017** → **2020**

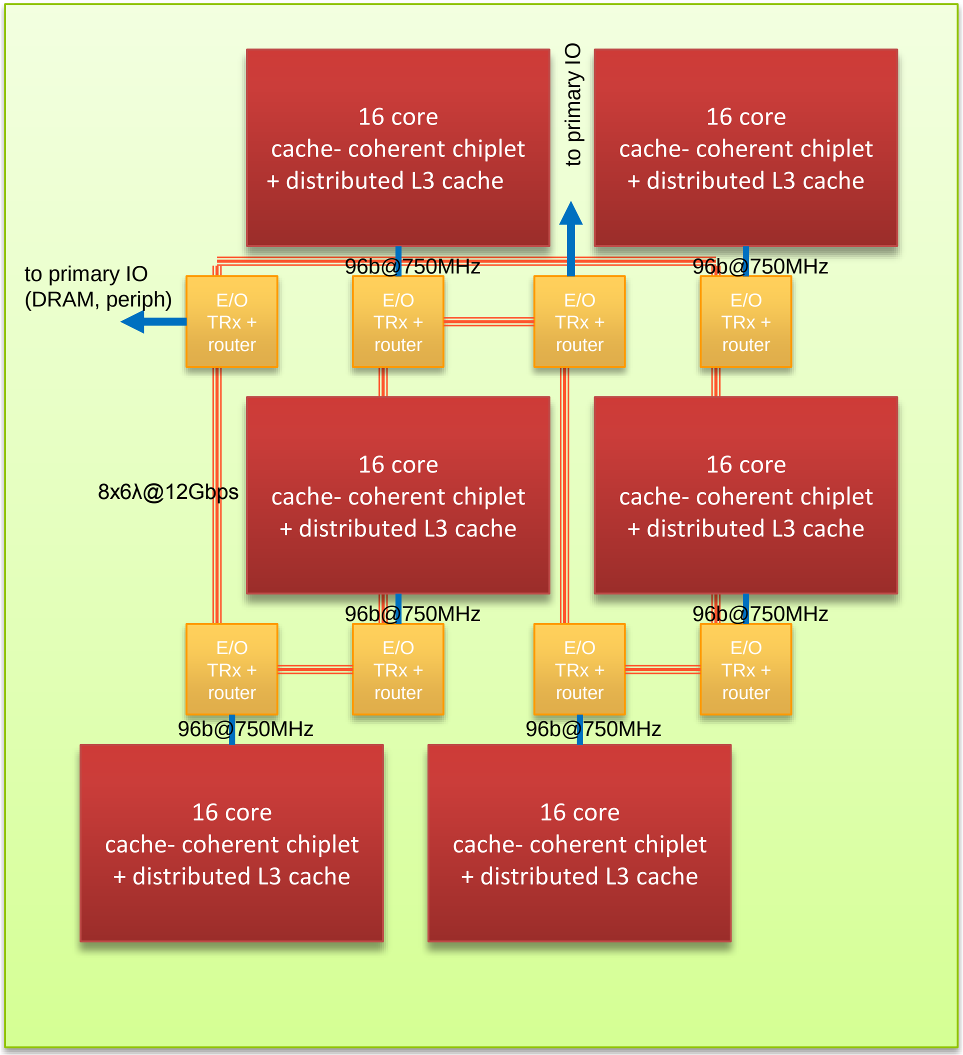
Technology	Metallic	Active	Photonic
On-chip bandwidth	≤ 250 Gb/s	≤2 Tb/s	>4Tb/s (>2x)
Number of cores	≤ 16	≤ 36	> 72 (>2x)
Power for on-chip com	~ 1 W	~ 20 W	~ 20 W (~1x)

(2015)[NOCS] Thonnart, Y.

TARGET MANYCORE ARCHITECTURE

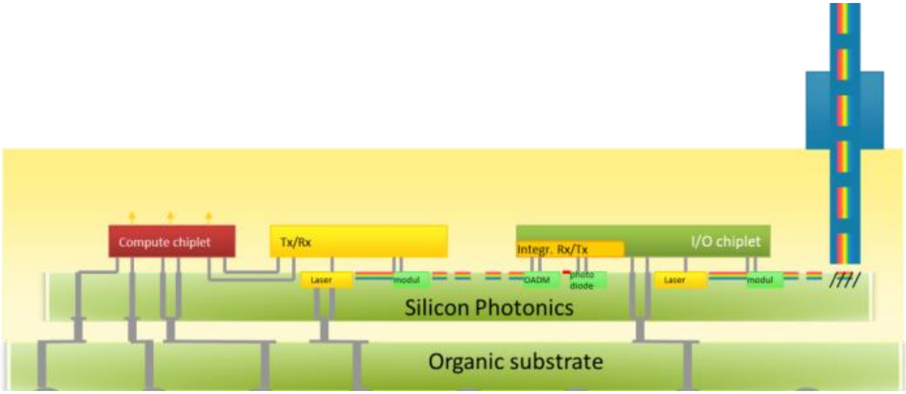
- **96 cores in 6 chiplets on the interposer**
  - Coherent shared-memory
  - Boots a single Linux OS
- **ONoC to convey cache coherence protocol**
  - Fan-in from the 16 cores to a 96b interface at 750MHz to the E/O transceiver/router
  - Transduction to 6 wavelengths used in parallel at 12 Gbps
  - Complete connection between 8 transceivers/routers
  - Fan-out to the distributed L3 caches, main memory and peripherals.

➔ Peak aggregate bandwidth on the interposer is 576 Gbit/s

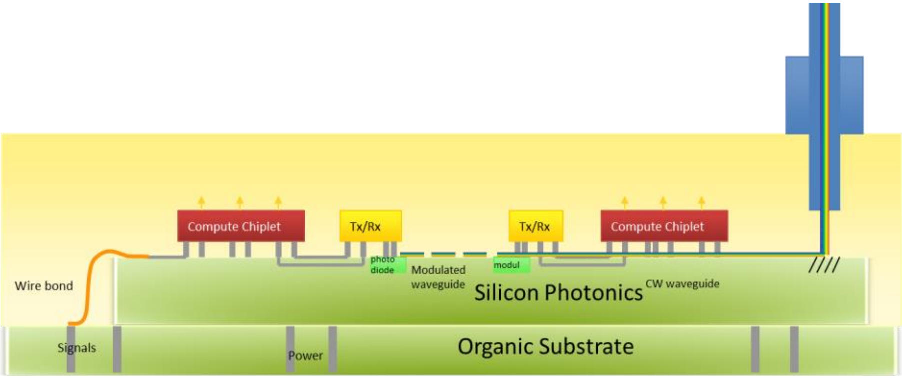


3D CROSS-SECTION & TECHNOLOGY OPTIONS

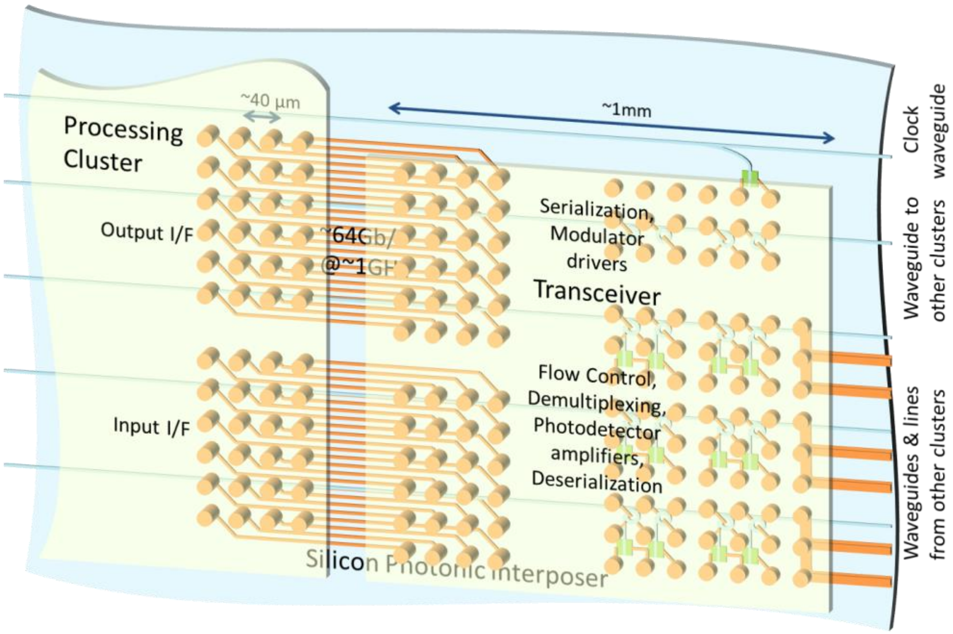
- **Long-term perspective**
  - Optical Primary IO
    - Would require to add a concentrator E/O chip with aggressive standards (400Gb Ethernet…)
  - Integrated E/O transceivers
    - With the compute chip
    - Or on the interposer with monolithic CMOS/SiPho process
  - Integrated lasers ?
    - Not necessarily because of WPE collapsing at high temperatures



- **Short-term option**
  - Off-chip lasers
  - No TSV (neither power nor signal)
  - Separated E/O transceivers



DESIGN TARGETS

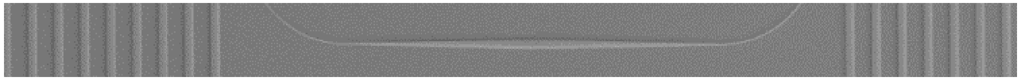


- **Ultra-dense integration**
  - ONoC Implements a complete graph interconnection between all transceivers/routers
  - ➔ Drivers should not take more space than the 3D connection interface pitch to the photonic interposer (~0.01mm² per channel)
- **Improved power-efficiency wrt. CMOS solutions**
  - Point-to-point high-speed electrical links do not scale
  - A similar synchronous NoC of the same size with the same performance including virtual channels would use > 20pJ/bit
- **Wide temperature range**
  - Dissipated power in manycores can create temperature rises up to the TDP of the package, but the system should also be operational at ambient
  - ➔ 0°C to 90°C operating range

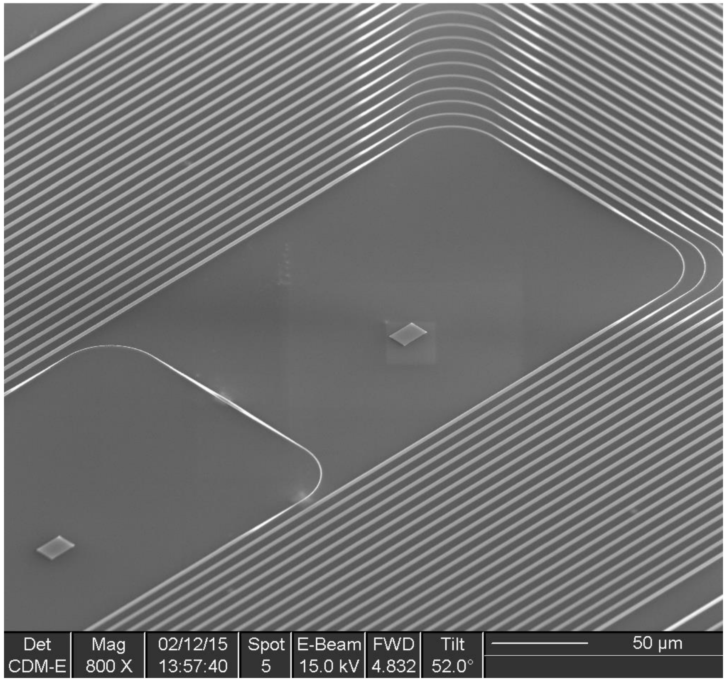
(2014)[FETCH] Y. Thonnart (invited)

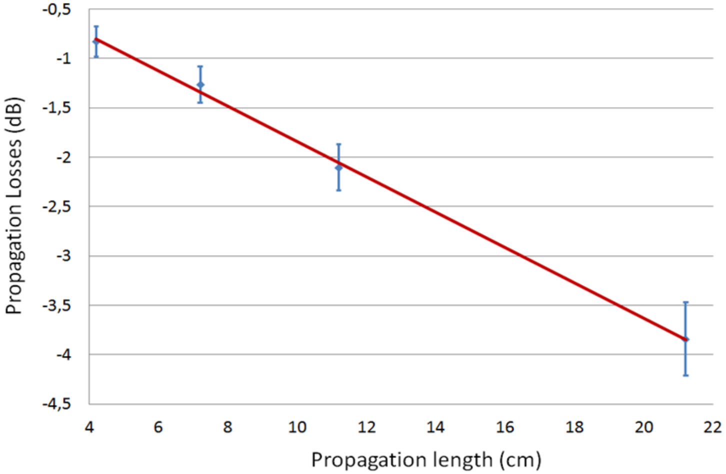
COPPER REPLACEMENT ON THE INTERPOSER: LOW-LOSS MULTIMODE WAVEGUIDES

- Tapered transitions from 400nm to 2.5 µm width
  - Preservation of a single mode in a multimode waveguide



- 12x Reduction of optical losses
  - from 2.2 dB/cm for a 400 nm width monomode waveguide
  - to 0.18 dB/cm with a variance of 0.02 dB/cm for the 2.5 µm width waveguide
- For a typical optical link length of 10 centimeters, the net gain in transmission expected to be 20 dB (relaxes the design constraints and the energy consumption for a 6 dies multiprocessor system).





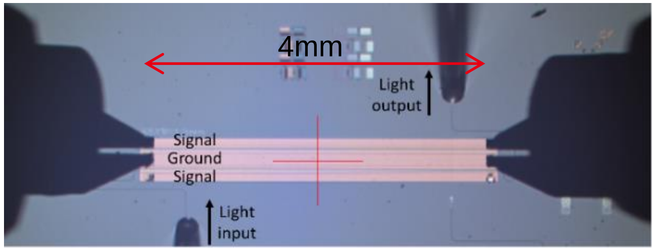
(2016)[SPIEOI] Reboud et al.

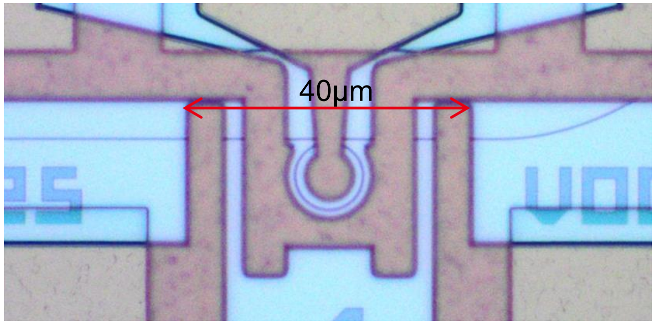
SWITCHES REPLACEMENT ON THE INTERPOSER: MICRORING RESONATORS

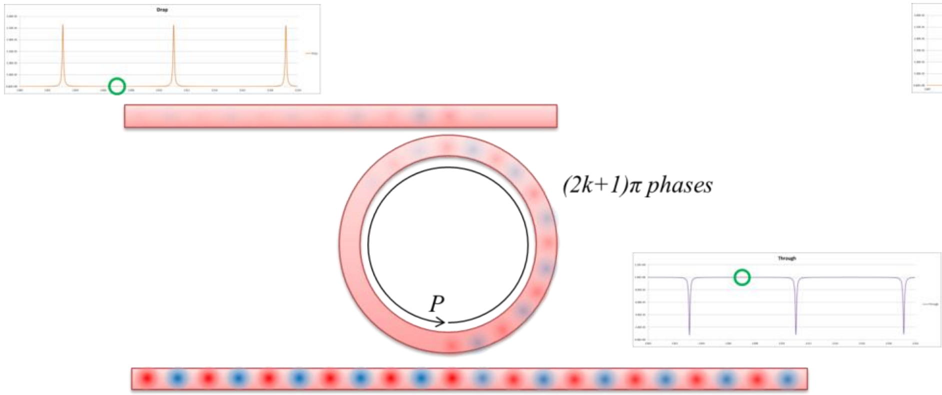
- **Dense integration requirement:**
  - Mach-Zehnder modulators are too long to be matriced locally (>1mm)

➔ Microring resonators are compact
  - ➔ have sharp resonances allowing WDM
  - ➔ PN or PIN diode junction for electrical control

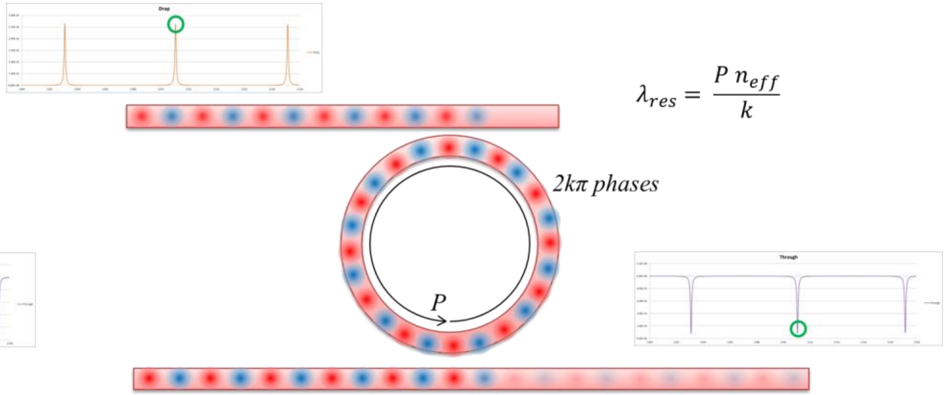
  - ➔ PN rings can be used as modulators (> 10 Gbps)
  - ➔ PIN rings can be used as filters (<500 MHz) for routing and wavelength demultiplexing







Out of resonance



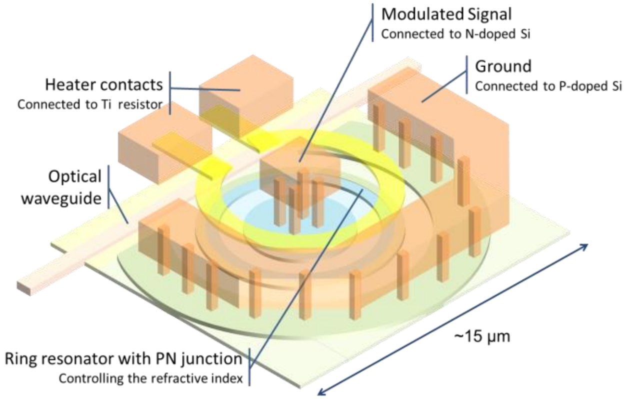
$$\lambda_{res} = \frac{P\, n_{eff}}{k}$$

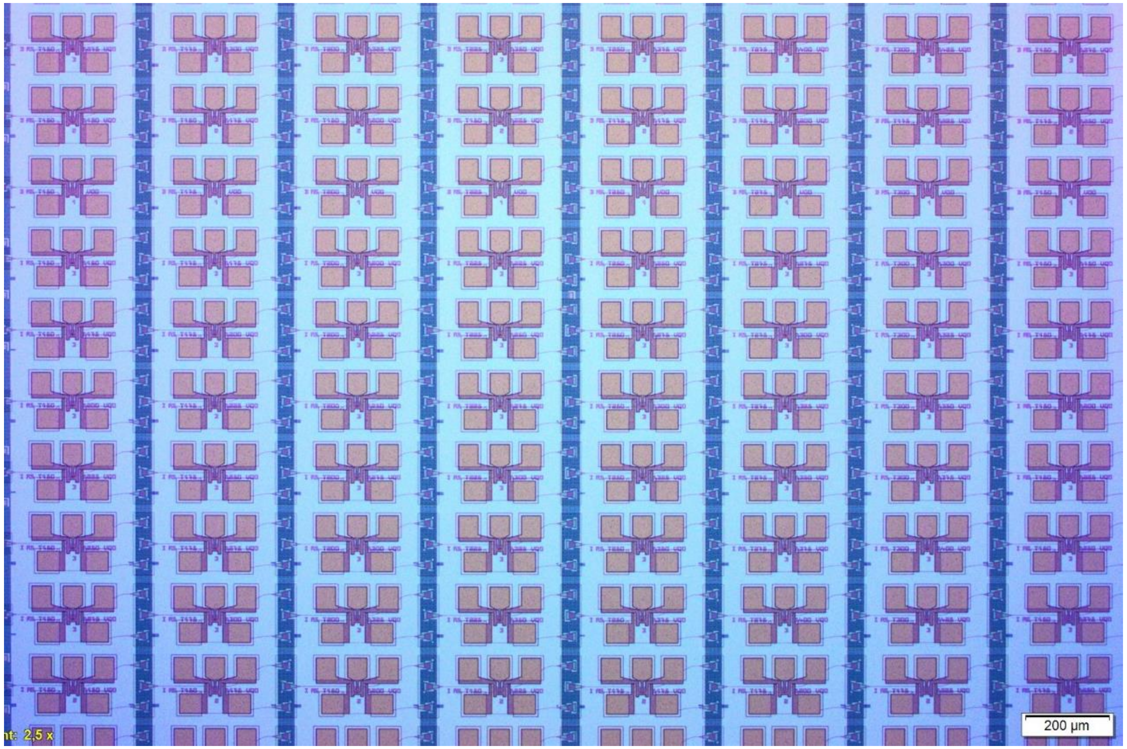
At resonance

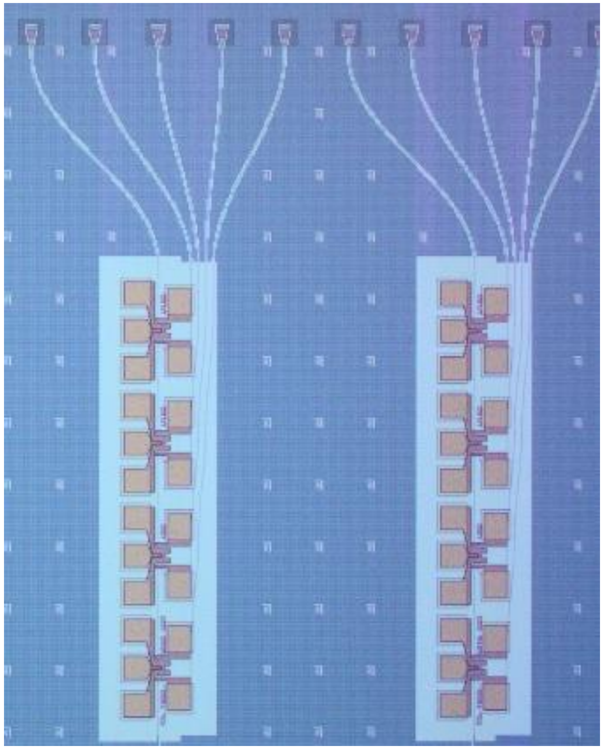
(2016)[SPIEOI] Reboud et al.

MICRORING CHARACTERIZATION

- **Test of various parameters**
  - ring radius
  - coupling factors
- **Assemblies of several rings with different radii for WDM transmission**

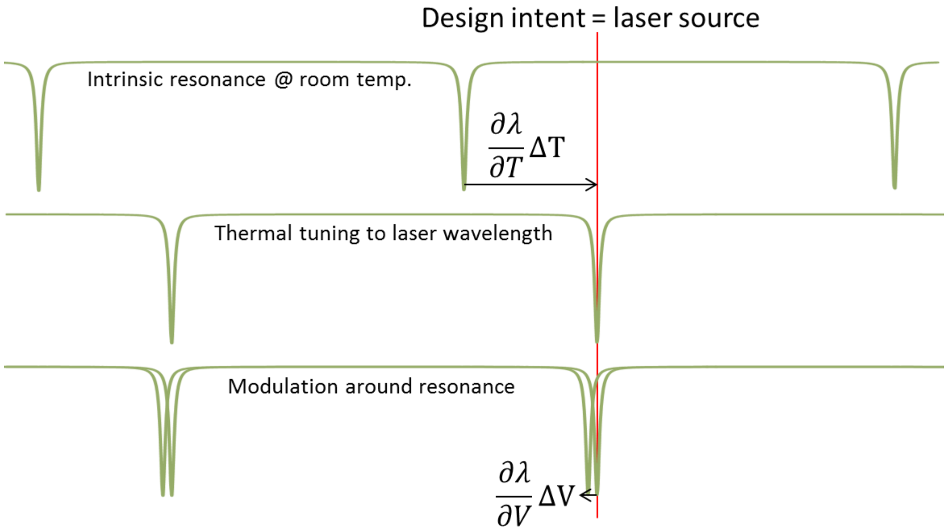




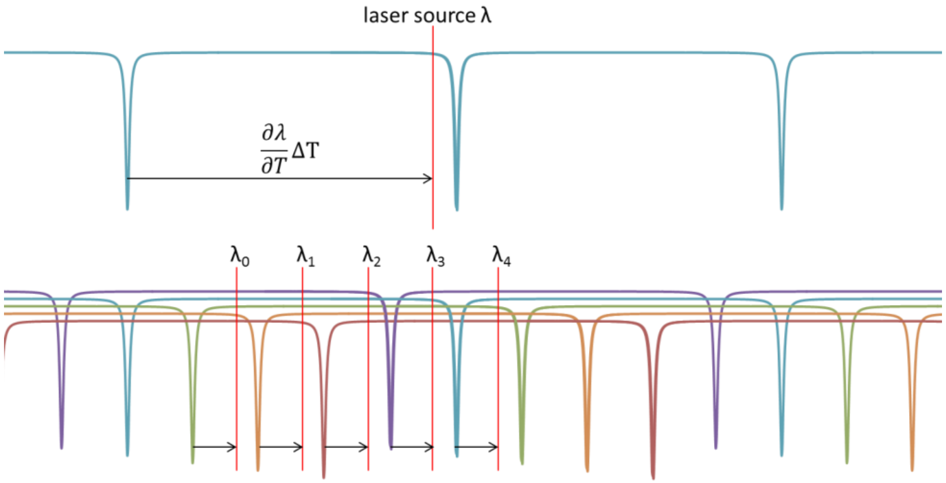


WDM: TAKE BENEFIT OF THE THERMAL SENSITIVITY

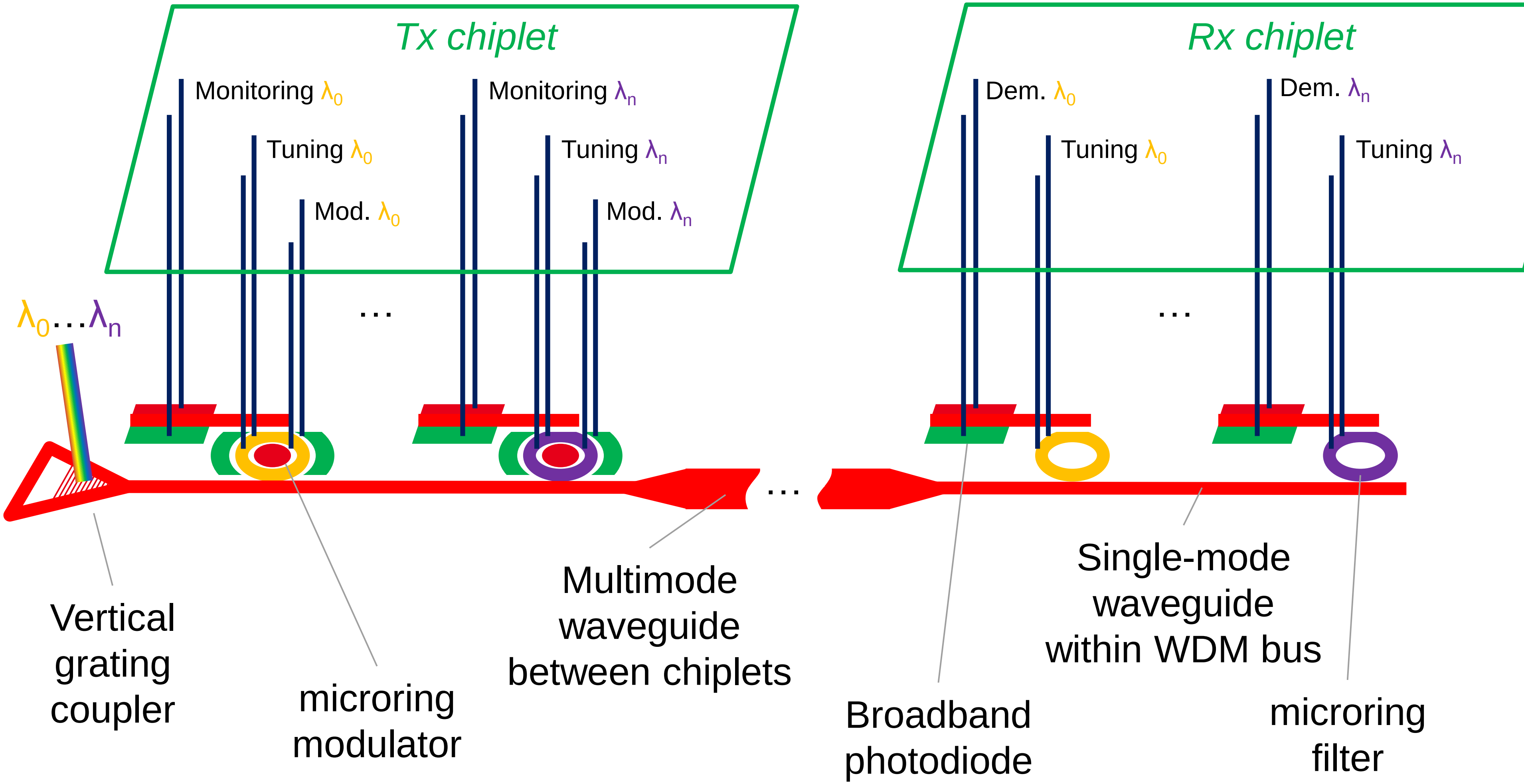
- Low voltage sensitivity requires high Q-factors
- High process variability forbids relying on design-time tuning
- ➔ Use thermal sensitivity to align to laser source



- Yet FSR is large compared to thermal tuning capability
- But WDM allows to use different wavelengths in a single waveguide
- ➔ The total power required to tune the WDM link is no more than to tune a single wavelength
- ➔ Need run-time reallocation of wavelengths for large T° variations

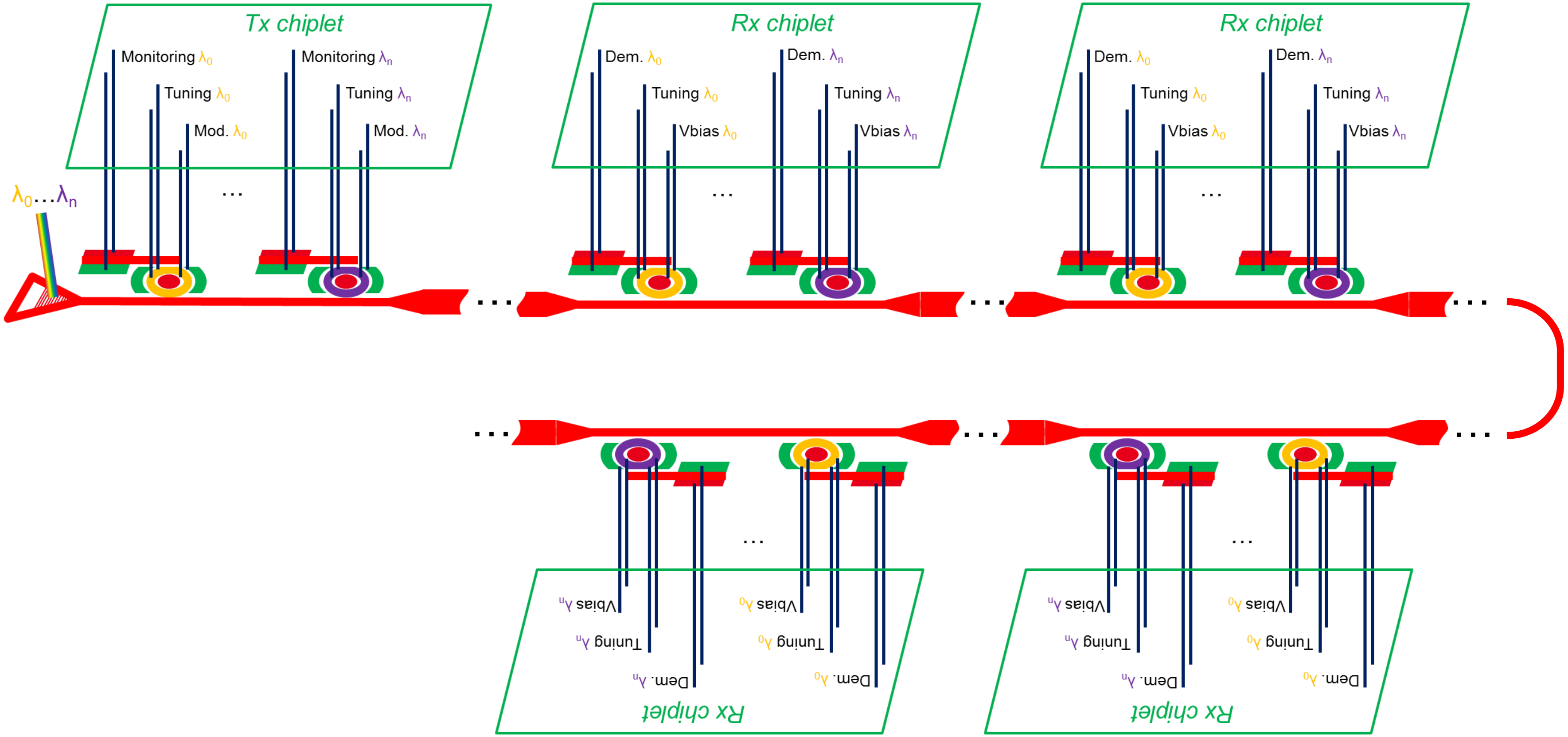


A SINGLE WDM POINT-TO-POINT LINK

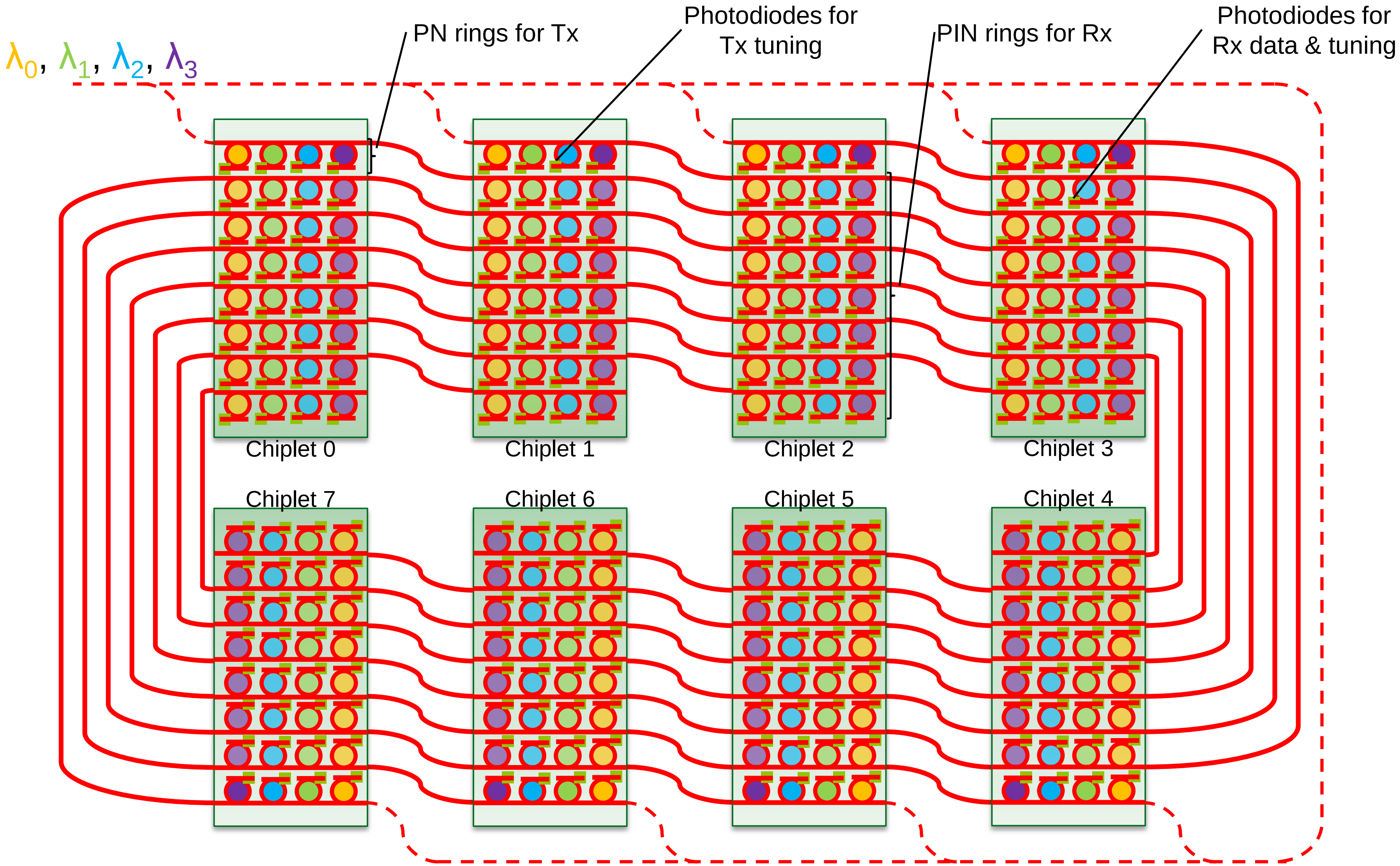


SINGLE-WRITER MULTIPLE READER LINK

- **Cascade several Rx chiplets**
  - Use voltage-controlled PIN ring filters to lock on Tx wavelengths only when active
  - Use higher-level protocol between chiplets to signal transmission



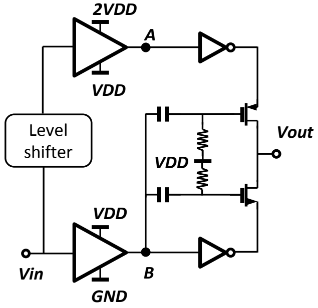
ONOC TOPOLOGY

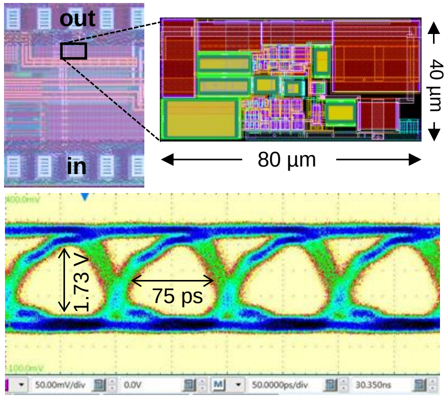


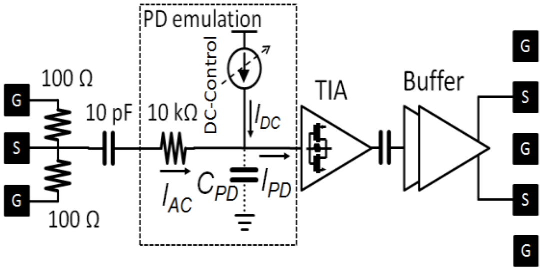
Patent (2013) EP2874334 / US9479256

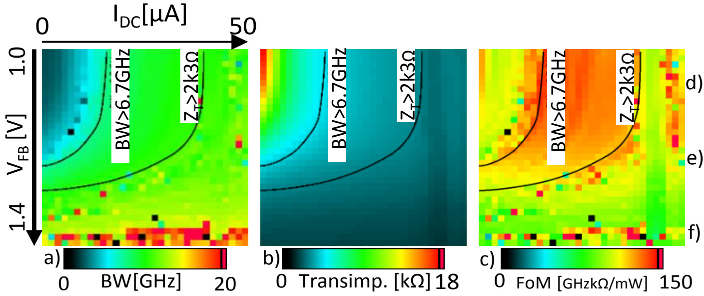
TX AND RX DRIVERS

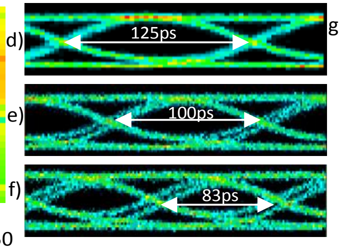
- **Designed in 65nm CMOS @ 8Gbps target**
  - Operational up to 12Gbps
- **Cascoded Tx driver**
  - able to drive a 70 fF modulator with 2.4 V_{pp} swing achieving an efficiency of 537 fJ/bit
- **Rx TIA**
  - does not require input DC current compensation
  - gain-bandwidth/power FoM of 150 THzΩ/mW
  - 23 fJ/bit of consumption for 2.3 kΩ of transimpedance

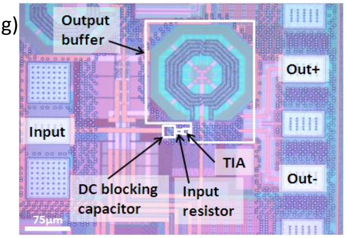








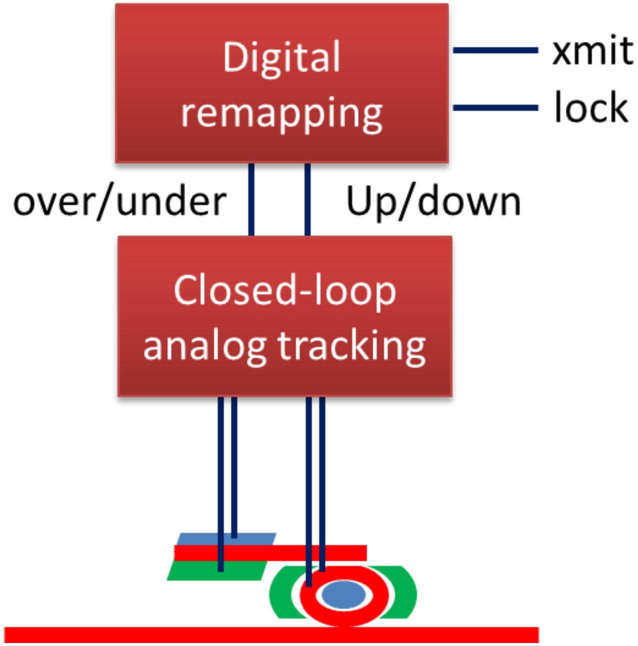




(2016)[SPIEOI] Reboud et al.
(2015)[OIC] Polster et al.
(2016)[NEWCAS] Gonzalez et al.

THERMAL TUNING DRIVER

- **Use of the drop-port of the modulator**
  - Robust closed-loop control
  - Decision thresholds for remapping with hysteresis
  - Digital remapping decision from the different rings of the WDM
  - Automatic remapping to higher/lower wavelength



Digital remapping

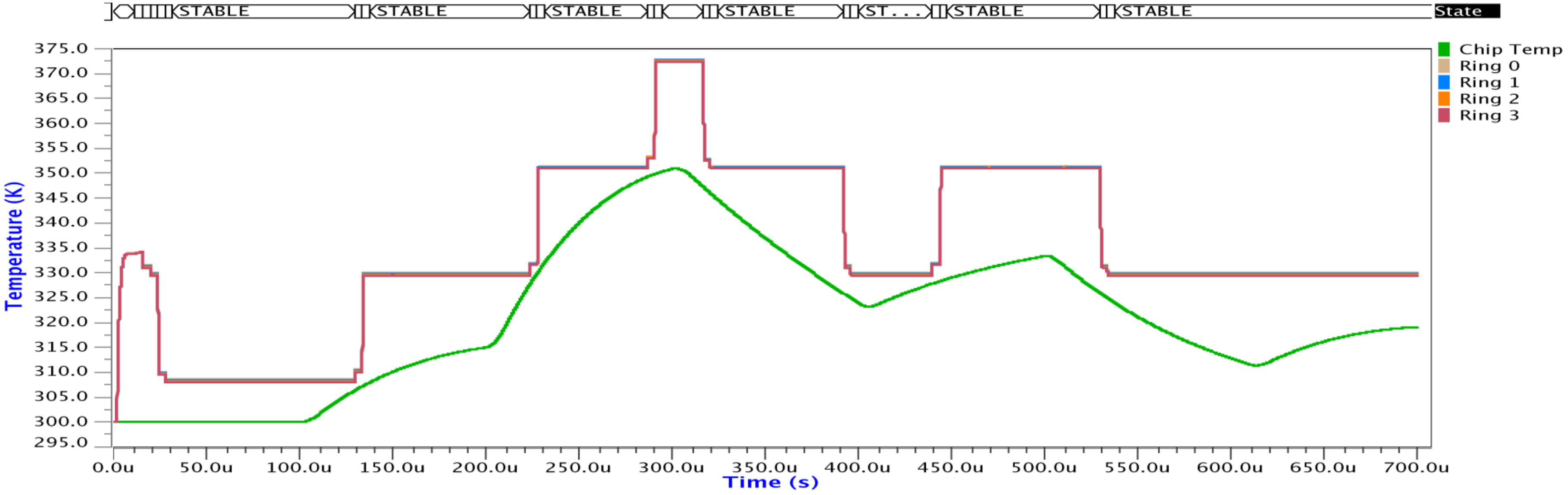
xmit

lock

over/under

Up/down

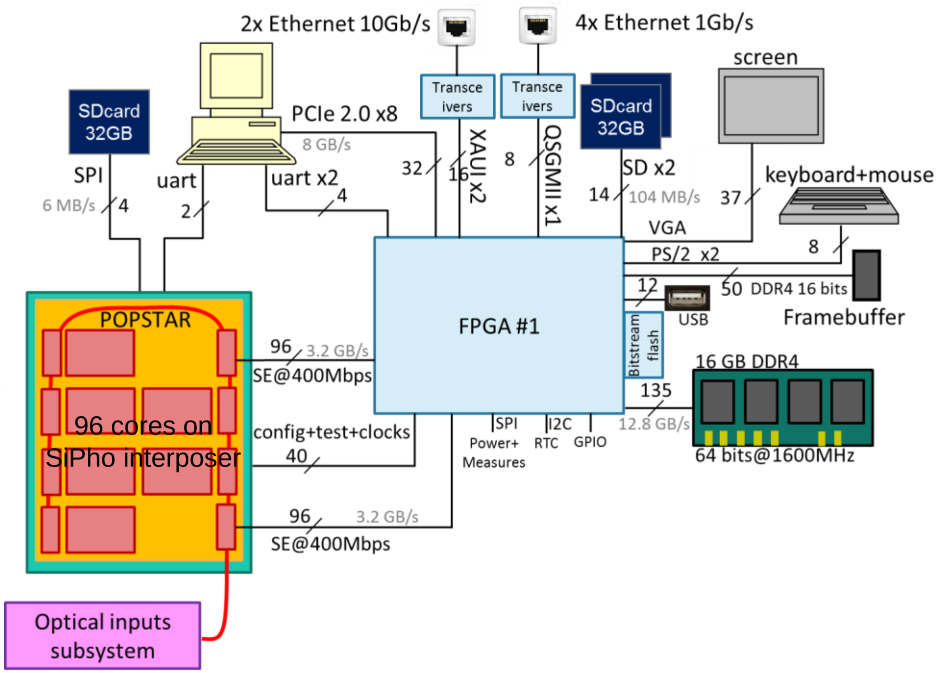
Closed-loop analog tracking

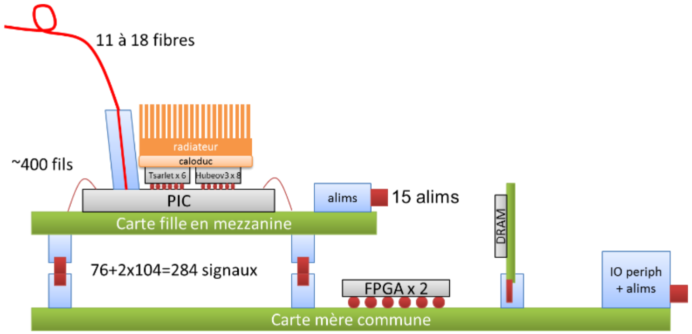


Patent (2014) EP3018526 / US2016131959

POPSTAR : MANYCORE ARCHITECTURE ON A SILICON INTERPOSER

- **POPSTAR : Processors On Photonic Silicon inTerposer Architecture**
- **Our objective: Demonstration of a manycore achitecture with optical routing on a photonic interposer**
  - 96 cores with unified shared memory
  - Peak aggregate bandwidth 576 Gb/s
  - End-to-end latency @0 load < 30ns
  - integrated management for routing, arbitration and flow-control of the optical communications
  - integrated thermal management and tuning of the microrings





CONCLUSION

- **Interposers are key to continue many-core integration**
  - Silicon photonics enables denser integration on interposers, with improved scaling capability
- **At SoC level, efficiency needs to reconsider design, architecture, and even application and partitioning**
  - Innovation is needed on many architectural and technological levels
- **In the long run, with unified optical interfaces for on-chip and off-chip communication, the computation model itself could evolve**

RELATED PUBLICATIONS

- (2016)[TVLSI] Polster, R., Thonnart, Y., Waltener, G., Gonzalez, J.-L., Cassan, E., "Efficiency Optimization of Silicon Photonic Links in 65-nm CMOS and 28-nm FDSOI Technology Nodes", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 24 (12), pp. 3450-3459.
- (2016)[TVLSI] Duong, L.H.K., Wang, Z., Nikdast, M., Xu, J., Yang, P., Wang, Z., Wang, Z., Maeda, R.K.V., Li, H., Wang, X., Le Beux, S., Thonnart, Y., "Coherent and Incoherent Crosstalk Noise Analyses in Interchip/Intrachip Optical Interconnection Networks", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 24 (7), pp. 2475-2487.
- (2016)[OIC] Bahadori, M., Polster, R., Rumley, S., Thonnart, Y., Gonzalez-Jimenez, J.-L., Bergman, K., "Energy-bandwidth design exploration of silicon photonic interconnects in 65nm CMOS", 5th IEEE Photonics Society Optical Interconnects Conference, OI 2016, pp. 2-3.
- (2016)[SPIEOI] Reboud, V., Blampey, B., Gindre, P., Dubray, O., Fowler, D., Lemonnier, O., Grellier, E., Fournier, M., Thonnart, Y., Bernabe, S., "Experimental study of silicon ring resonators and ultra-low losses waveguides for efficient silicon optical interposers", Proceedings of SPIE - The International Society for Optical Engineering, 9753.
- (2016)[NEWCAS] Gonzalez, J.L., Polster, R., Waltener, G., Thonnart, Y., Cassan, E., "10 Gbps, 560 fJ/b TIA and modulator driver for optical networks-on-chip in CMOS 65nm", 14th IEEE International NEWCAS Conference, NEWCAS 2016.
- (2015)[MWSCAS] Polster, R., Gonzalez Jimenez, J.L., Miro-Panades, I., Cassan, E., "An optical clock receiver based on an injection locked ring oscillator featuring auto-calibration", Midwest Symposium on Circuits and Systems, 2015-September.
- (2015)[NEWCAS] Polster, R., Jimenez, J.-L.G., Cassan, E., "A novel optical integrate and dump receiver for clocking signals", Conference Proceedings - 13th IEEE International NEW Circuits and Systems Conference, NEWCAS 2015.
- (2015)[OIC] Polster, R., Jimenez, J.L.G., Cassan, E., Vivien, L., "A TIA for optical networks-on-chip in 65nm CMOS", 2015 IEEE Optical Interconnects Conference, OI 2015, pp. 109-110.
- (2015)[DATE] Duong, L.H.K., Nikdast, M., Xu, J., Wang, Z., Thonnart, Y., Le Beux, S., Yang, P., Wu, X., Wang, Z., "Coherent crosstalk noise analyses in ring-based optical interconnects", Proceedings -Design, Automation and Test in Europe, DATE, 2015-April, pp. 501-506.
- (2015)[NOCS] Thonnart, Y., Zid, M., "Technology assessment of silicon interposers for manycore SoCs: Active, passive, or optical?", Proceedings - 2014 8th IEEE/ACM International Symposium on Networks-on-Chip, NoCS 2014, pp. 168-169.
- (2015)[DAC] Li, H., Le Beux, S., Thonnart, Y., O'Connor, I., "Complementary communication path for energy efficient on-chip optical interconnects", Proceedings - Design Automation Conference, 2015-July.
- (2014)[OIC] Polster, R., Jimenez, J.L.G., Cassan, E., Vincent, P., "Optimization of TIA topologies in a 65nm CMOS process", 2014 IEEE Optical Interconnects Conference, OI 2014, pp. 117-118.
- (2014)[PRIME] Polster, R., Jimenez, J.-L.G., Cassan, E., "TIA optimization for optical network receivers for multi-core systems-in-package", Conference Proceedings - 10th Conference on Ph. D. Research in Microelectronics and Electronics, PRIME 2014.

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