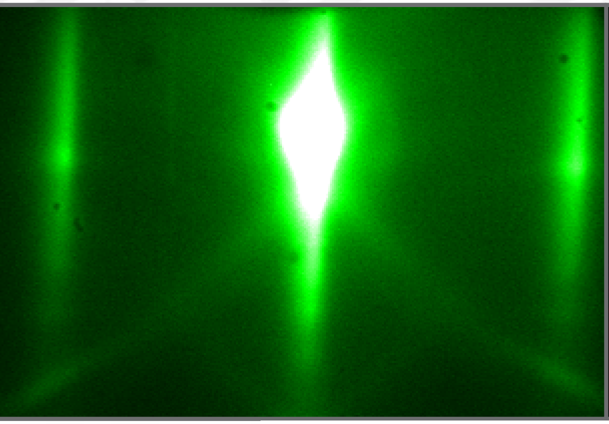
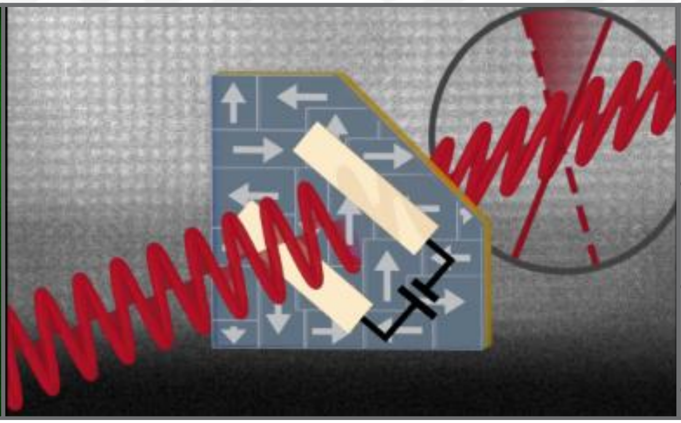
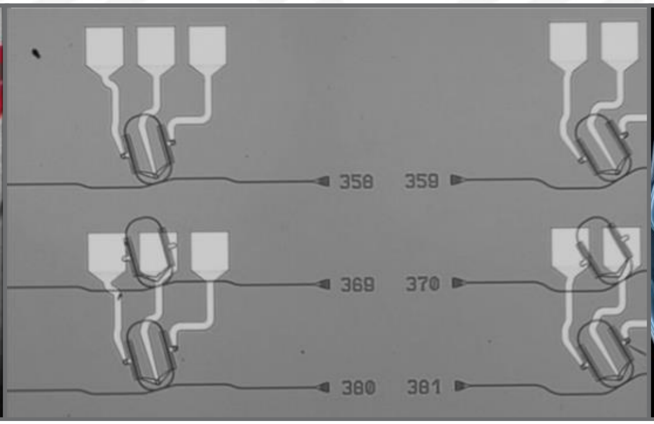
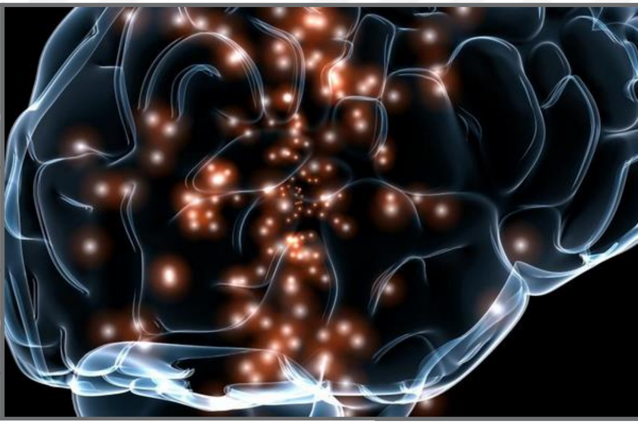
Silicon Photonics Technology for Advanced Computing Applications

Bert Jan Offrein









OPTICS

Dresden, March 23, 2018

Optical/Photonic Interconnects for Computing Systems

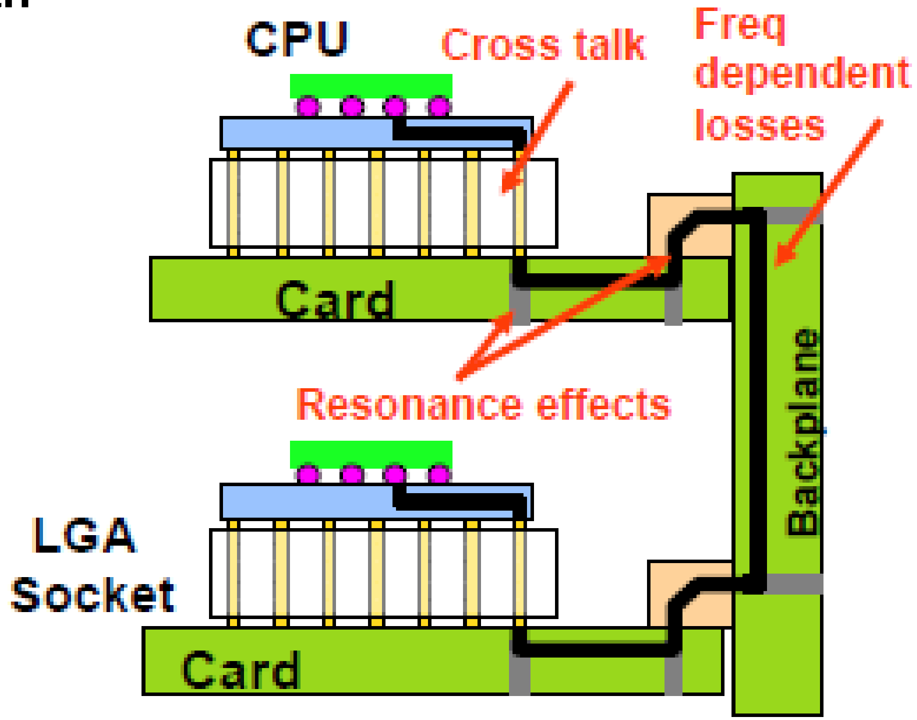
Neuromorphic Devices and Systems Group

Outline

- **Photonics and computing?**
  - The interconnect bottleneck
  - The Von Neumann Bottleneck
- **Optical interconnects for computing systems**
  - Optical interconnects roadmap
  - CMOS Silicon Photonics
  - Novel functionalities by adding new materials
- **Photonic synaptic elements for Neural Networks**
  - Motivation
  - Photonic Synaptic Processor
  - Non-volatile optical memory elements
- **Conclusions**

Why Optics – The interconnect bottleneck

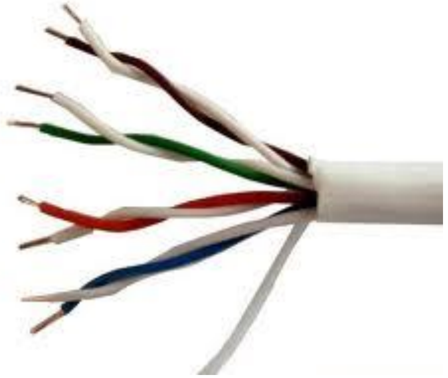
- **Physics of electrical links - going towards higher bandwidth**
  - Increased loss
  - Increased crosstalk
  - Resonant effects



- **Physics of optical links – 190 THz EM waves**
  - 50 THz Bandwidth available (1300-1600 nm)

- **Larger bandwidth X length product of optics**
  - Electrical coax cable: ~ 100 MHz km
  - Multimode fiber: ~ 500 MHz km
  - Single mode fiber: > 5000 MHz km

- **Lower propagation loss of optical cables**
  - Electrical coax cable: ~ 1 dB/m
  - Multimode fiber: ~ 3 dB/km
  - Single mode fiber: > 0.3 dB/km



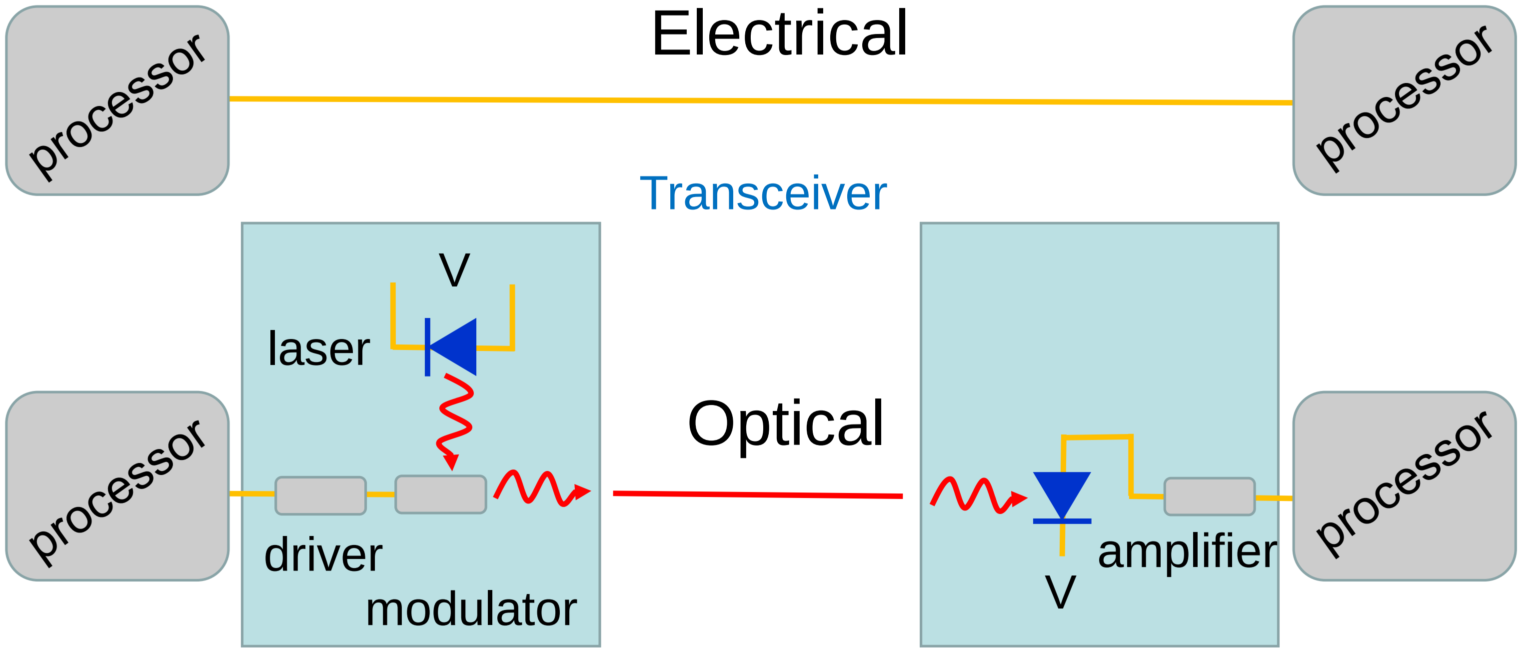
- **Power efficiency**

- **Larger density of optical links**

Electrical and Optical Communication between two processors

Physics of RF EM waves
The signal is the carrier

Physics of optical EM waves
The signal is modulated on an optical carrier



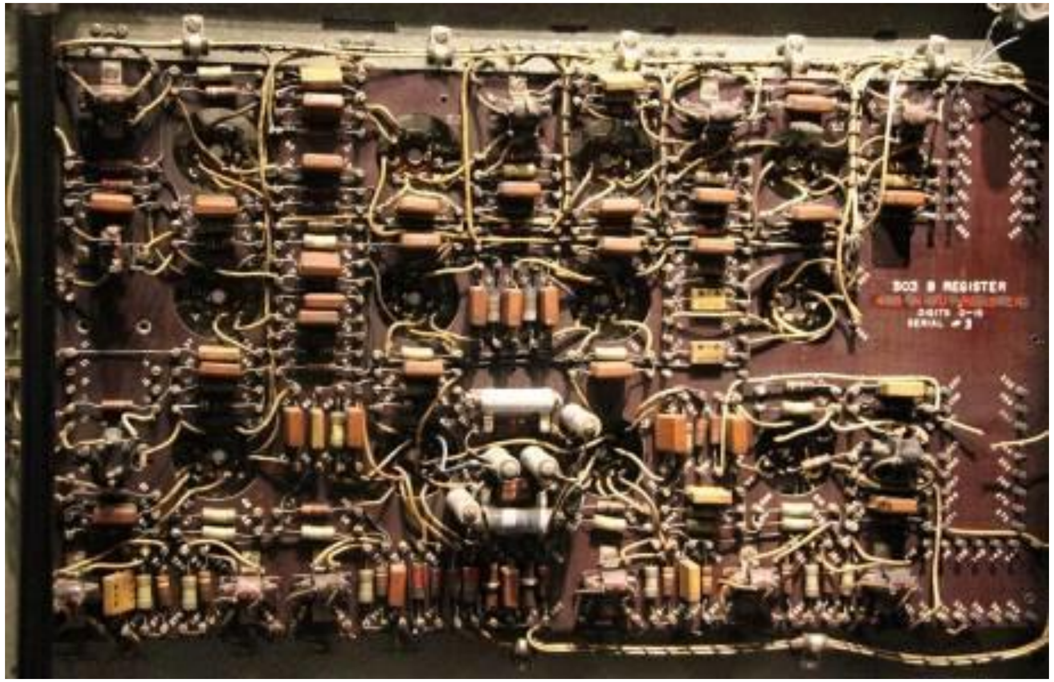
Optical communication:

- 1000 x Larger bandwidth
- 1000 x Lower loss
- 100 x Larger distance

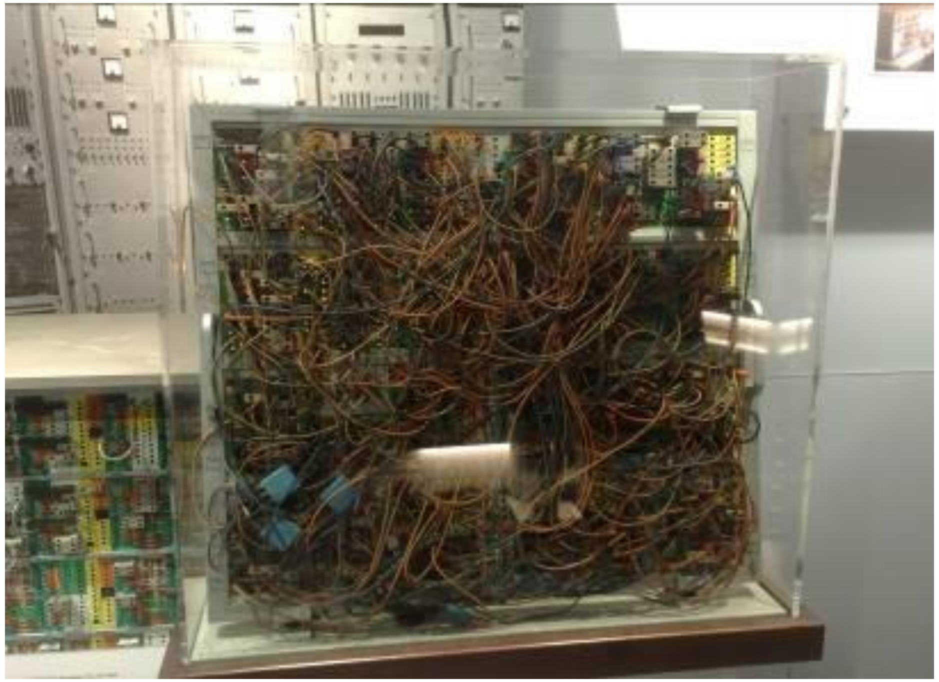
Scalability & Power efficiency !!!

However, many more components and assembly steps required !!!

Integration? Looking back, electronics



Whirlwind, MIT, 1952



EAI 580 patch panel, Electronic Associates, 1968

Pictures taken at: Computer History Museum

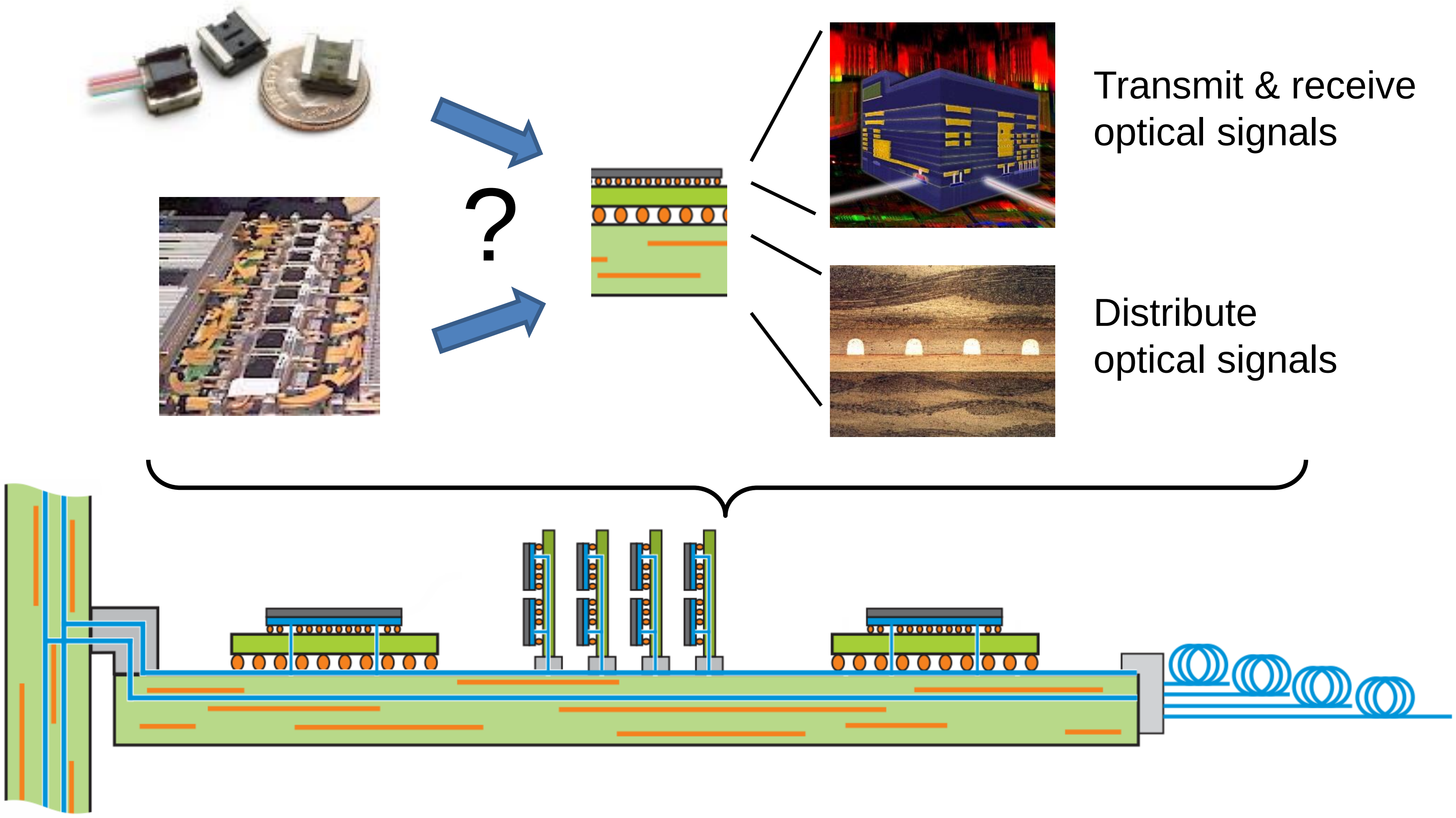
Today's state of computing is based on:

- Integration and scaling of the <u>logic functions</u> (CMOS electronics)
- Integration and scaling of the <u>interconnects</u> (PCB technology & assembly)

For optical interconnects, this resembles:

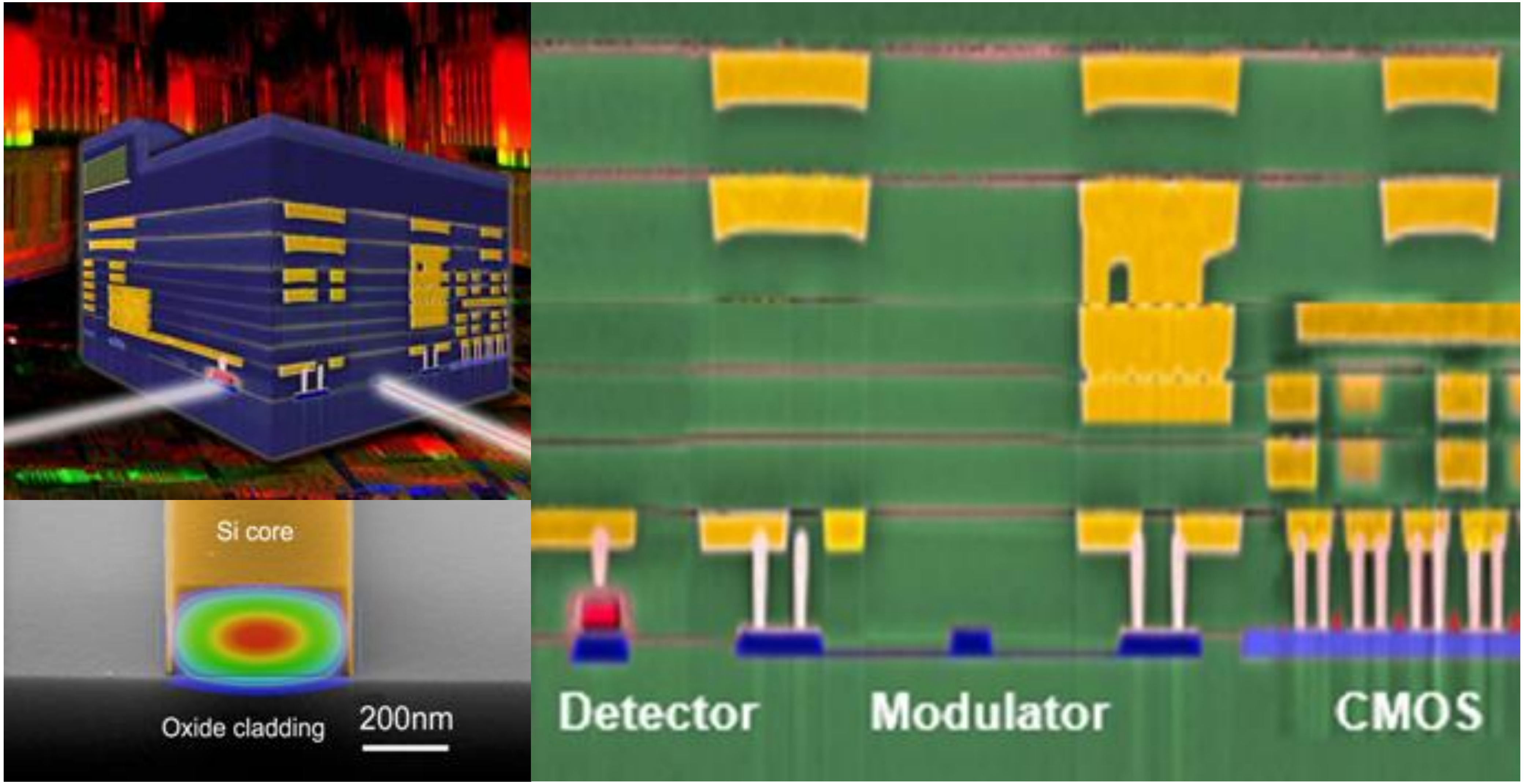
- Electro-optical integration and scaling of <u>transceiver technology</u>
- Integration of optical <u>connectivity</u> and signal <u>distribution</u>

Could one INTEGRATE the electrical and optical functions into the system?



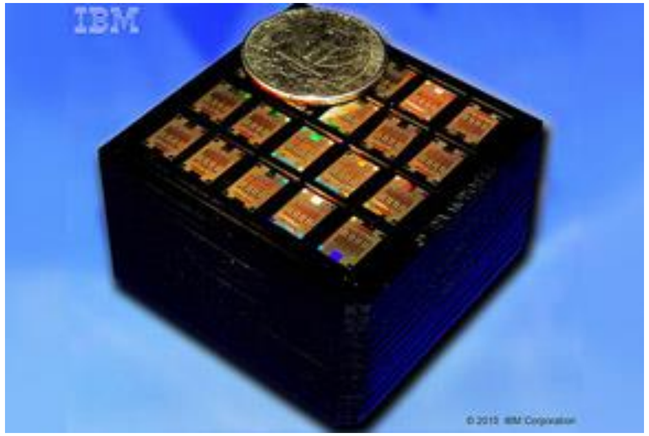
Vision: Electrical and optical communication embedded in a computing system

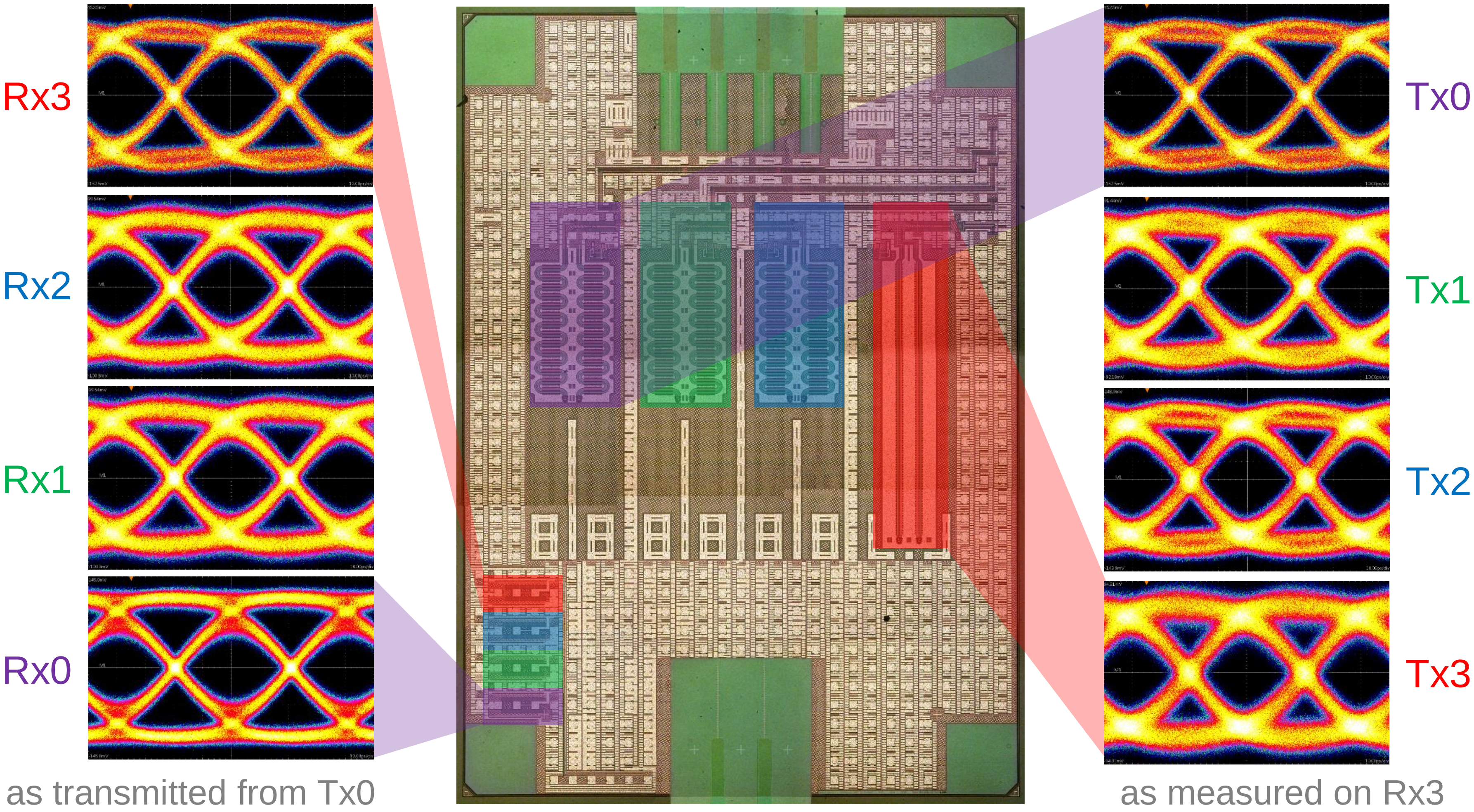
CMOS Silicon photonics



Integrate electrical **& optical** functions in silicon

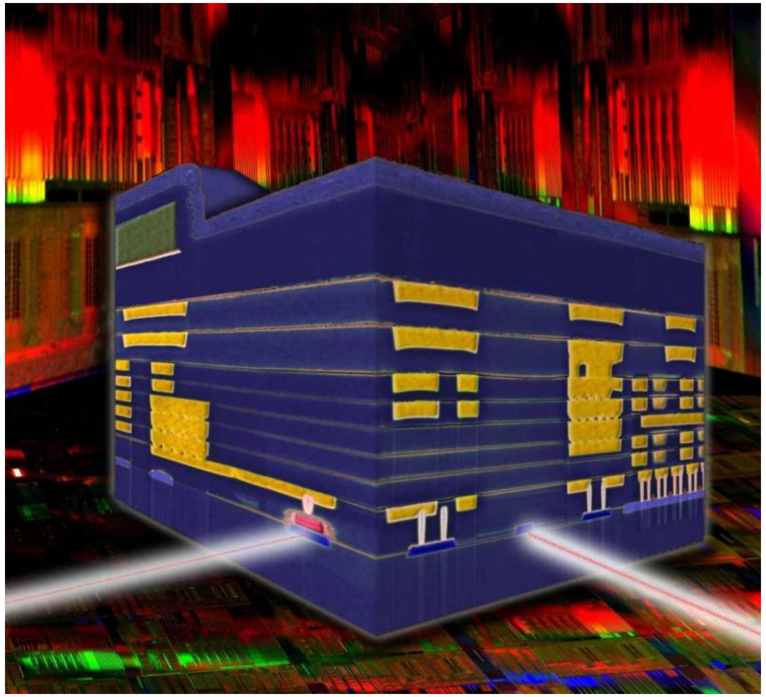
4 λ x 25 Gb/s optical transceiver demonstration



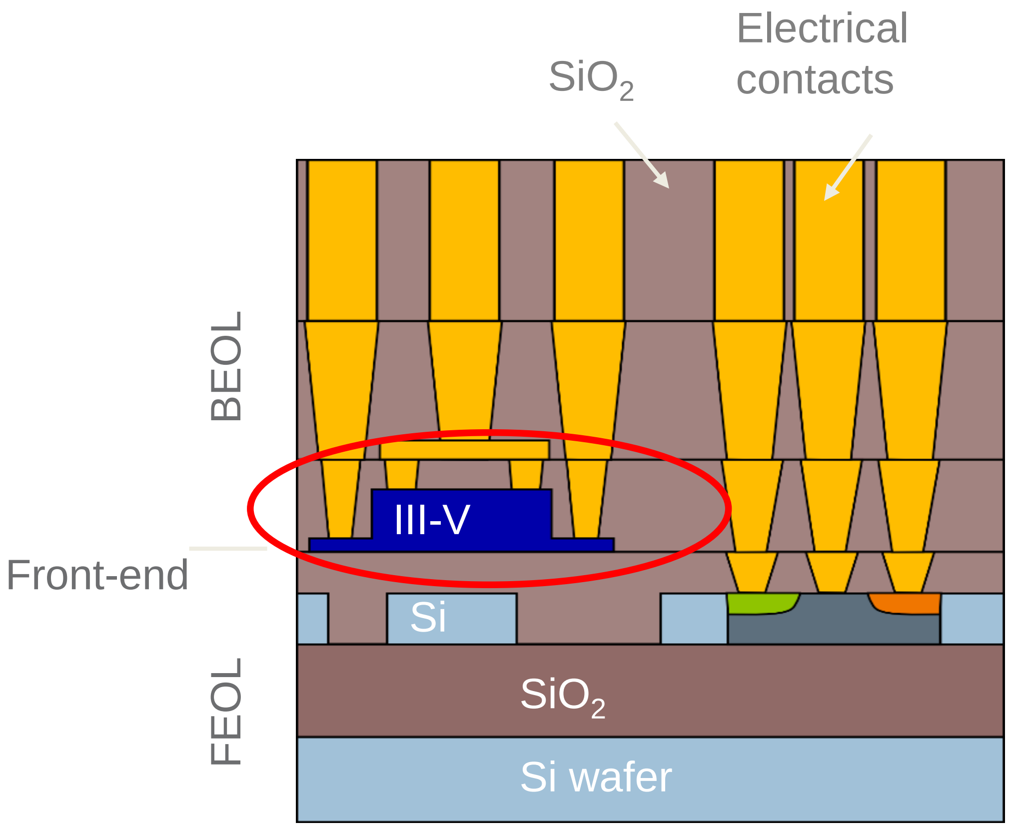


Demonstration of a flip chip mounted 100G transceiver with four wavelength multiplexing at 25 Gb/s each.

CMOS Embedded III-V on silicon technology



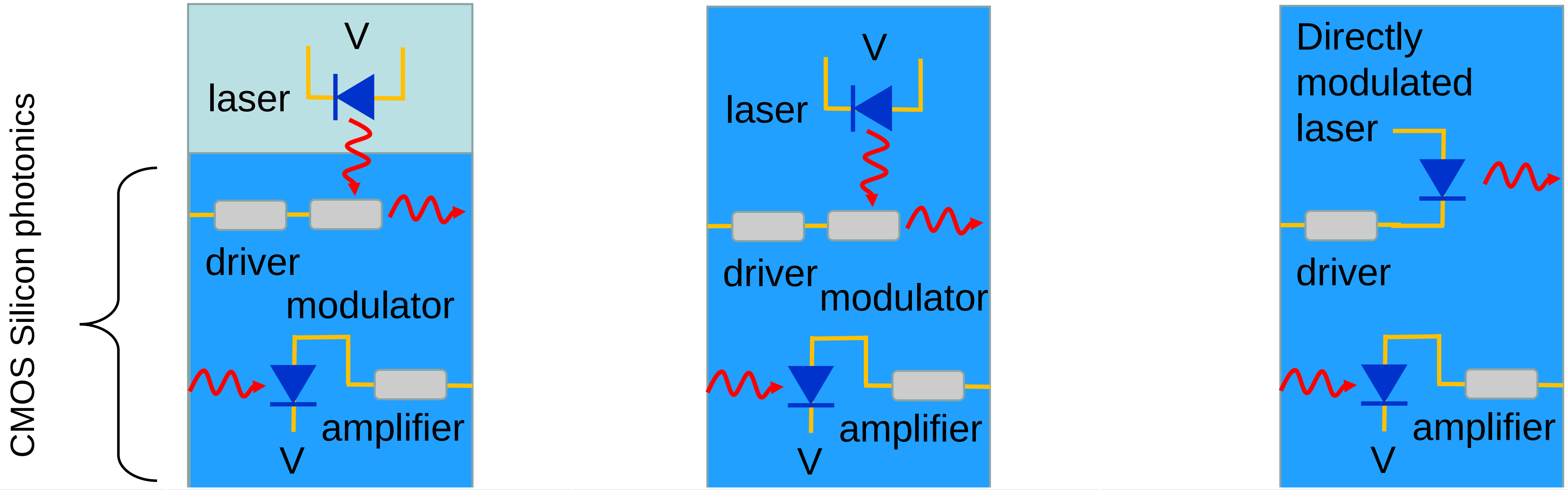
CMOS Si Photonics



… + III-V functionality

- **Overcome discrete laser and assembly cost**
- **New functions, directly combining electronics, passive and active photonics**

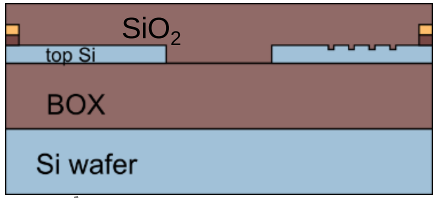
Silicon photonics integration roadmap



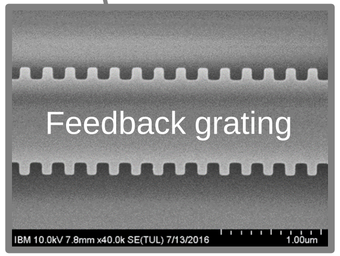
Laser specs			
Wavelength	1300 nm		
Optical Power	20 mW	10 mW	2.5 mW
Electrical Power	200 mW	100 mW	50 mW
Total link power @ 25 Gb/s	Laser: 200 mW Modulator: 900 mW TIA: 100 mW Total: 1200 mW	Laser: 100 mW Modulator: 900 mW TIA: 100 mW Total: 1100 mW	Laser: 50 mW Laser driver: 100 mW TIA: 100 mW Total: 250 mW

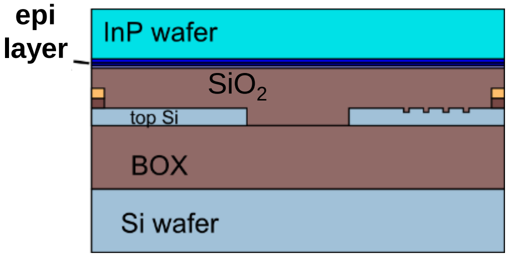
Processing scheme

- 5 InAlGaAs quantum wells (MOCVD)

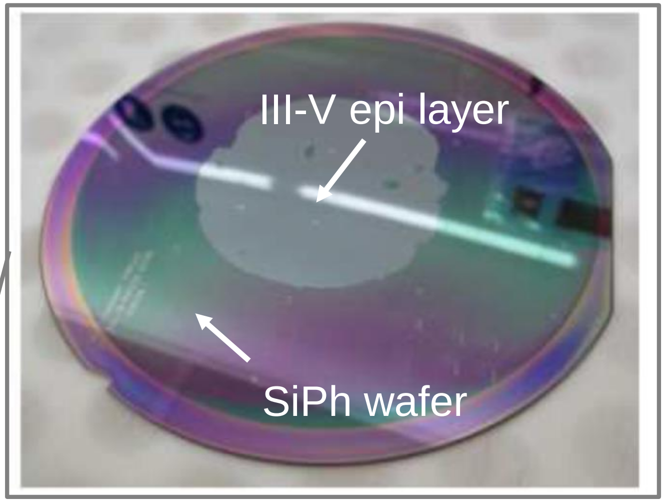


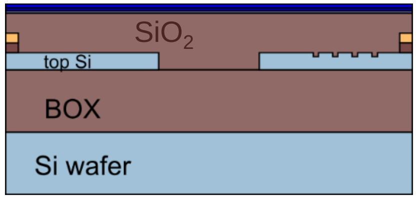
SiPh wafer



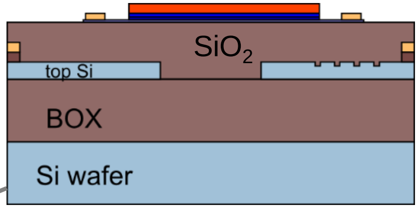


Wafer bonding

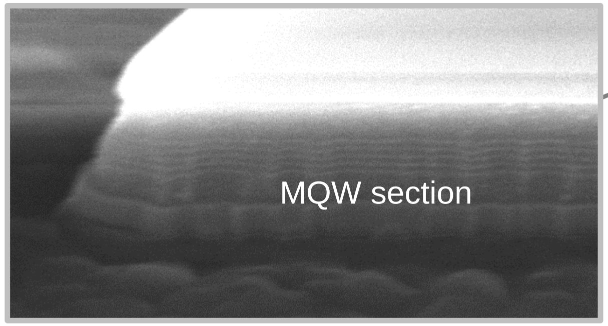


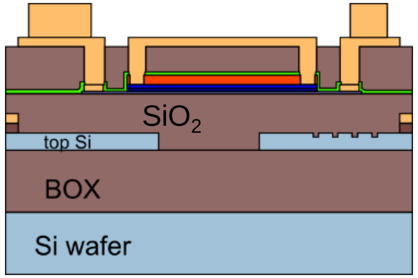


Substrate removal



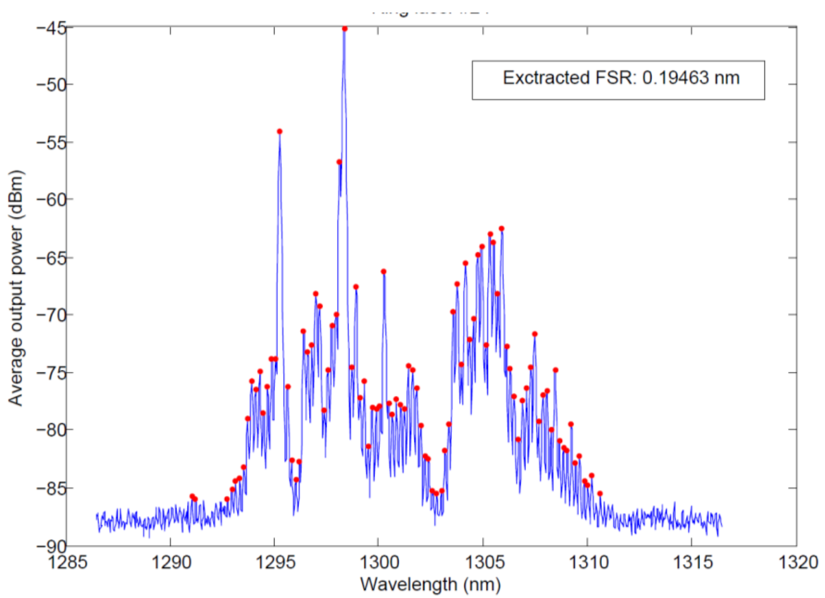
III-V structuring





Metallization

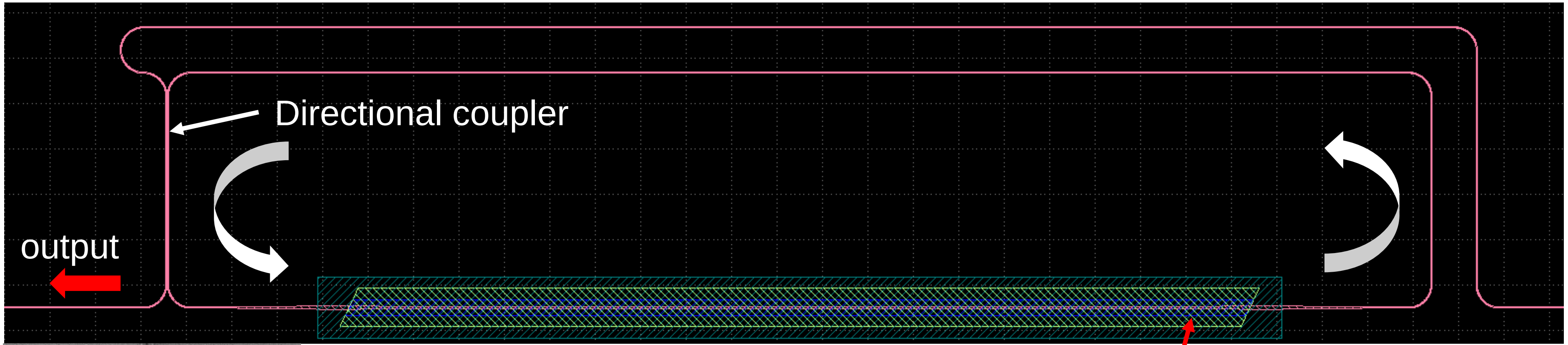
Optically pumped ring laser

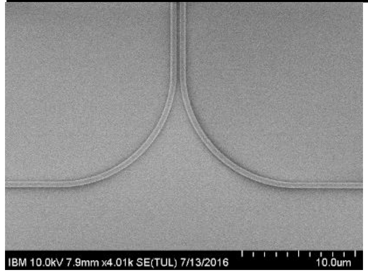


Measured FSR: 0.194 nm

Estimated FSR from ring: 0.203 nm
Estimated FSR from III-V: 0.266 nm

- Lasing with feedback from silicon photonics





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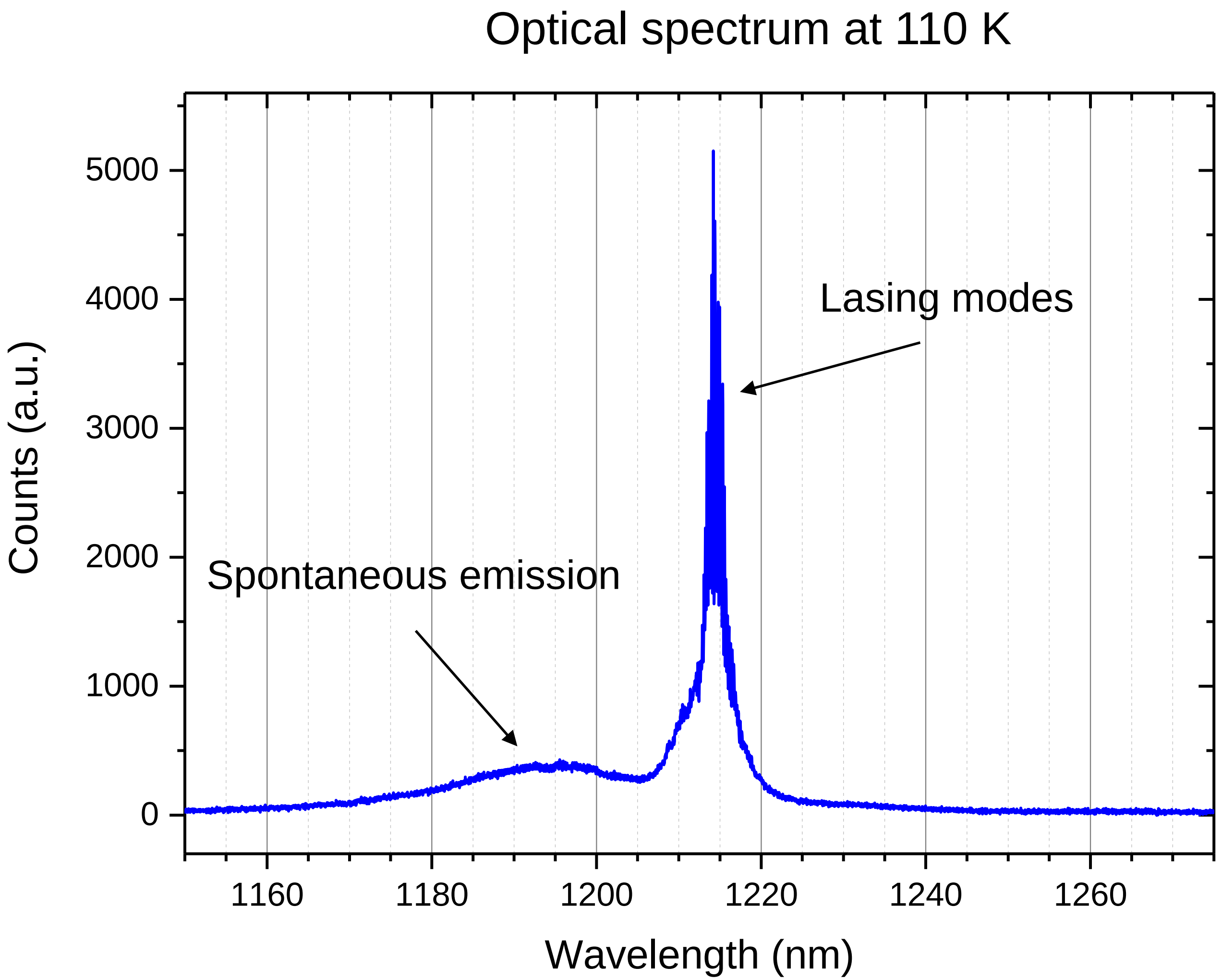
Electrically pumped lasing



- Laser devices: 10 dB optical loss at room temperature
- Cooling down increases gain
- Increased gain can overcome loss
- Pulsed electrical pumping

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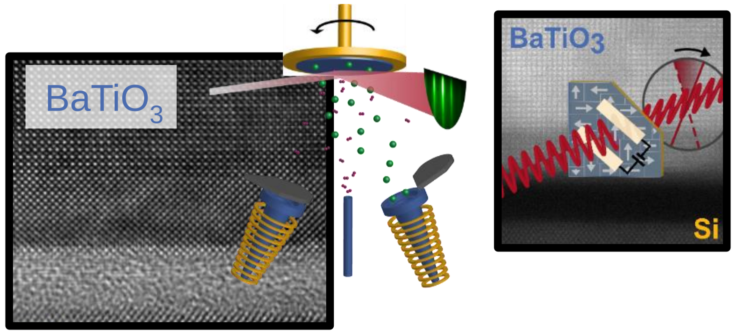
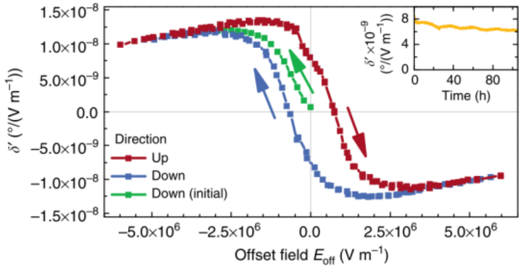
Electro-optical integration – building block overview



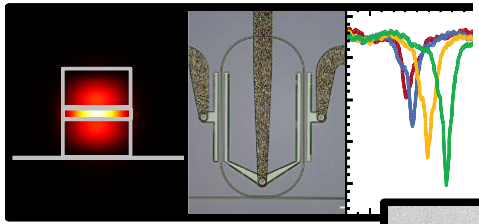
Materials fabrication

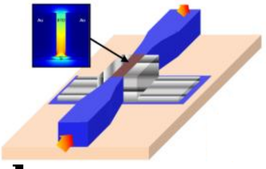
- MBE deposition of epitaxial oxides
- High-k dieelectrics
- TEM, XRD, AFM, XPS, …

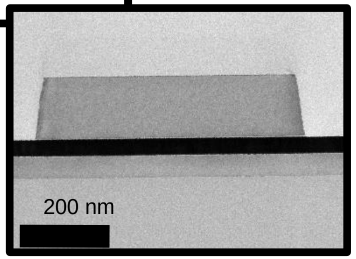


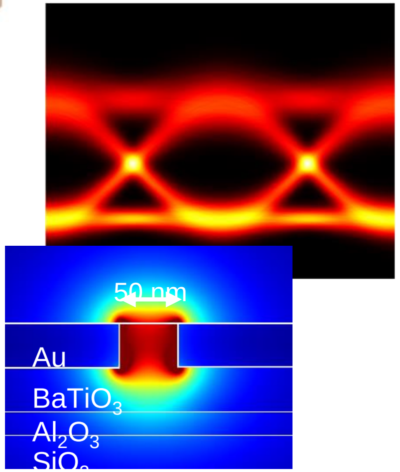
Materials characterization

- Optical nonlinearities
- Ferroelectricity
- Metal-insulator phase transitions





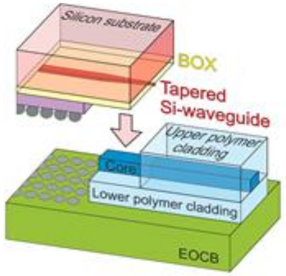




Integrated photonics

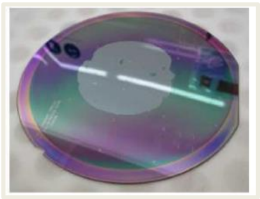
- Novel modulators & tuning elements

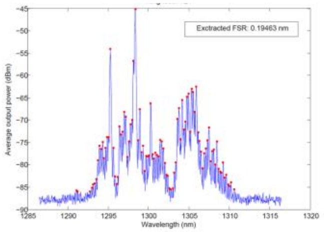
Neuromorphic Devices and systems – relevant expertise –



Silicon photonics packaging

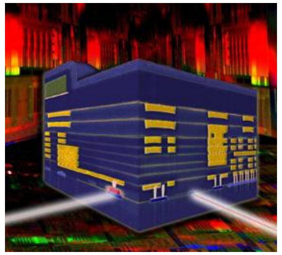
- >100 broadband optical IO to Si Ph

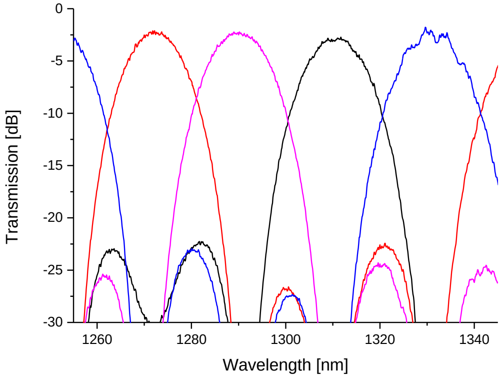




III-V on Si Photonics

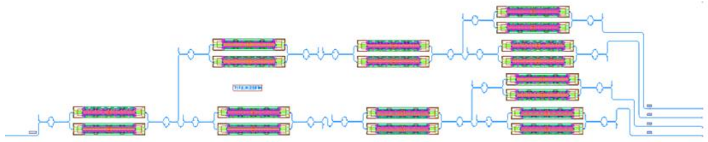
- CMOS embedded III-V devices
- III/V light sources & detectors





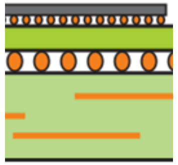
CMOS Silicon photonics

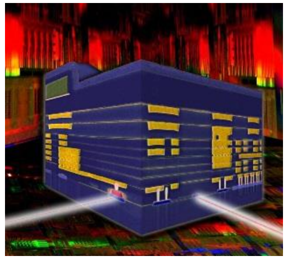
- Integrated optic devices
- Wavelength filters



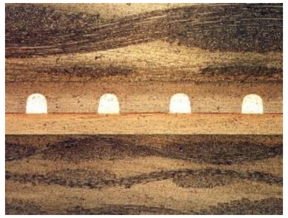
Could one INTEGRATE the optical functions into the system?

?

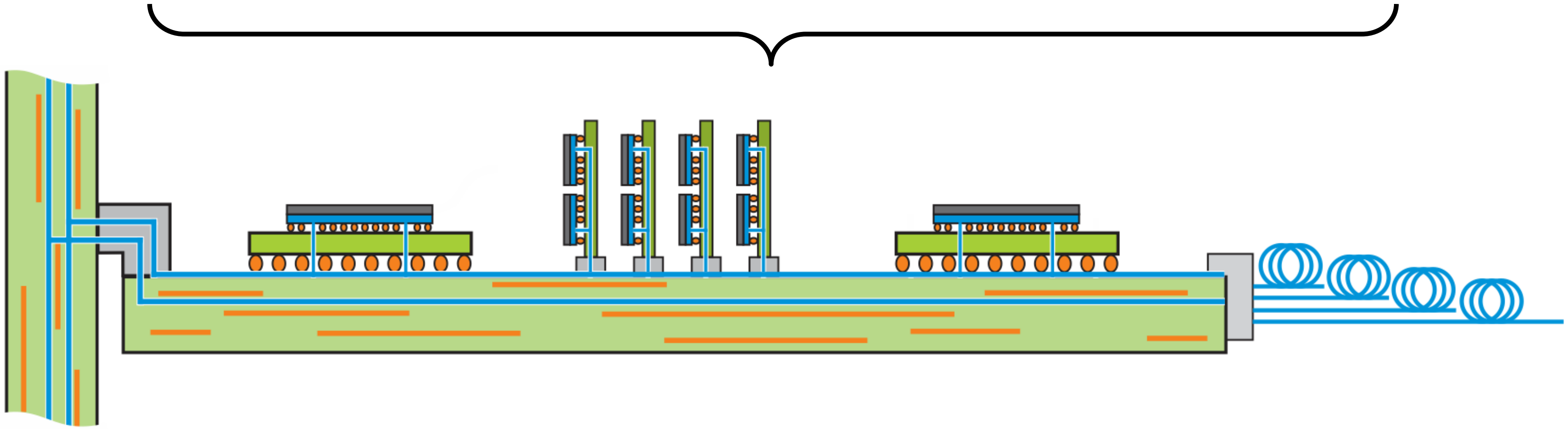




Transmit & receive optical signals



Distribute optical signals



Vision: Electrical and optical communication embedded in a computing system

Outline

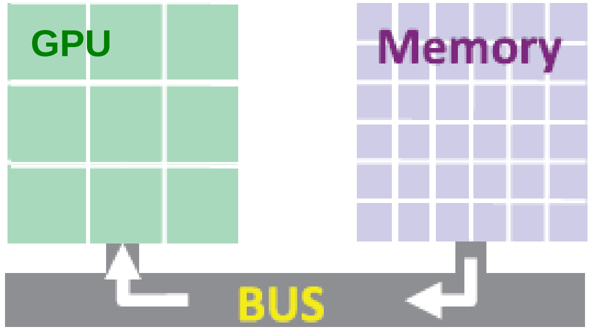
- **Photonics and computing?**
  - The interconnect bottleneck
  - The Von Neumann Bottleneck

- **Optical interconnects for computing systems**
  - Optical interconnects roadmap
  - CMOS Silicon Photonics
  - Novel functionalities by adding new materials

- **Photonic synaptic elements for Neural Networks**
  - Motivation
  - Photonic Synaptic Processor
  - Non-volatile optical memory elements

- **Conclusions**

Neuromorphic hardware for big data analytics

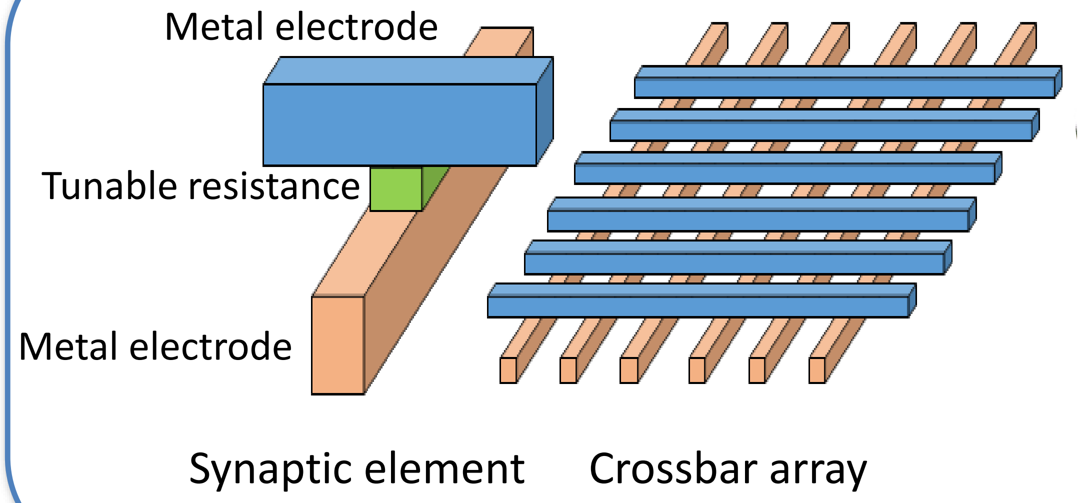


- **Today's status on deep neural networks**
  - Software based on Von Neumann systems
  - Training is the bottleneck – HPC required
  - GPU accelerators – **processing - memory bottleneck**

- **Fast and efficient neural network data processing**

1. Analog approximate signal processing
2. Tight integration of processing and memory
   – 10'000x improvement using crossbar arrays

- **Hardware implementations**
  – *Electrical* crossbar arrays
  – *Photonic* crossbar arrays

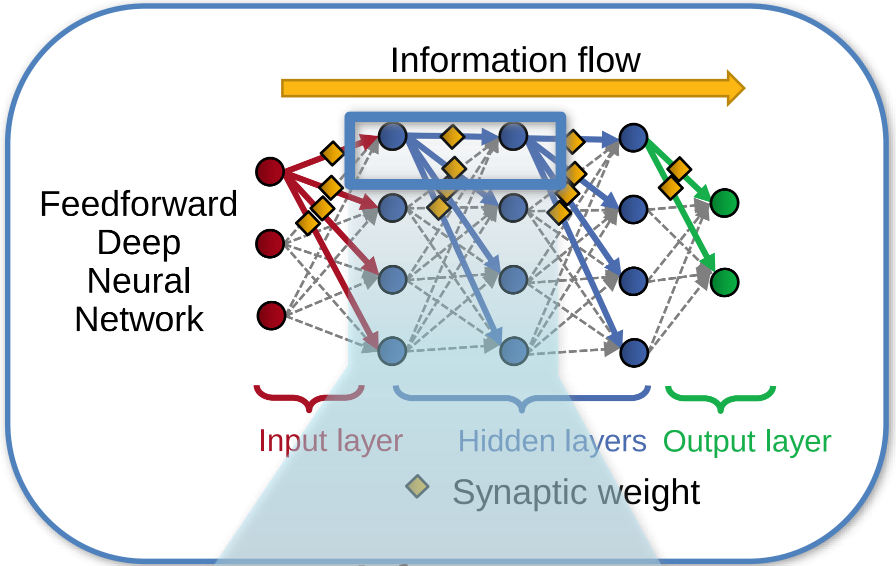


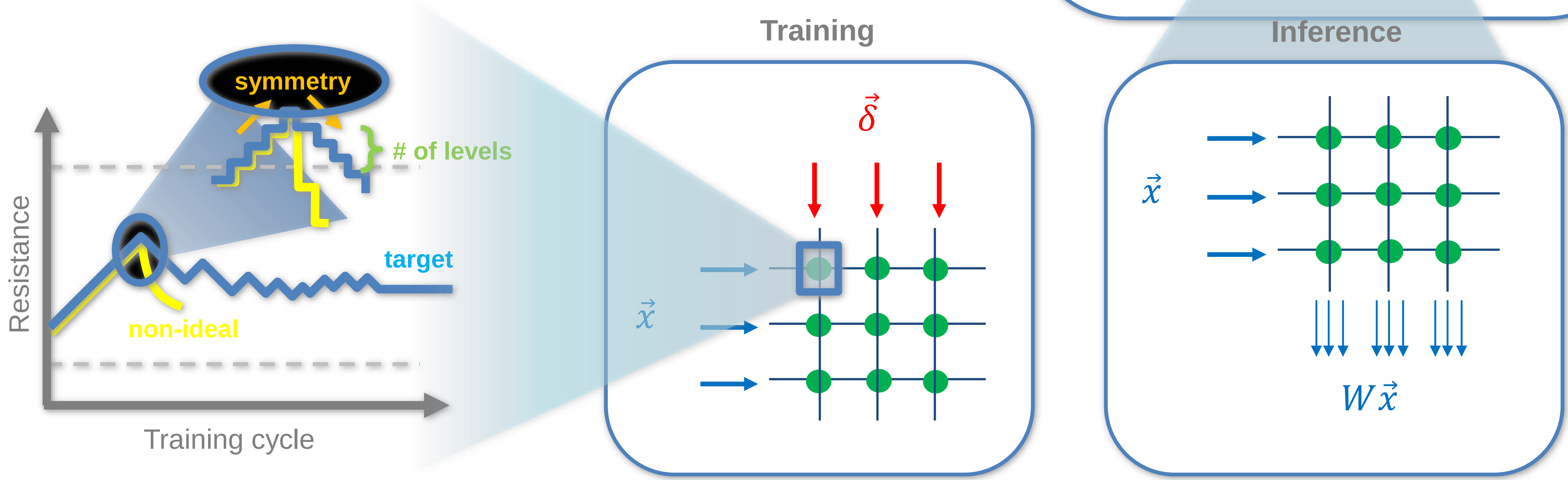
Accelerated learning: Analog crossbar arrays

Update weight proportional to signals on crossbar row and column

- Increase and decrease of weight
- Symmetric behavior for positive and negative updates
- High weight resolution (~1000 levels) required

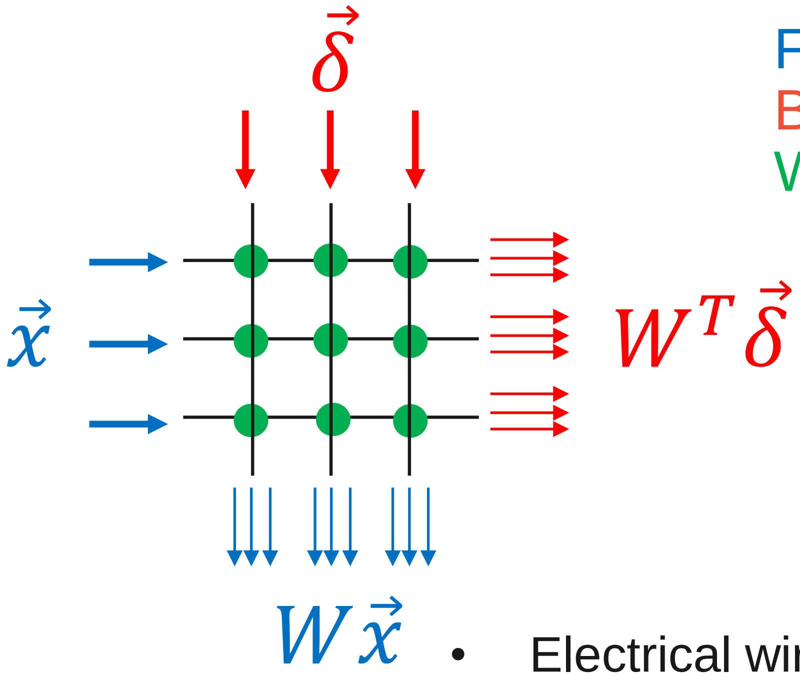
Physical challenge: Identify material systems fulfilling those requirements





Photonic crossbar unit - operating principle

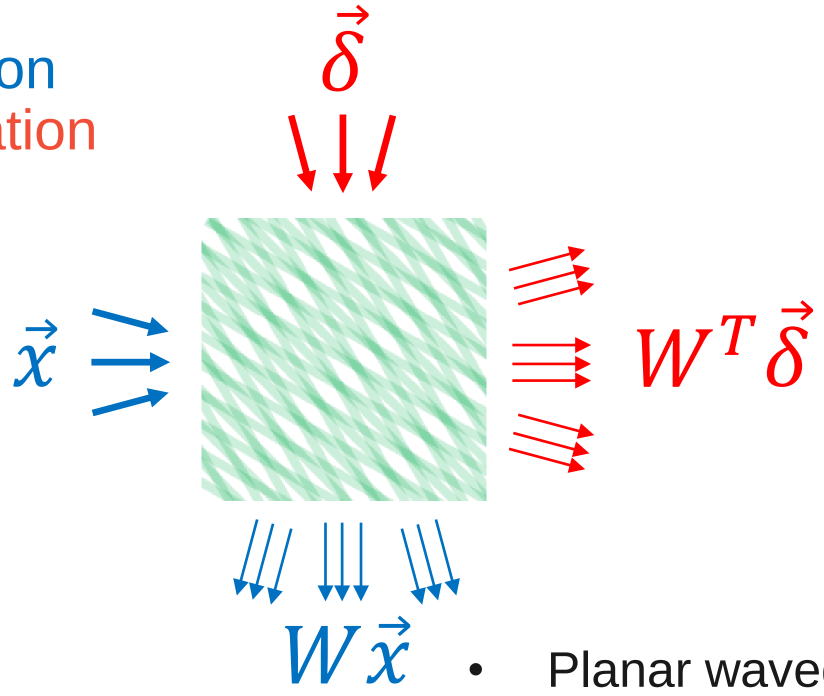
Electrical crossbar



- Electrical wires
- Local weights
- Resistance tuning

Forward propagation
Backward propagation
Weights

Photonic crossbar

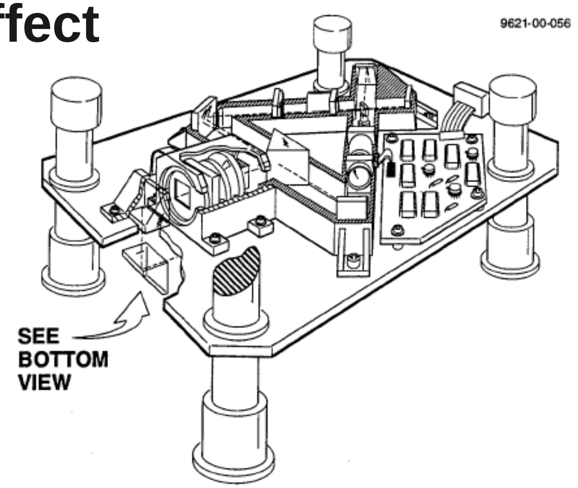


- Planar waveguiding
- Distributed weights
- Refractive index tuning

Writable photorefractive gratings provide the same functionality as the tunable resistive elements in a crossbar unit

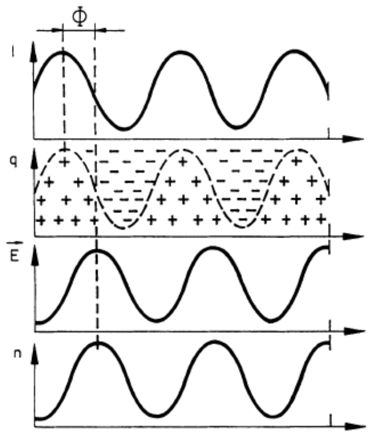
Photonic crossbar unit

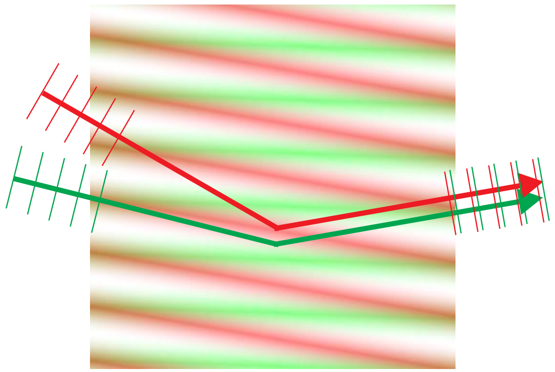
- **Alternative crossbar physical principle leveraging the photorefractive effect**
  - Demonstrated in 3D free space photonic neural networks in the 90s
    - i.e. Hughes Research Laboratories
  - New developments we can leverage
    - *Integrated* optic technology
    - Co-integration of new materials



- **Non-volatile weights applying the photorefractive effect**
    - Grating writing by interference of optical plane waves in an electro-optic material

      Strength proportional to product of the amplitudes of the writing beams
    - Written grating acts as the synaptic interface between plane optical waves

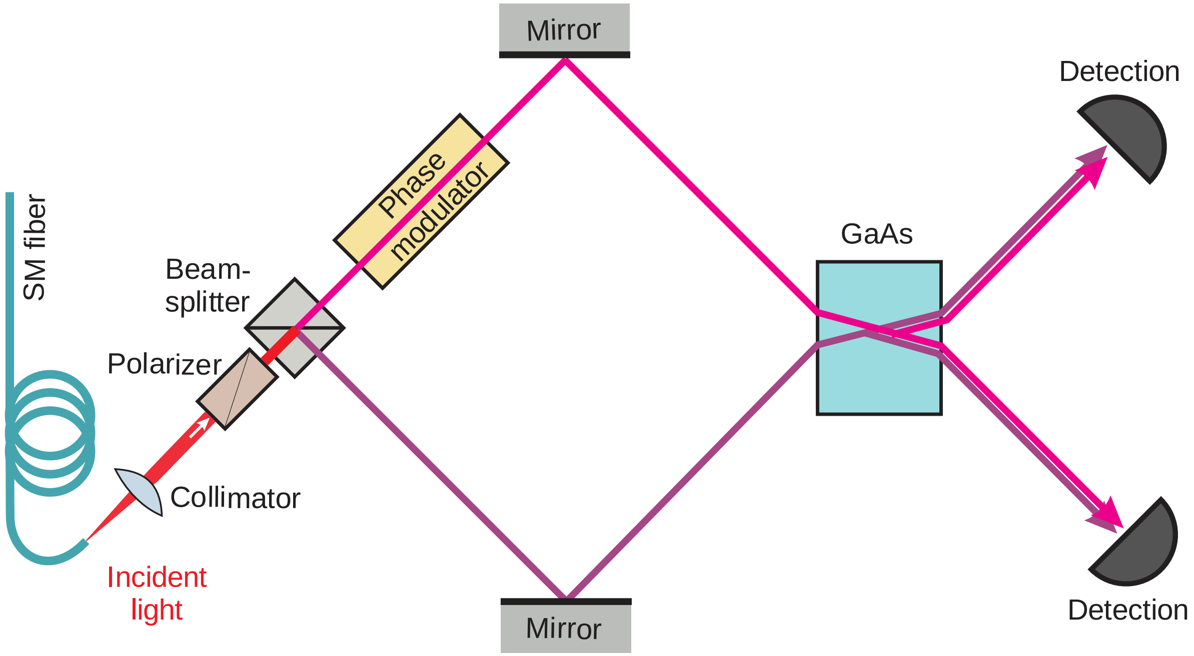


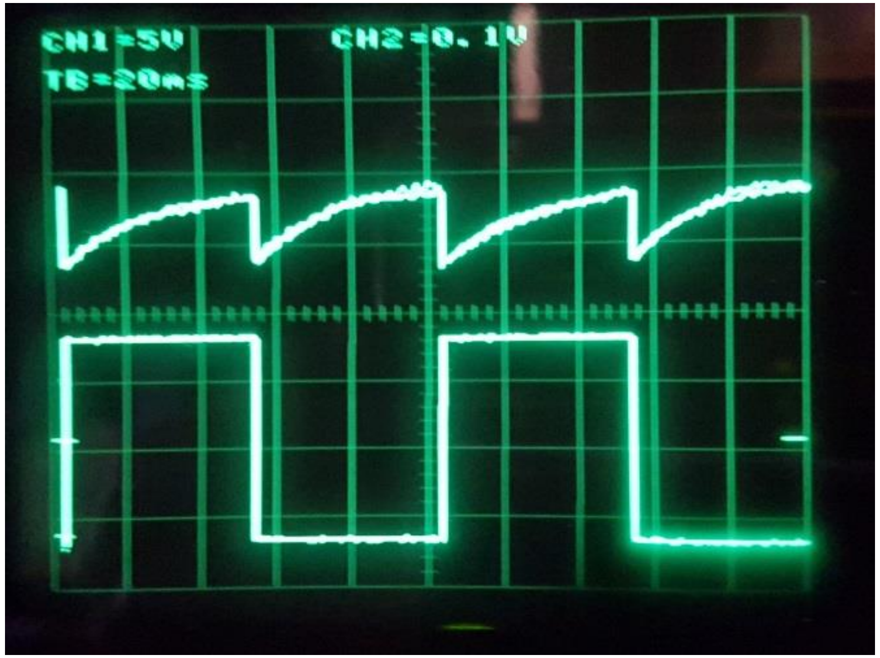


Diffraction from a photorefractive grating

- **Measurement on a thick GaAs layer**

Two-wave mixing in bulk GaAs ≈ single synapse

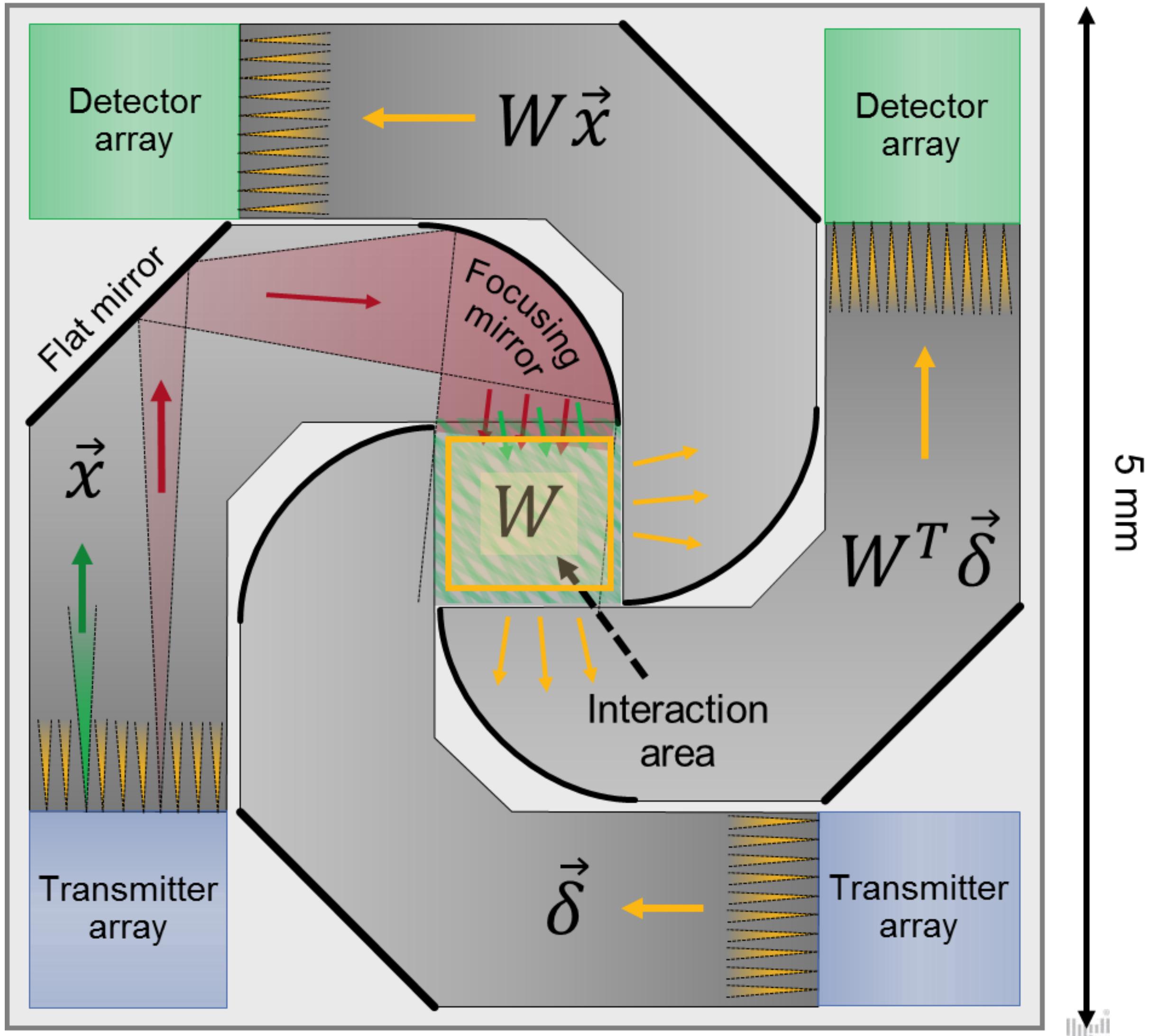




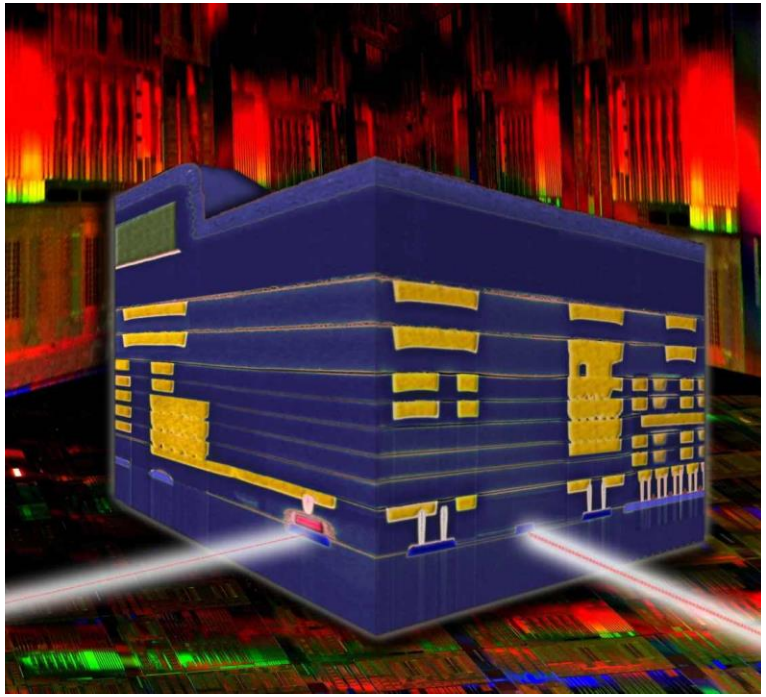
Photonic crossbar unit - subsystem layout

Design study: 200 x 200 processing unit

- Weighting elements
  - Thin planar photorefractive slab on SOI, 1mm x 1mm
  - BTO or GaAs
- 200 Pre-synaptic electrical input signals
  - Optical power control through silicon photonic eo modulators
  - Plane optical waves under different angles in Si slab layer
- 200 Post-synaptic electrical output signals
  - Diffracted plane wave outputs are focused by Si mirror
  - Converted to electrical signals by a Si photonic detector array
- Weight adjustment
  - Photorefractive index modulation through interference pattern originating from the two transmitter arrays
- Scalability
  - A 200 x 200 processing unit fits in 5mm x 5mm
  - Theoretical capacity of interaction area is 2000 x 2000
  - Linear width and height scaling with # channels



CMOS Embedded III-V on silicon technology



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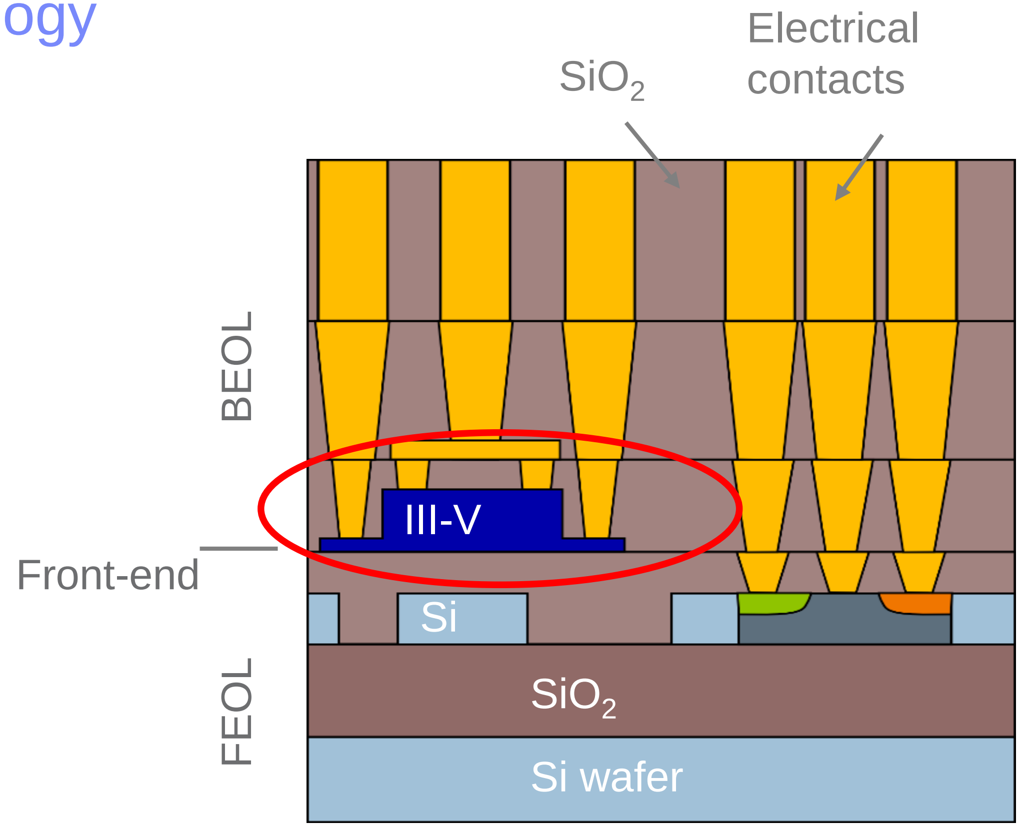


… + III-V functionality

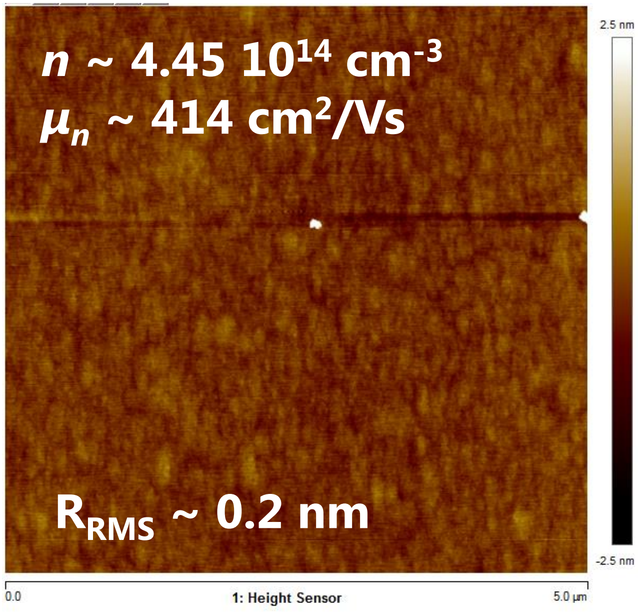
- Overcome discrete laser and assembly cost
- New functions, directly combining electronics, passive and active photonics
- **& photorefractive materials**

MOCVD-based growth of epitaxial GaAs core and InGaP cladding

Development of low-temperature grown GaAs on (110) GaAs wafers

- T_g = 440°C with 600°C pre-bake under As for oxide desorption.
- Atomically flat layers obtained.
  Decreasing growth temperature using high V/III ratio results in a semi-insulating (10^{14} cm^{-3}) material containing electron traps (EL2 ?).

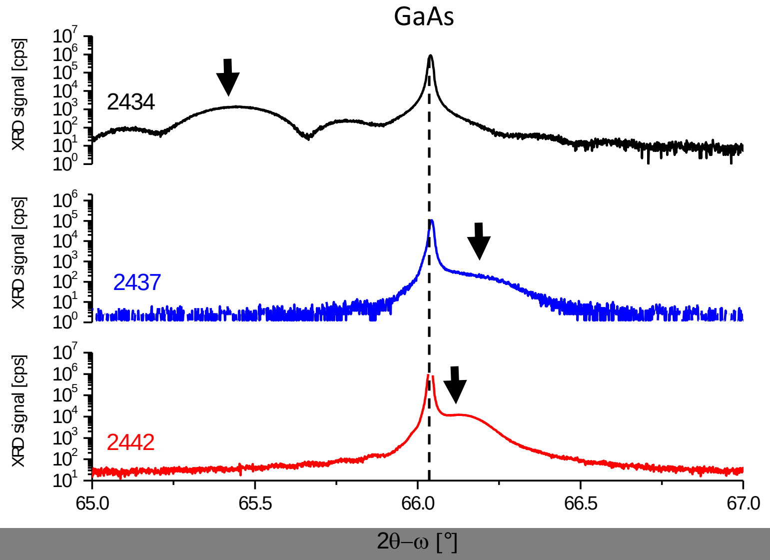
AFM



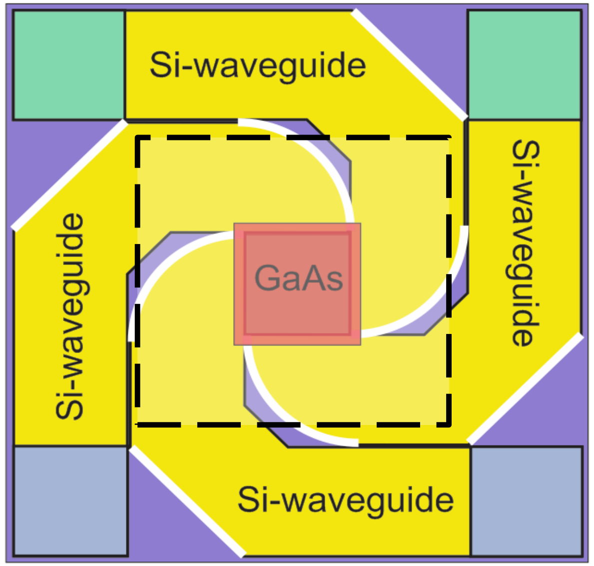
Development of InGaP cladding layer

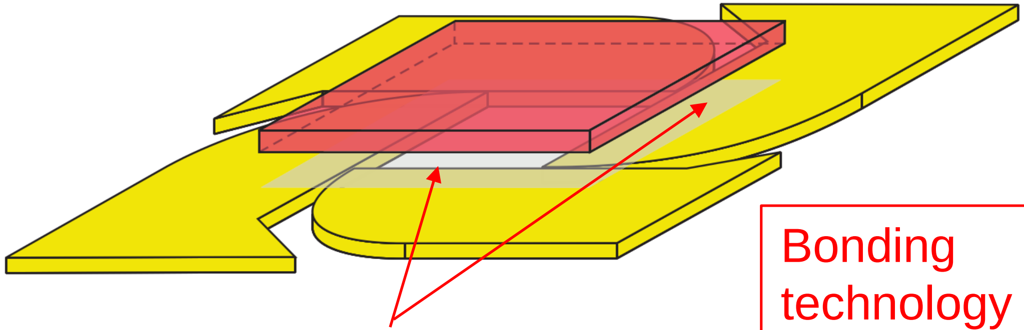
- Tuning the content of $In_xGa_{1-x}P$ allows to grow layers lattice matched to GaAs.
- Further development steps include the growth of a thick InGaP cladding with a low-temperature grown EL2-containing GaAs.

XRD



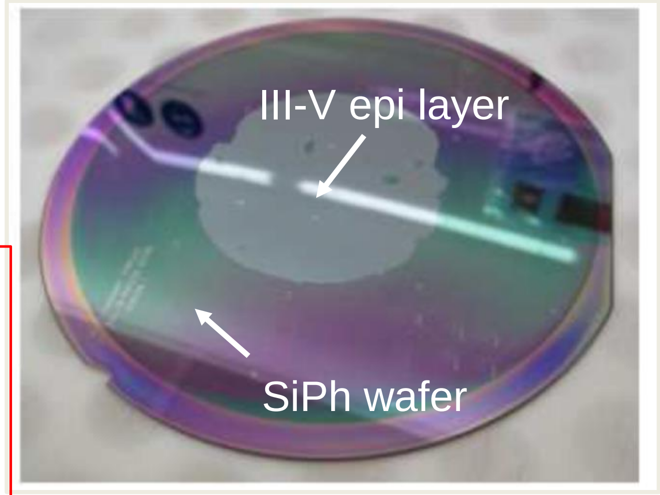
Optical coupling between GaAs and Si



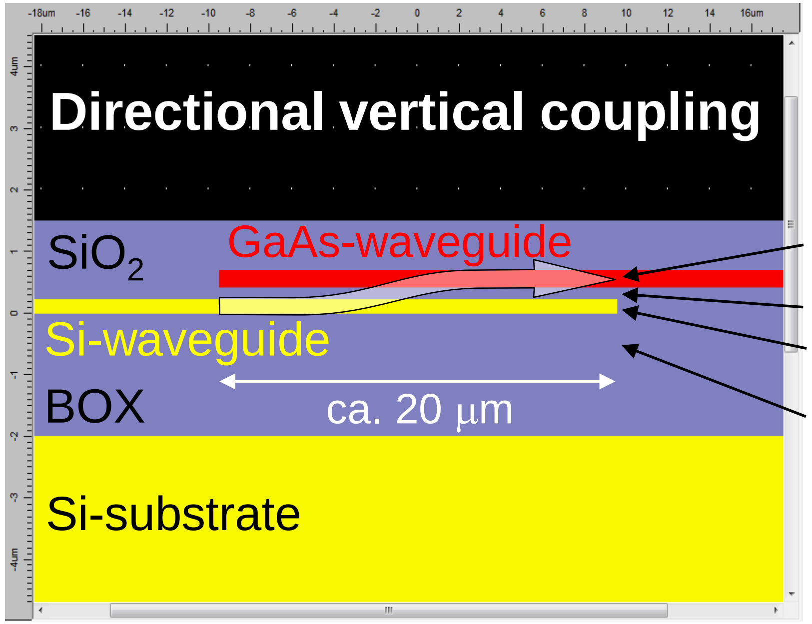


Areas of directional vertical coupling

Bonding technology as for III-V on Si for CMOS and photonics

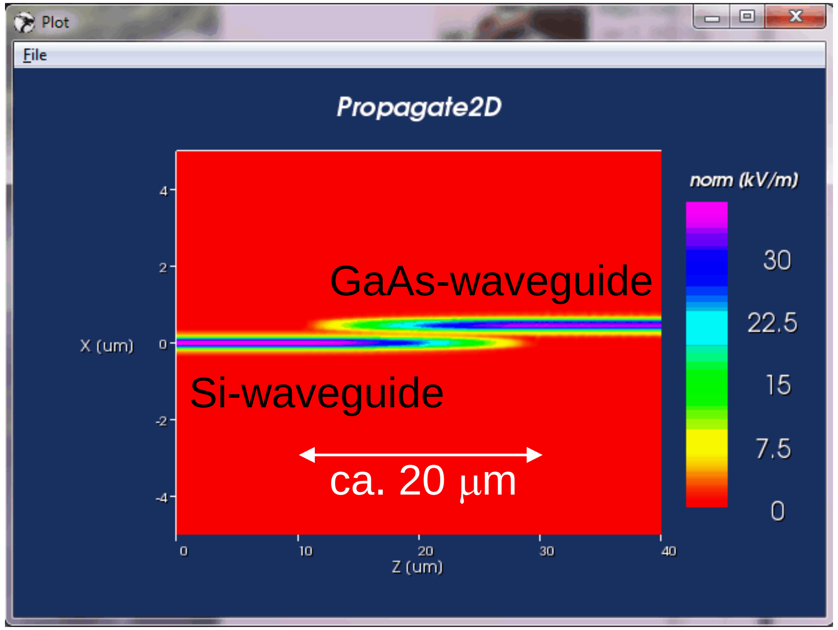


III-V bonded on oxide on Si



Layer thicknesses:

$t_{GaAs\text{-}WG}$ = 260 nm
t_{Gap} = 180 nm
$t_{Si\text{-}WG}$ = 220 nm
t_{BOX} = 2.0 μm



Mode overlap calculation: **99.7%**

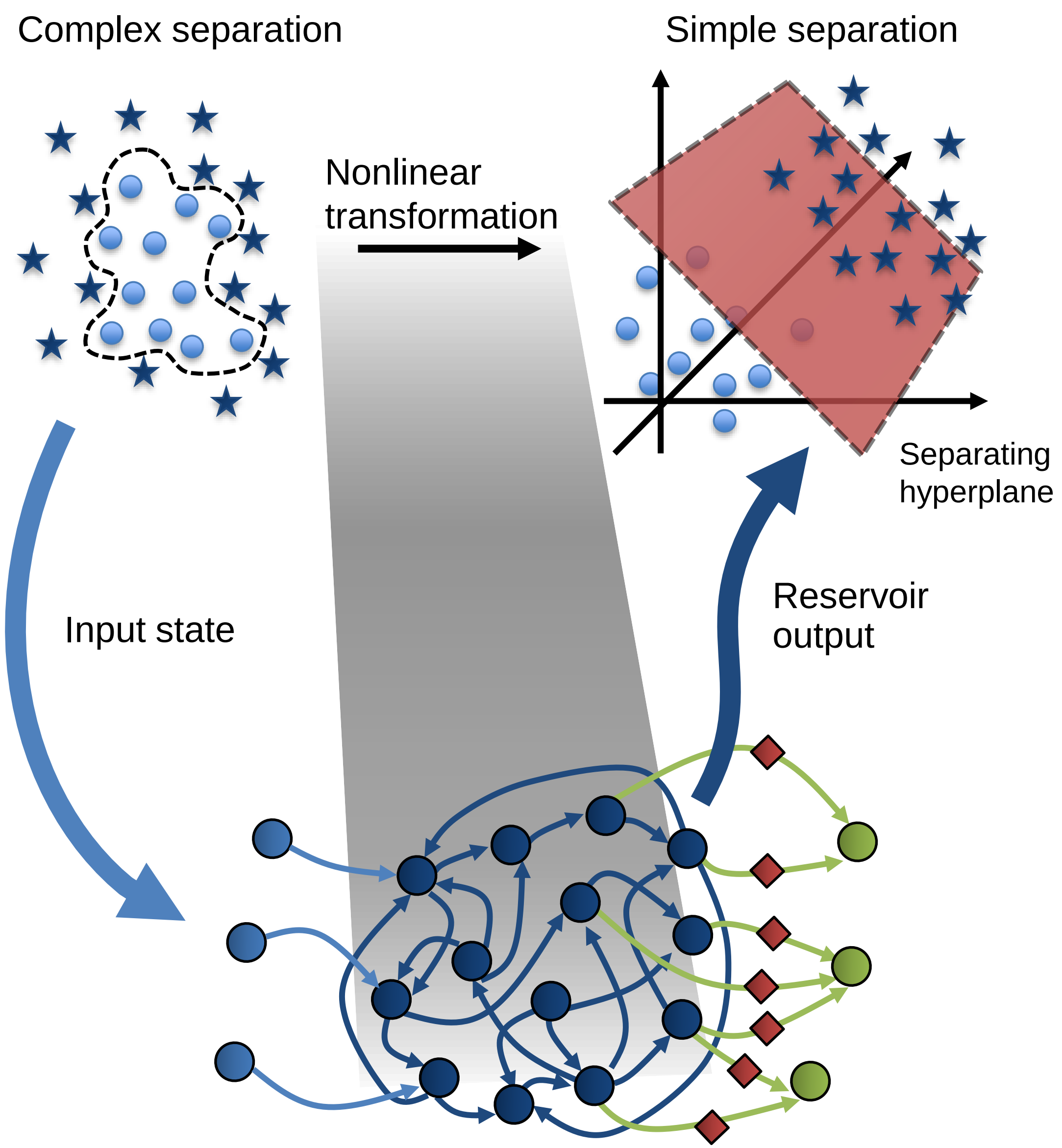
Outline

- **Photonics and computing?**
  - The interconnect bottleneck
  - The Von Neumann Bottleneck
- **Optical interconnects for computing systems**
  - Optical interconnects roadmap
  - CMOS Silicon Photonics
  - Novel functionalities by adding new materials
- **Photonic synaptic elements for Neural Networks**
  - Motivation
  - Photonic Synaptic Processor
  - Non-volatile optical memory elements
- **Conclusions**

Principle of reservoir computing

Structure and properties

- **Layout**
  - – Multiple input channels, single output layer with trainable weights
  - – Reservoir with many interconnected internal nodes
  - – One trainable output layer
- **Working principle**
  - – Reservoir maps dynamic input states into **higher-dimensional state**
  - – Linear classification in higher-dimensional space
    → **reduction of learning/separation complexity**



Appeltant, Nature Commun, 2011
Jaeger, Science, 2004
Maas, Neural computation, 2002

Silicon photonic reservoirs

Generation 1: Passive systems

- **Reservoir system can be mapped onto silicon photonic circuits**

nature COMMUNICATIONS

ARTICLE

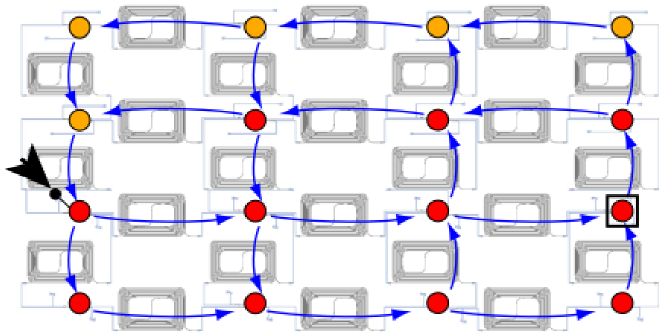
Received 13 Aug 2013 | Accepted 4 Mar 2014 | Published 24 Mar 2014 DOI: 10.1038/ncomms4541 OPEN

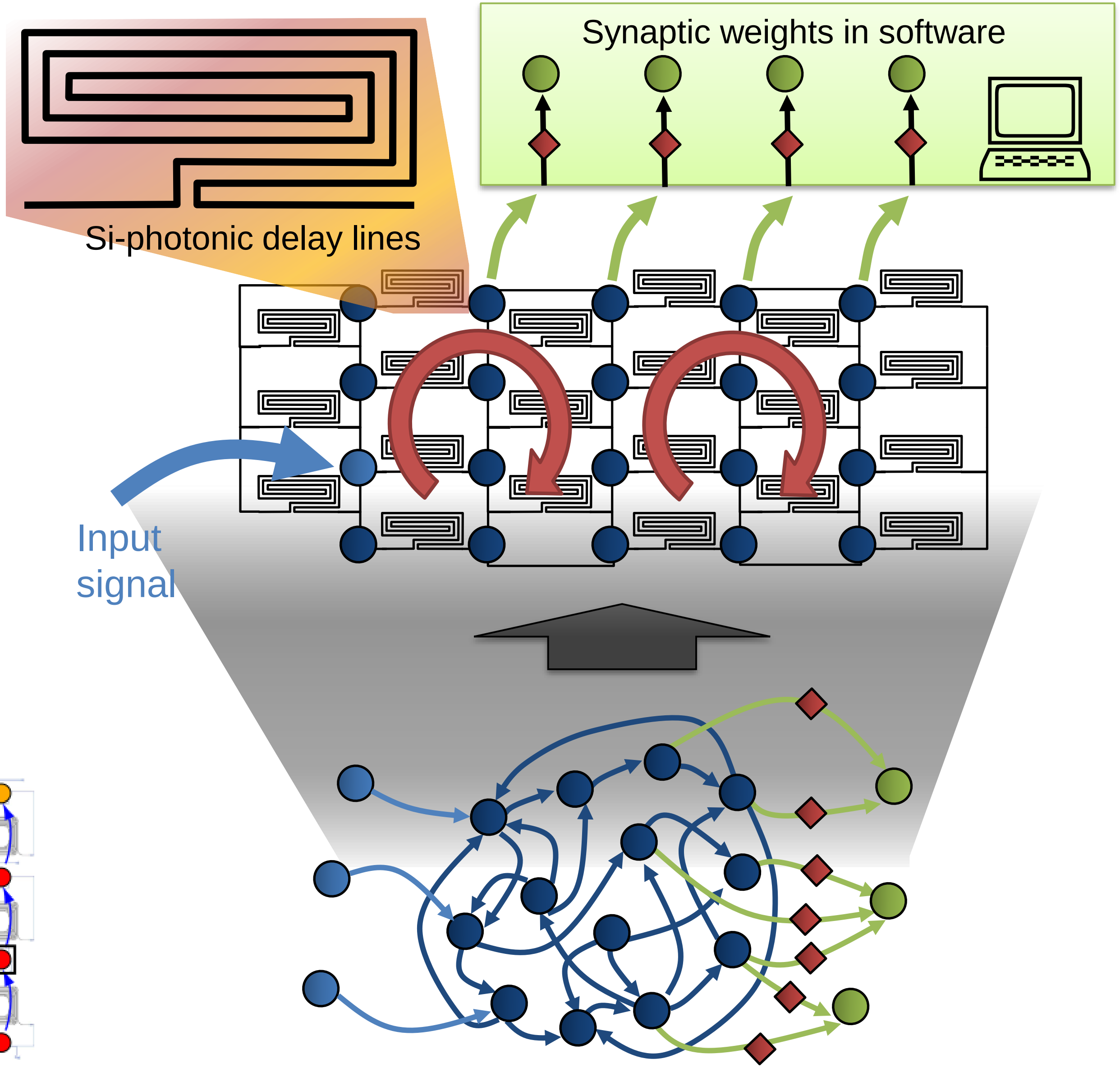
Experimental demonstration of reservoir computing on a silicon photonics chip

Kristof Vandoorne[1,2], Pauline Mechet[1,2], Thomas Van Vaerenbergh[1,2], Martin Fiers[1,2], Geert Morthier[1,2], David Verstraeten[3], Benjamin Schrauwen[3], Joni Dambre[3] & Peter Bienstman[1,2]

Silicon photonics chip

- 2cm delay lines (280ps)
- MMI splitters
- Readout of nodes via grating coupler



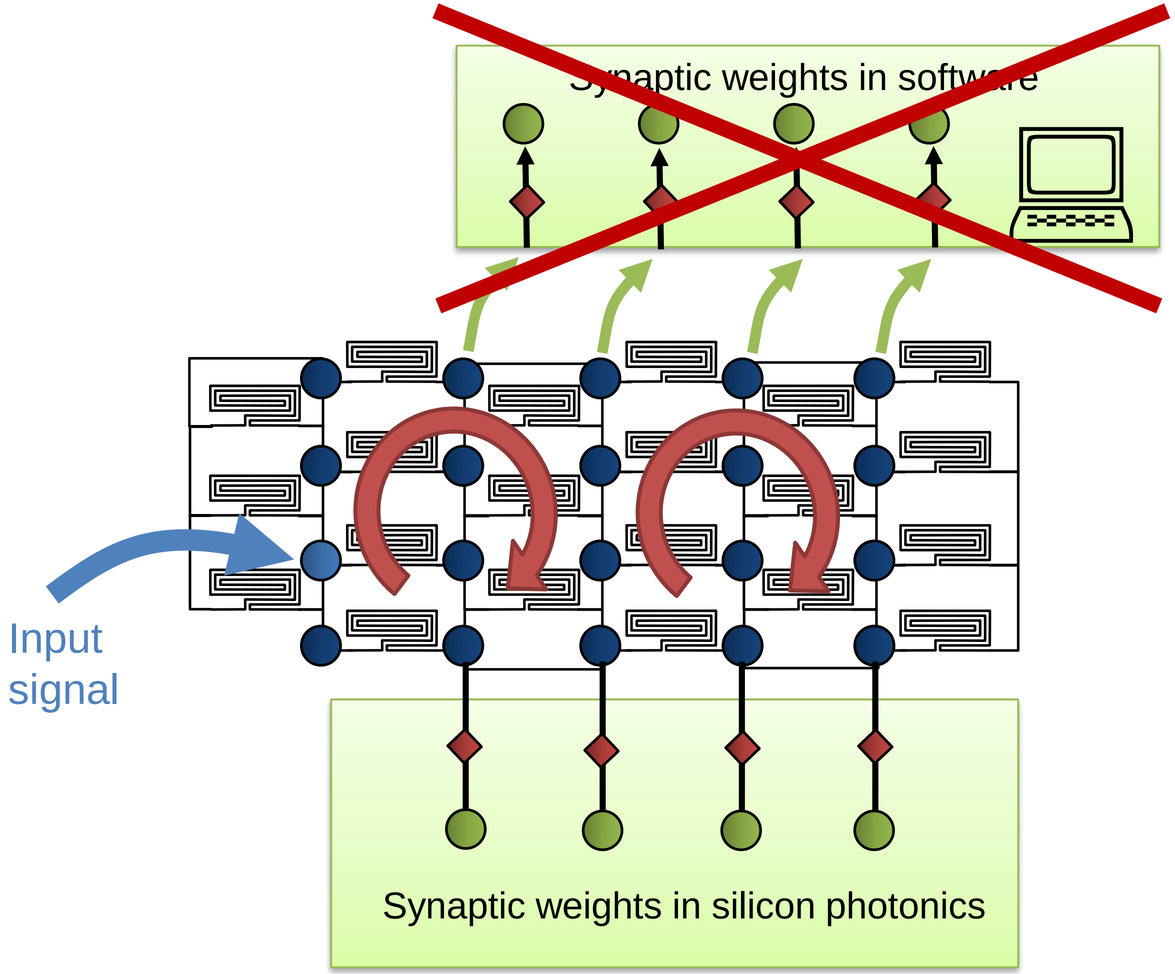


Vandoorne, Nature Commun., 2014

Silicon photonic reservoirs

Generation 1: Passive systems

- **Reservoir system can be mapped onto silicon photonic circuits**

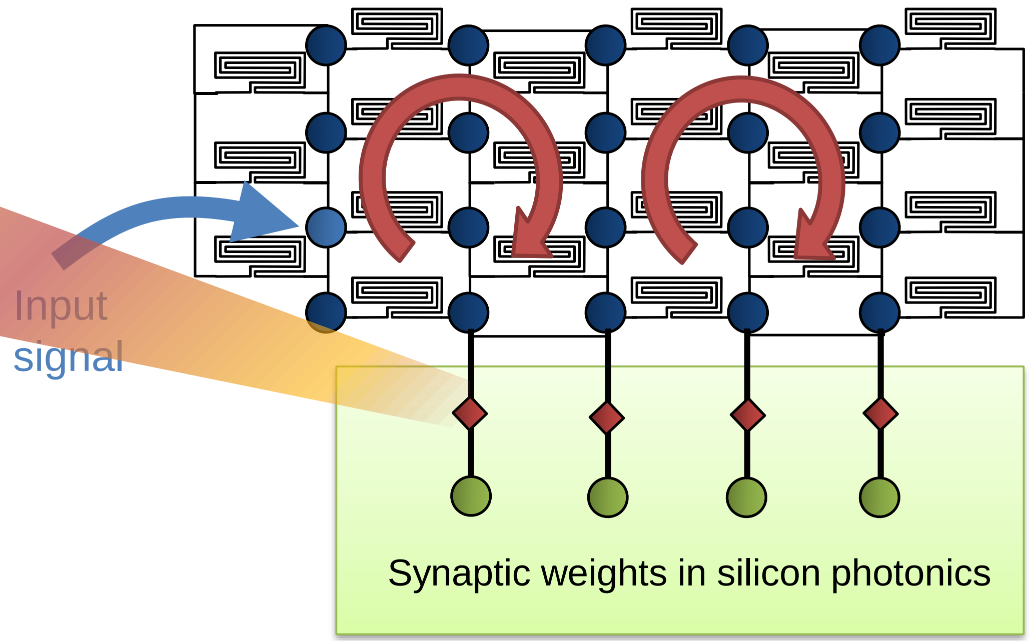


Silicon photonic reservoirs

Generation 2: Active systems

- **Reservoir system can be mapped onto silicon photonic circuits**
- **Need for novel optical devices**
  - Non-volatile optical synapses
  - Other functional oxides (e.g. VO_2)

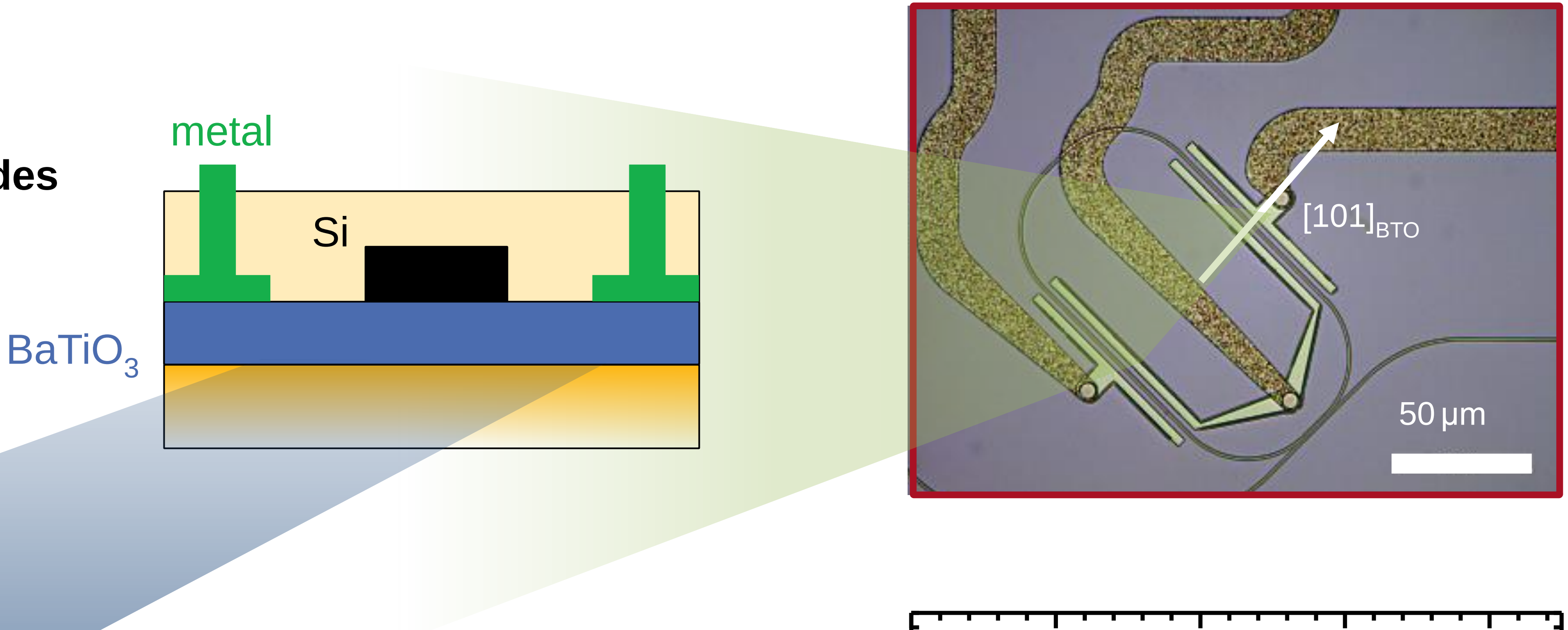
Horizon 2020
European Union funding
for Research & Innovation

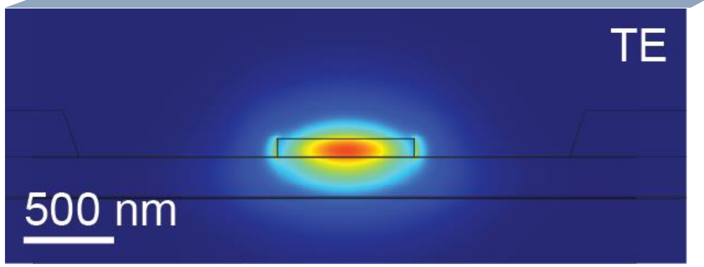


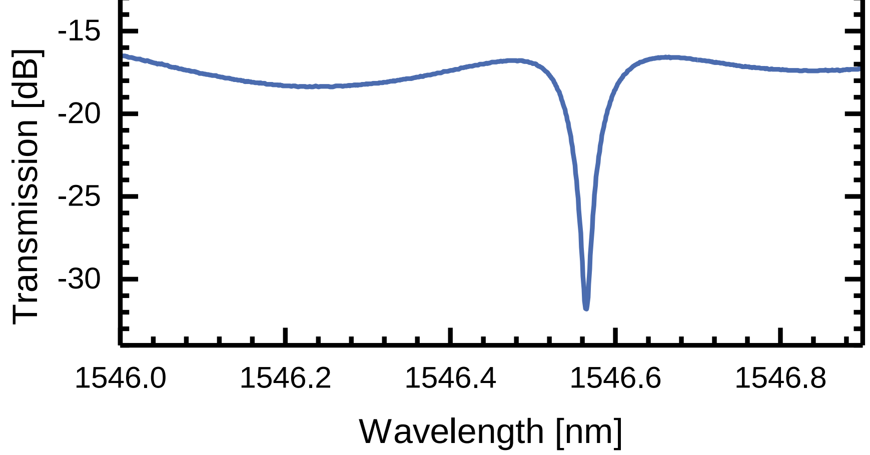
Non-volatile optical weights

Device layout

- **Hybrid $BaTiO_3$/Si waveguides**





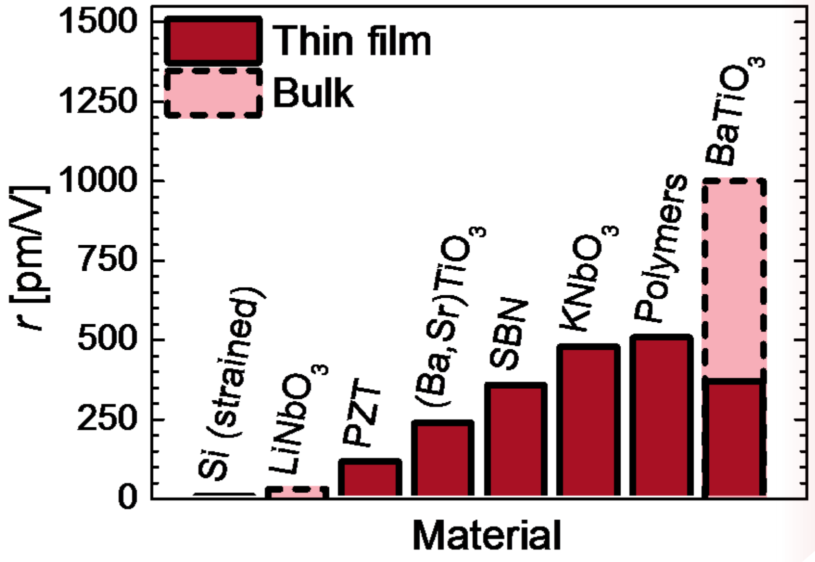


Non-volatile optical weights

Device concept

- **Hybrid $BaTiO_3$/Si waveguides**
- **Why $BaTiO_3$?**

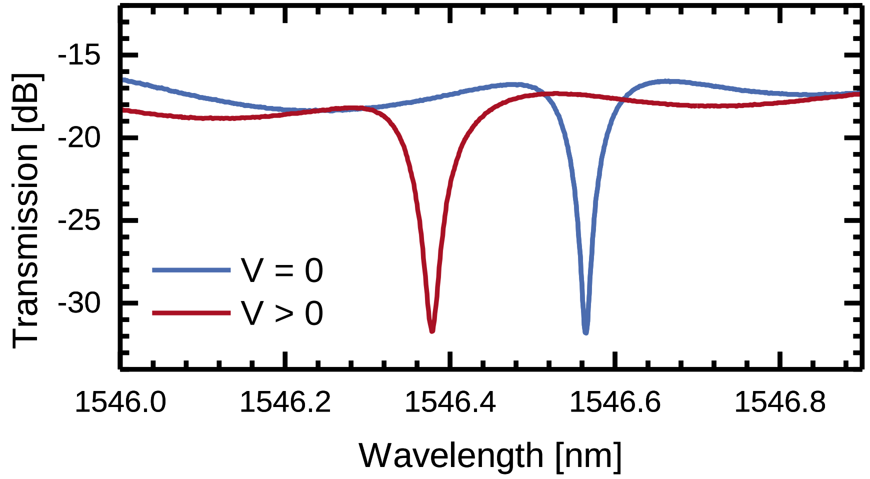
Literature values for Pockels coefficients



Electro-optic switching

$$n(E) = n - \frac{1}{2} r n^3 E$$

Pockels effect

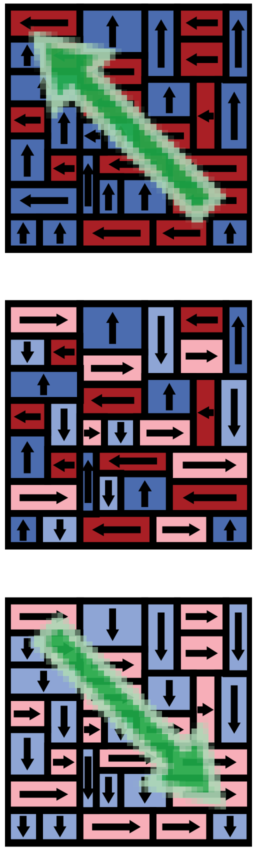


Non-volatile optical weights

Device concept

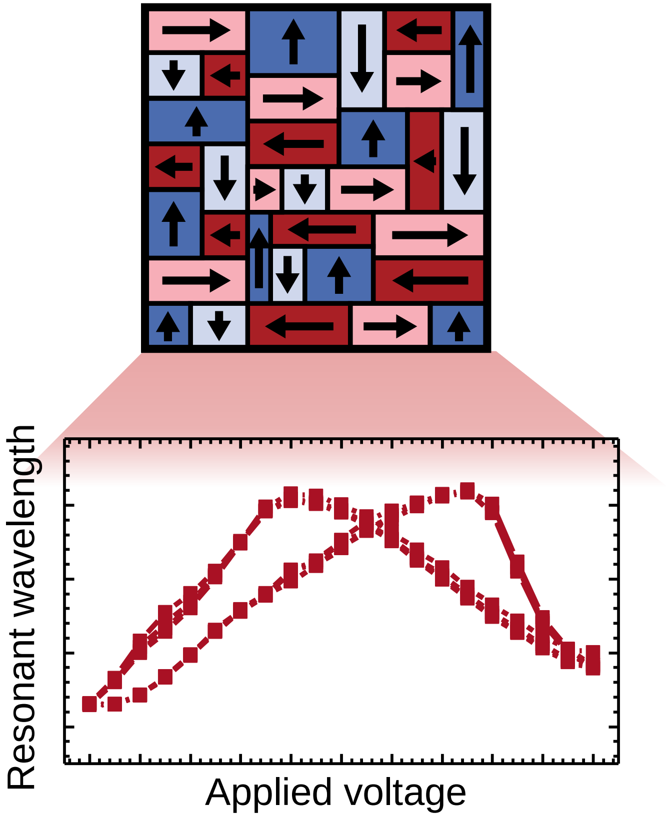
- **Hybrid $BaTiO_3$/Si waveguides**
- **Why $BaTiO_3$?**

Domain switching by applying electric field



Ferroelectricity

Non-volatile storage in domain patterns

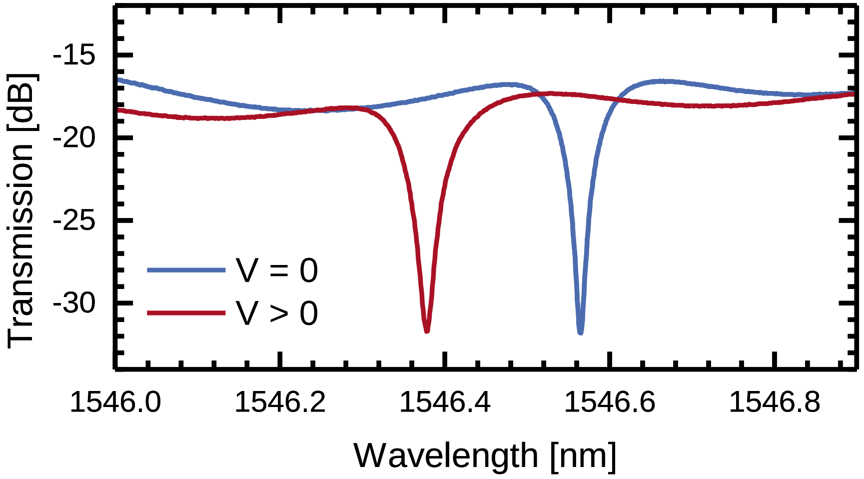


Electro-optic switching

$$n(E) = n - \frac{1}{2} r n^3 E - \frac{1}{2} \xi n^3 E^2$$

Pockels effect

Kerr effect



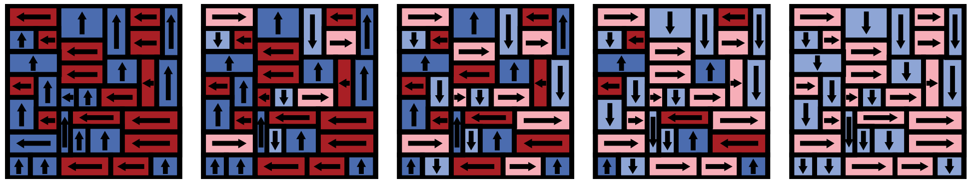
Non-volatile optical weights

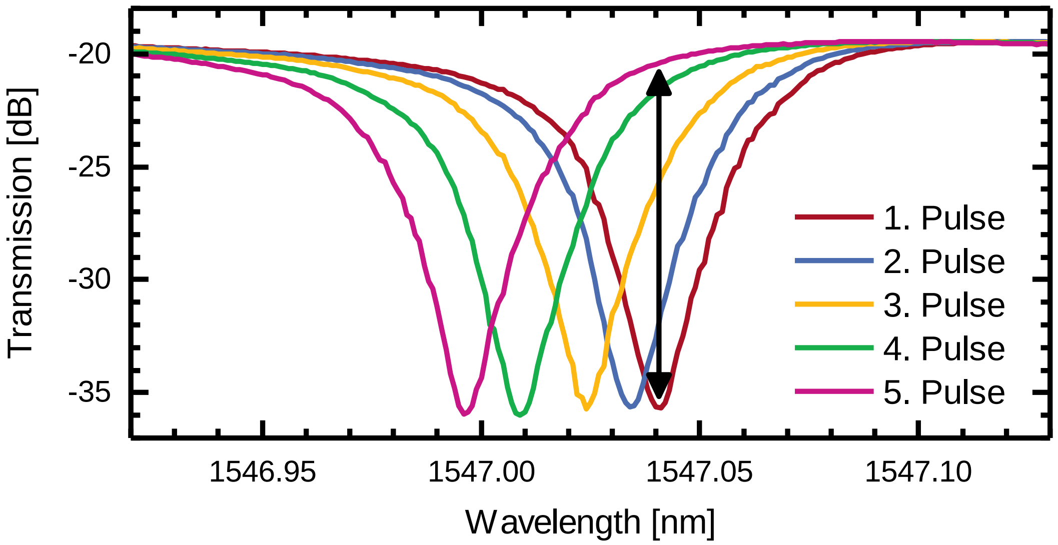
Results

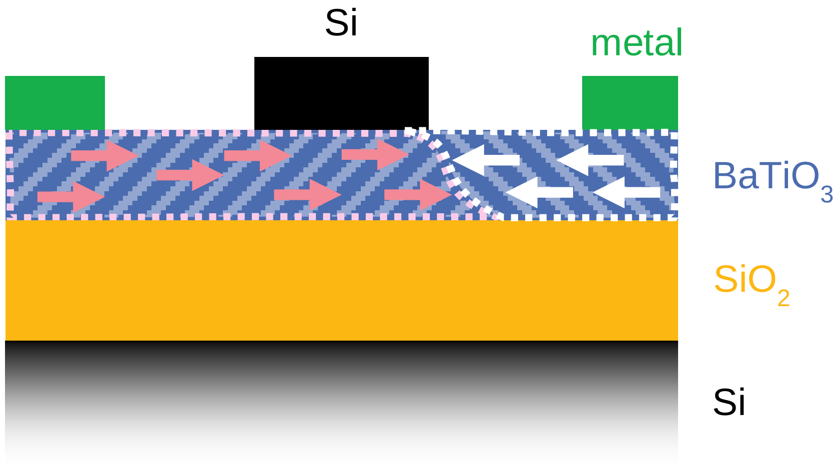
- **Hybrid $BaTiO_3$/Si waveguides**
- **Why $BaTiO_3$?**

Stabilization of ferroelectric domains

- **Non-volatile optical multi-level weights**







Non-volatile optical weights

Results

- **Hybrid $BaTiO_3$/Si waveguides**
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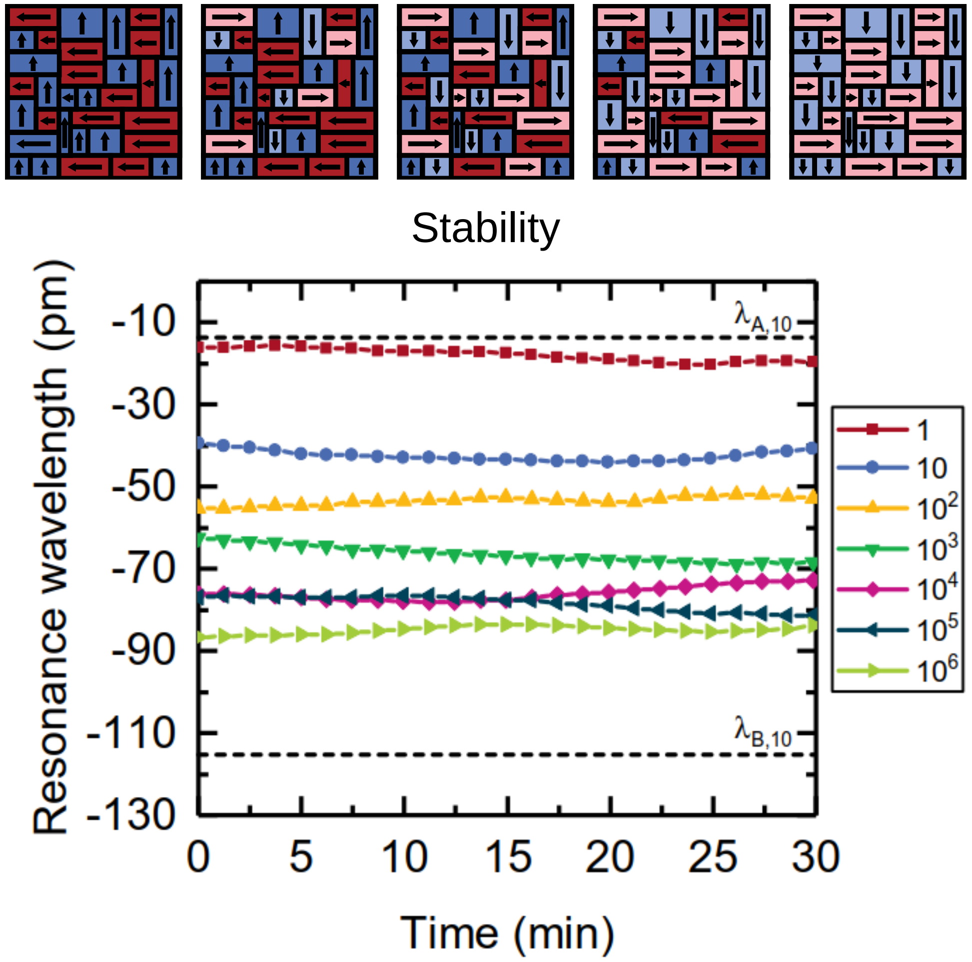
Stabilization of ferroelectric domains

- **Non-volatile optical multi-level weights**
- **Stable for >30 minutes**



Non-volatile optical weights

Results

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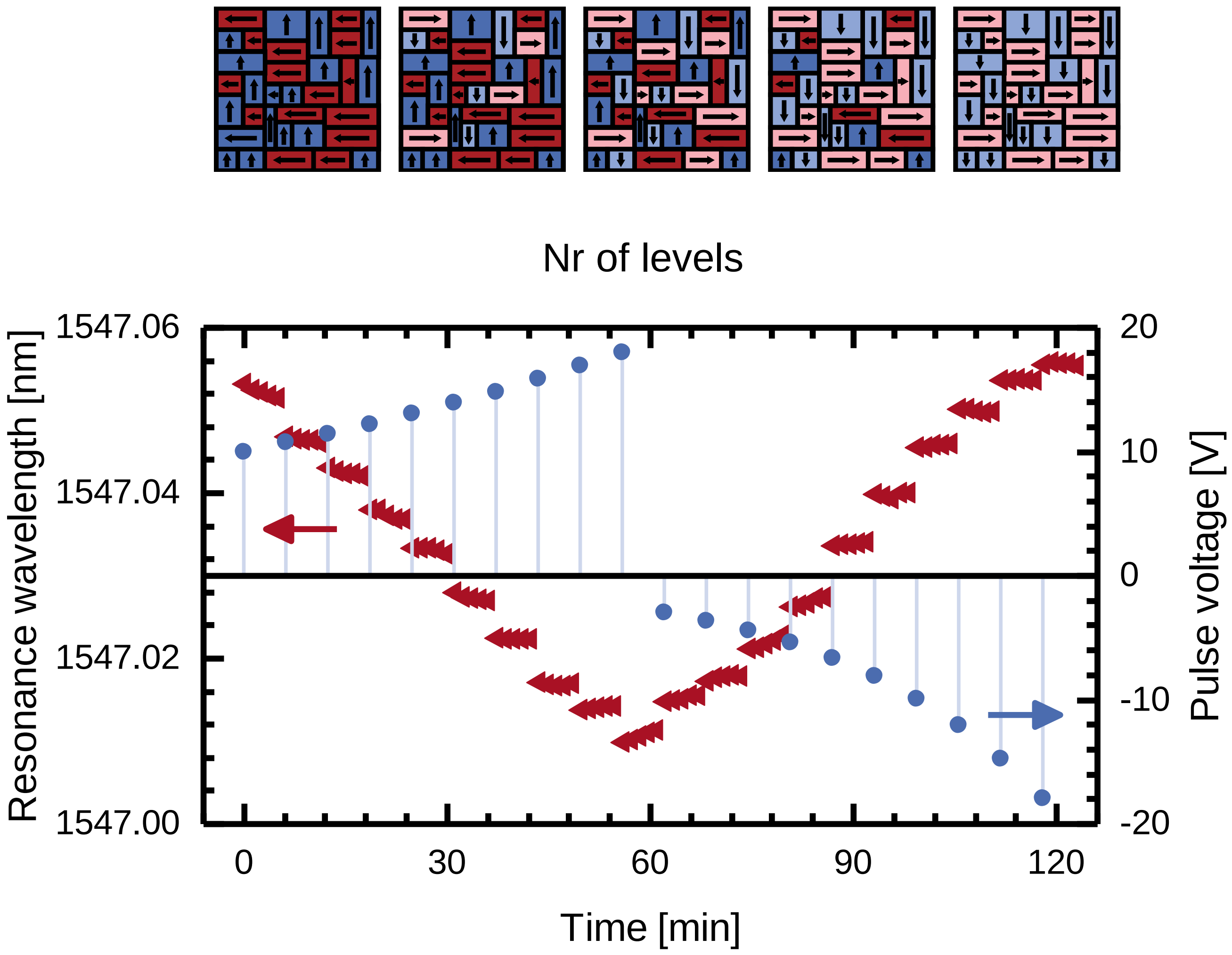
Stabilization of ferroelectric domains

- **Non-volatile optical multi-level weights**
- **Stable for >30 minutes**
- **Multiple (>10) levels achieved**



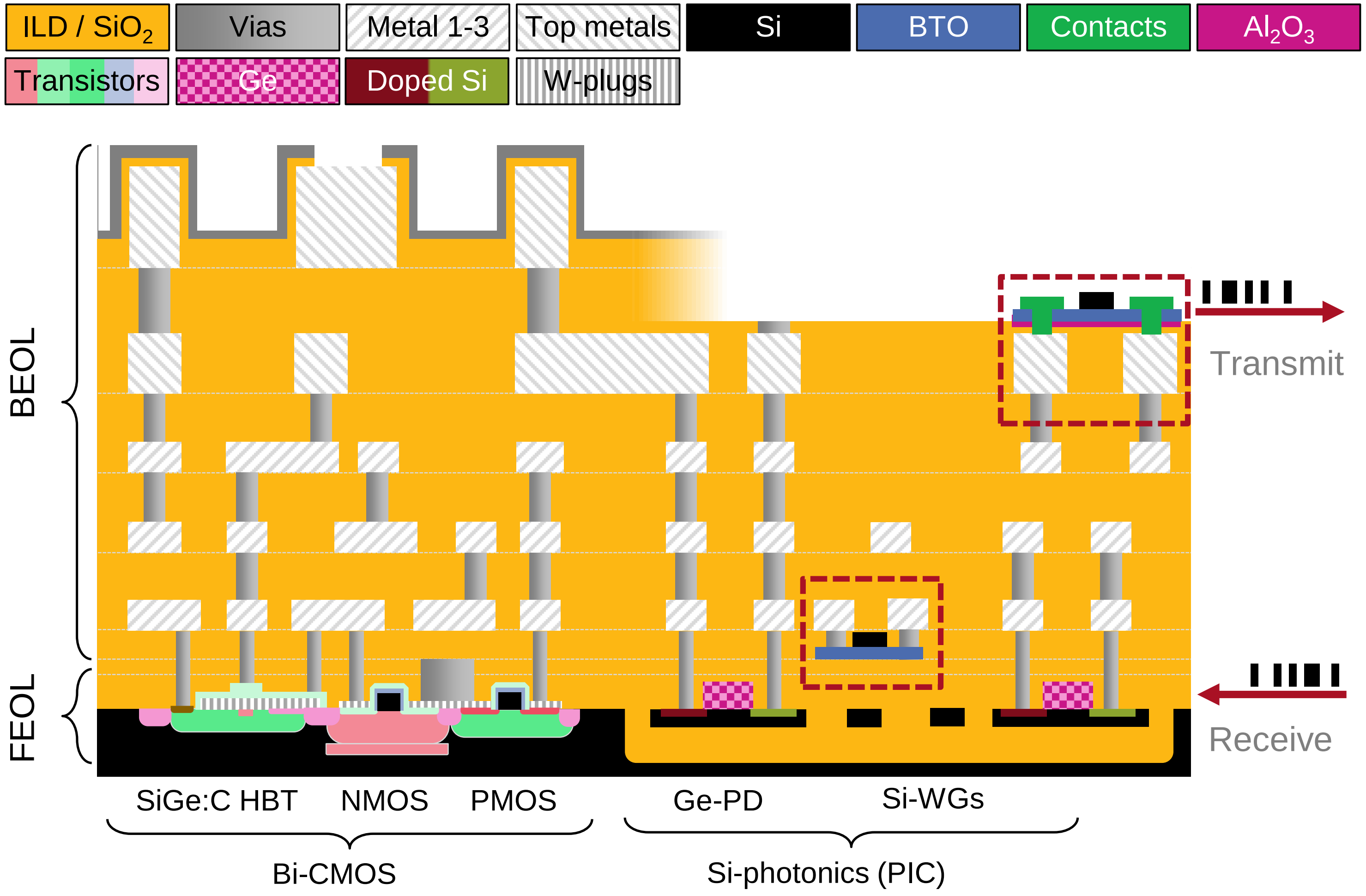
Non-volatile optical weights

Results

- **Hybrid $BaTiO_3$/Si waveguides**
- **Why $BaTiO_3$?**

Stabilization of ferroelectric domains

- **Non-volatile optical multi-level weights**
- **Stable for >30 minutes**
- **Multiple (>10) levels achieved**
- **Compatibility with CMOS process flow & 200mm wafer size**

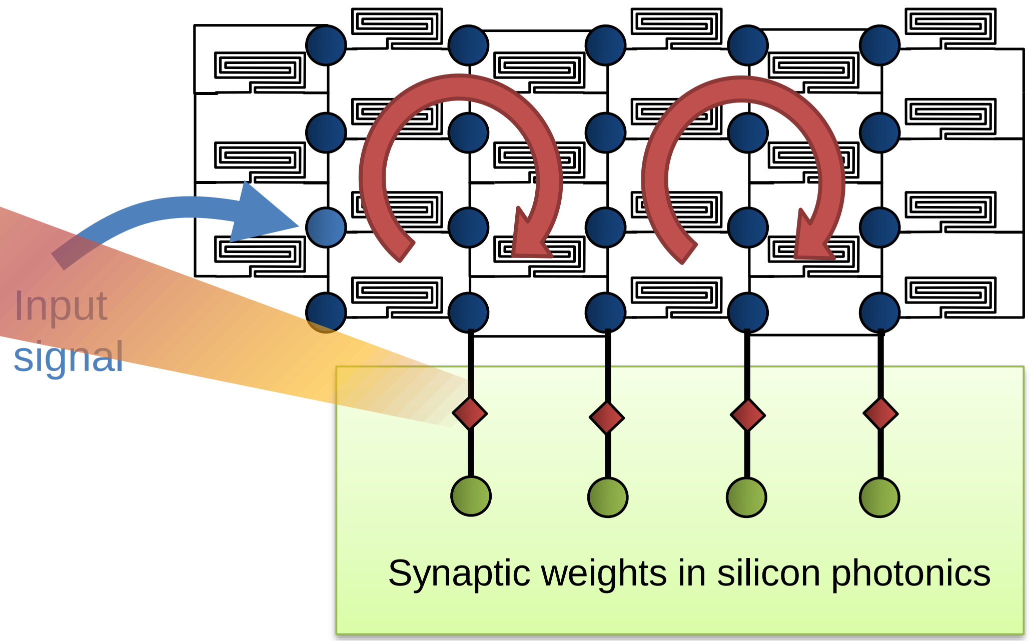


Accepted at IEDM 2017

Silicon photonic reservoirs

Generation 2: Active systems

- **Reservoir system can be mapped onto silicon photonic circuits**
- **Need for novel optical devices**
  - Non-volatile optical synapses
  - Other functional oxides (e.g. VO_2)



Silicon photonic reservoirs

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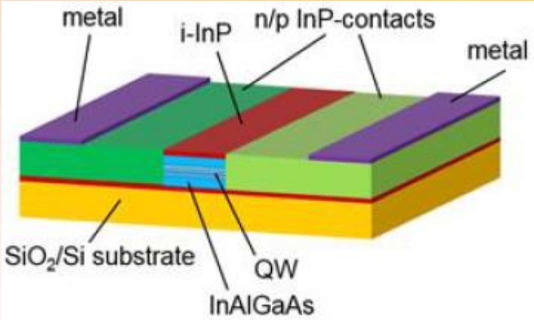
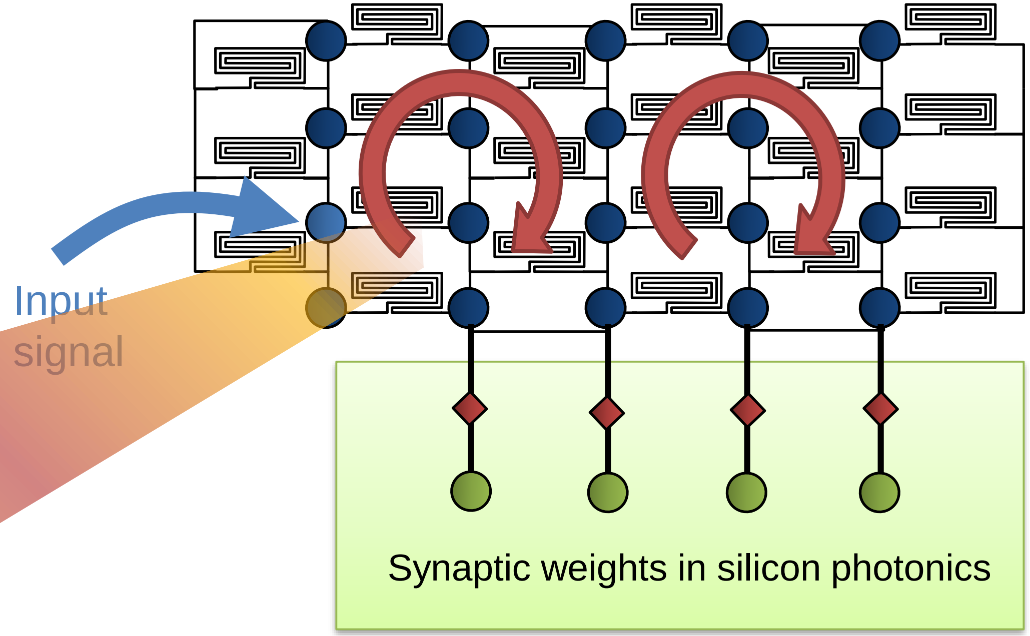
- **Other materials to be integrated to increase system performance**
  - Nonlinear materials
  - Optical amplification
  - …

III/V devices on silicon





Silicon photonic reservoirs

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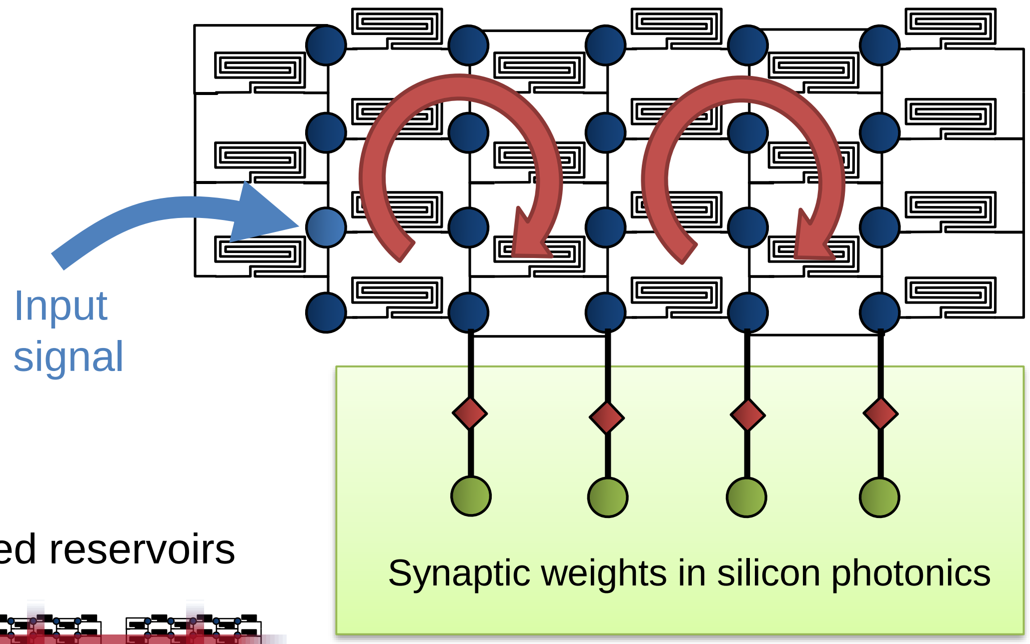
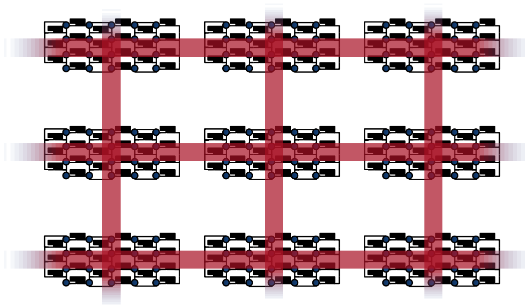
  - Optical amplification
  - …

Generation 2 of silicon photonic reservoir systems

- **Larger networks**
- **Weighting in hardware**
- **Cascading of networks**
- **Richer dynamics**



Cascaded reservoirs



Conclusions

- **Photonics technology helps to overcome interconnect bottlenecks**
  – Communication at scale
  – Von Neumann bottleneck

- **Applications for computing**
  – Optical interconnects
  – Training of synaptic weights in neural networks
  – Reservoir computing systems

- **Extend silicon technology**
  – III-V but also other types such as ferroelectric
  – Photorefractive, optical gain, switching, optical weights

- **+ large variety of other opportunities and applications**

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IBM Research – Zurich, Switzerland
Stefan Abel, Folkert Horst, Marc Seifried, Gustavo Villares, Roger Dangel, Felix Eltes, Jacqueline Kremer, Jean Fompeyrine, D. Caimi, L. Czornomaz, M. Sousa, H. Siegwart, C. Caer, Y. Baumgartner, D. Jubin, N. Meier, A. La Porta, J. Weiss, V. Despandhe, U. Drechsler

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