An Approximate Parallel Multiplier with Deterministic Errors for Ultra-High Speed Integrated Optical Circuits

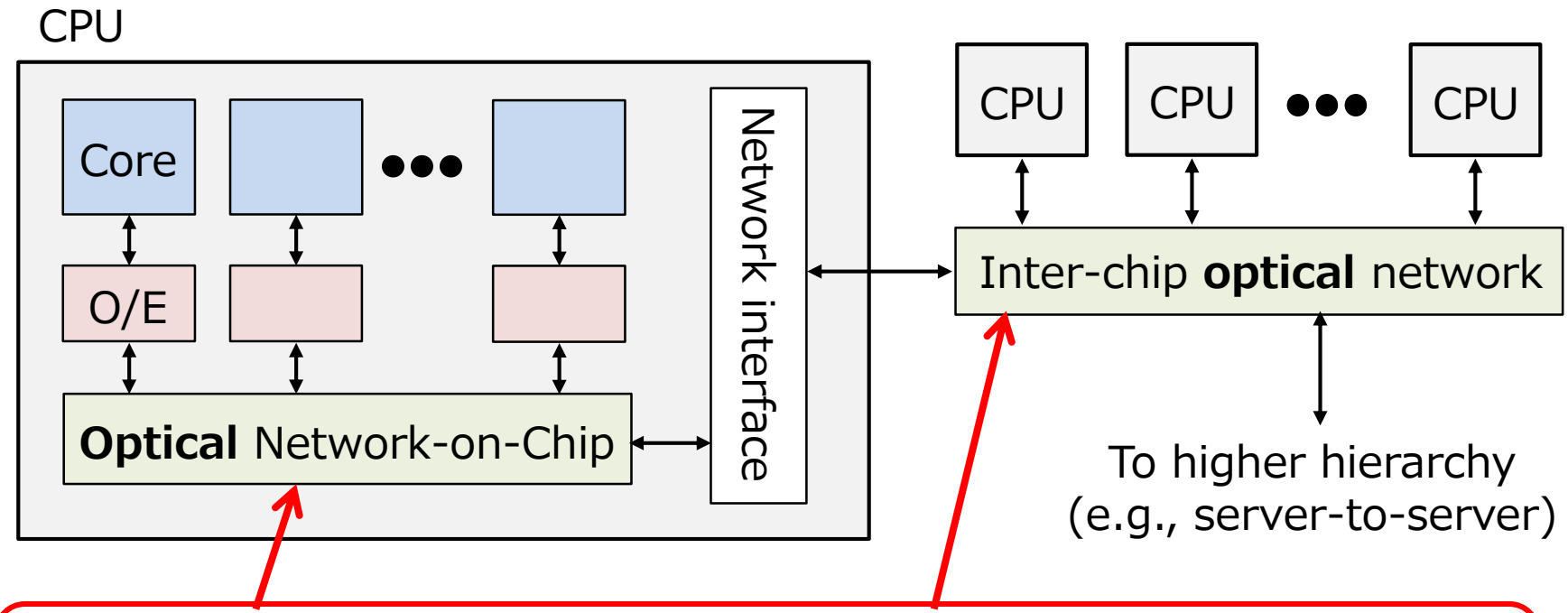
Jun Shiomi[1], Tohru Ishihara[1], Hidetoshi Onodera[1],
Akihiko Shinya[2], Masaya Notomi[2]

[1]Graduate School of Informatics, Kyoto University, Japan
[2]NTT Nanophotonics Center / NTT Basic Research Laboratories, Japan

Beyond Optical Communication

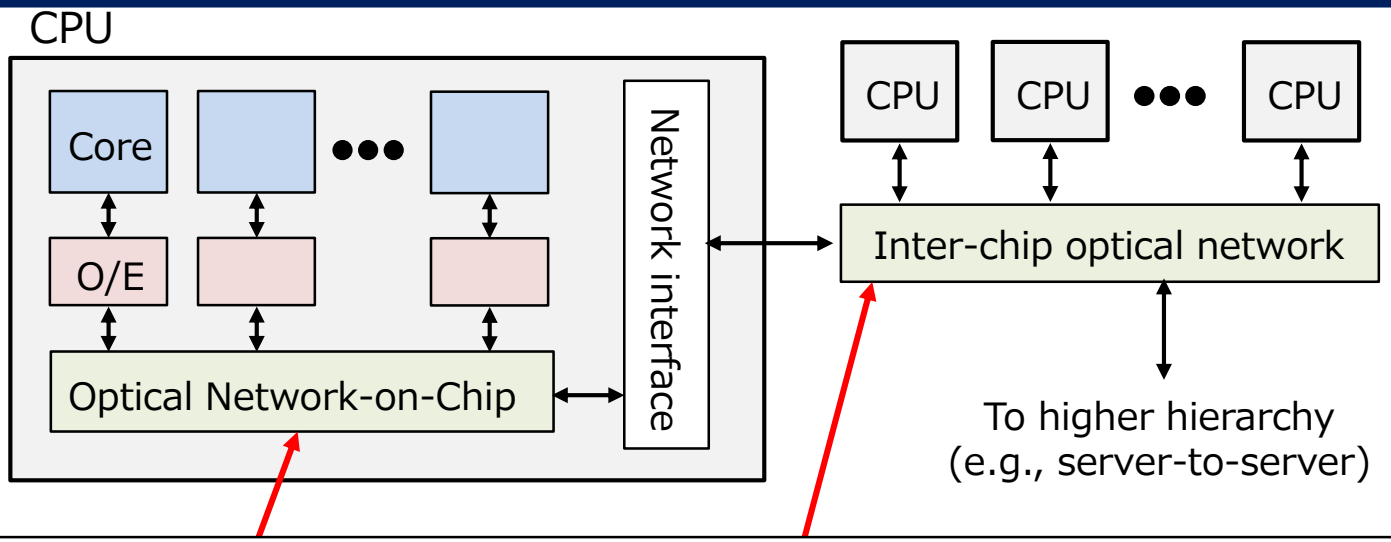
Background: Advancement in nanophotonic devices

⇨ Enables on-chip interconnects for broadband commutation



Goal: Add **functional unit** to boost up on-chip communication
E.g. pattern recognition

Approximate Parallel Multiplier with Nanophotonic Devices



- ✓ Optical implementation of **approximate parallel multiplier**
  - For Machine Learning (ML), Approximate Computing (AC)
  - 11% deterministic error at the worst case
- ✓ Enables signal processing with **ultra-low latency**
  - Example (32-bit parallel multiplier)

W/o approximation: > 800 ps (< 1.25 GHz)

This work: 123 ps (8.1 GHz)

6.5 × boost

Outline

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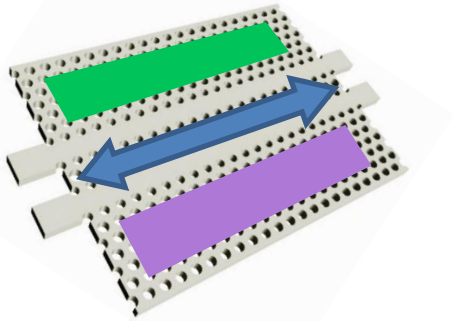
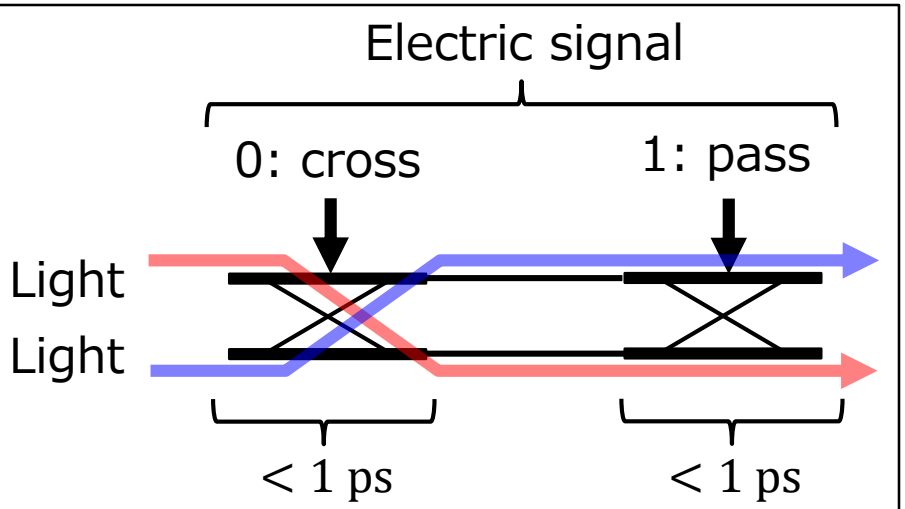
Photonic Crystal-Based Optical Pass-Gate (OPG) [2]

Directional coupler

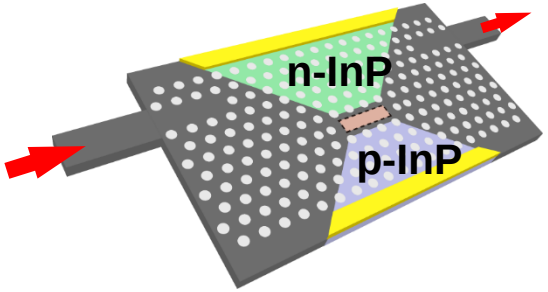
Length $> 100\mu m$

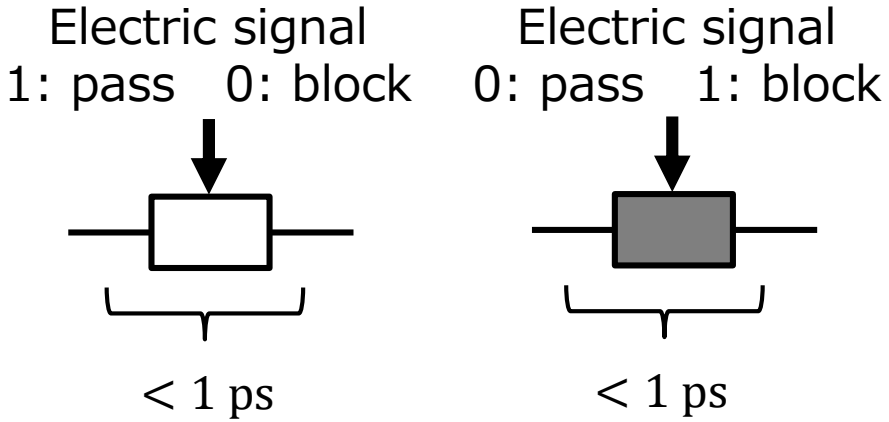




Modulator

Length ~ 1.3 μm

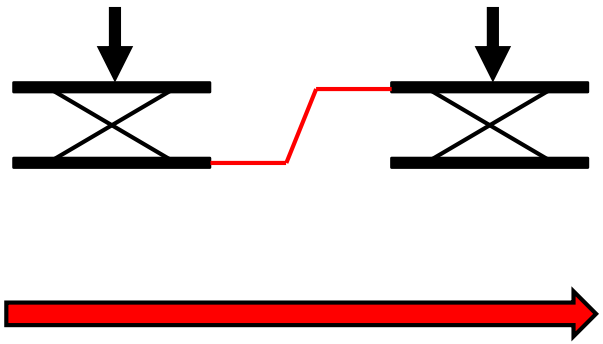




[2] T. Ishihara, et al., International SoC Design Conference, 2016

OptoElectoric Conversion Delay

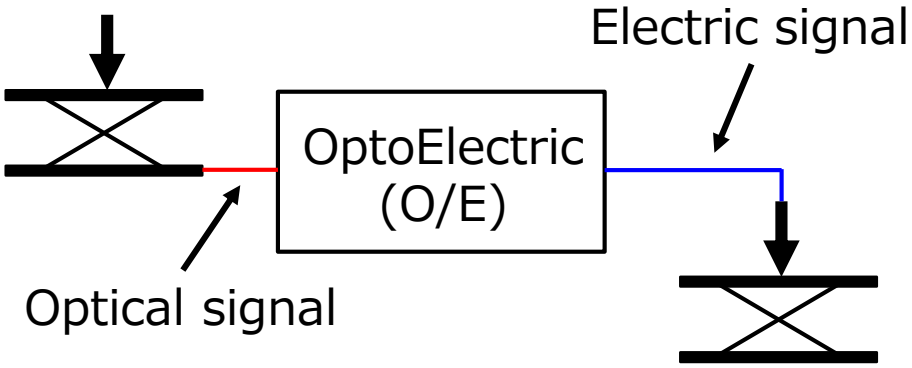
Serial connection



Light speed ($\sim$ **1 ps** /gate)

τ_{OPG}

Cascade connection



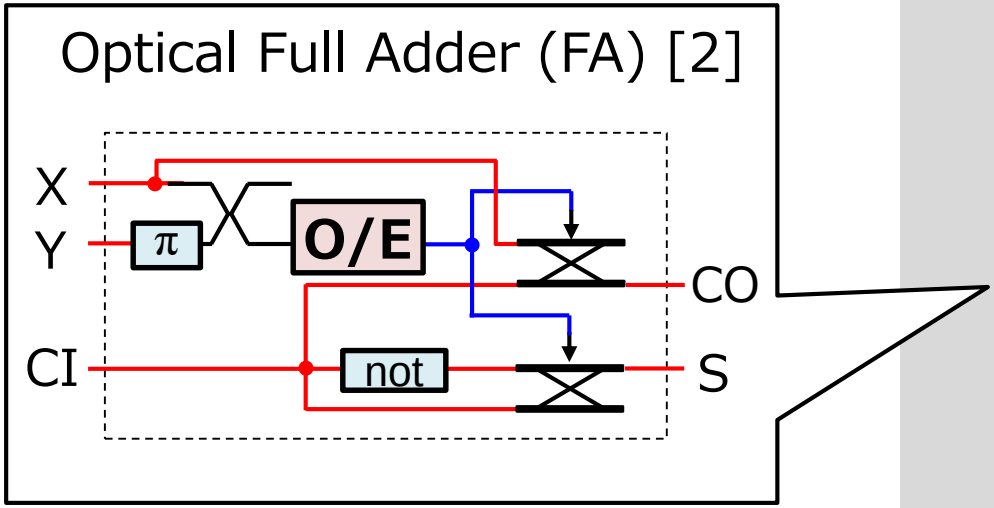
O/E conversion ($\sim$ **25 ps**)

τ_{OE}

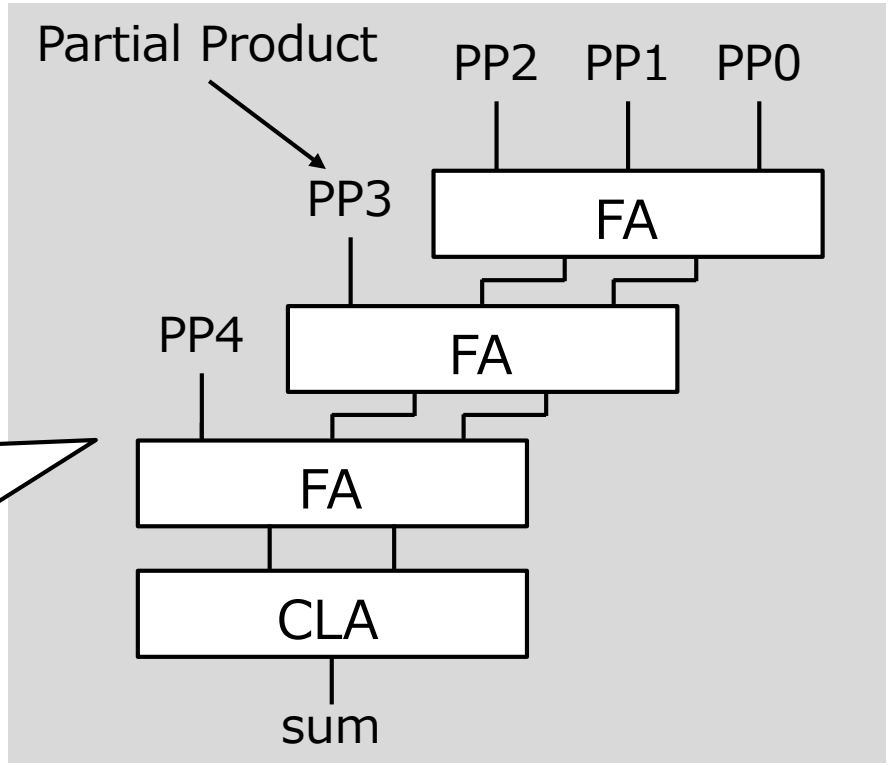
✓ **Reducing O/Es on a critical path** is a key to ultra-fast operation

Issues in Conventional Optical Parallel Multiplier

5-bit array multiplier



[2] T. Ishihara, et al., International SoC Design Conference, 2016



Issue: #(O/Es) = **(Bit width n)** ☹ Large latency for large n

$1\tau_{\mathrm{OE}} = 25$ ps (40 GHz) ⟶ $32\tau_{\mathrm{OE}} = 800$ ps (1.25 GHz) ⟶ $64\tau_{\mathrm{OE}} = 1600$ ps (625 MHz)

Too slow!

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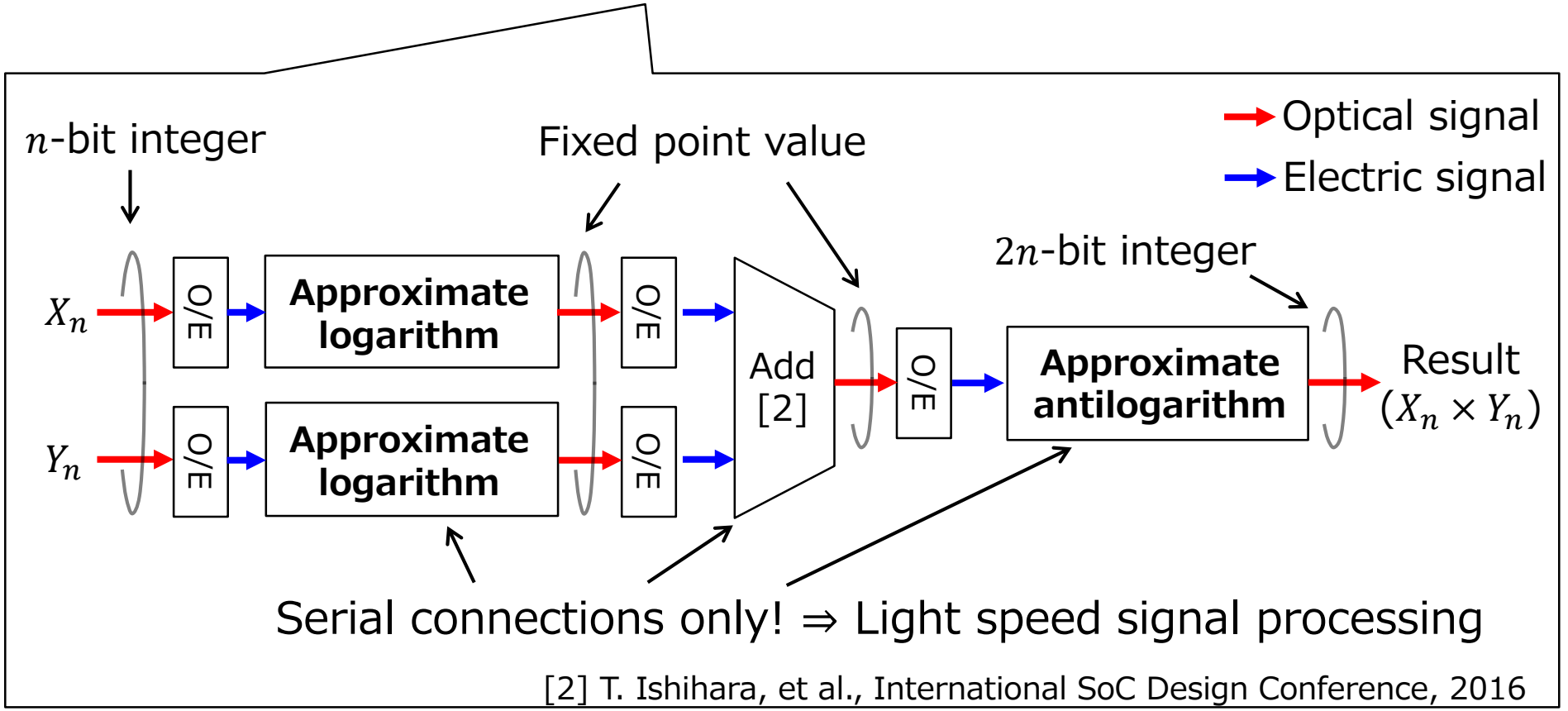
Basic Idea of the Proposed Approximate Multiplier

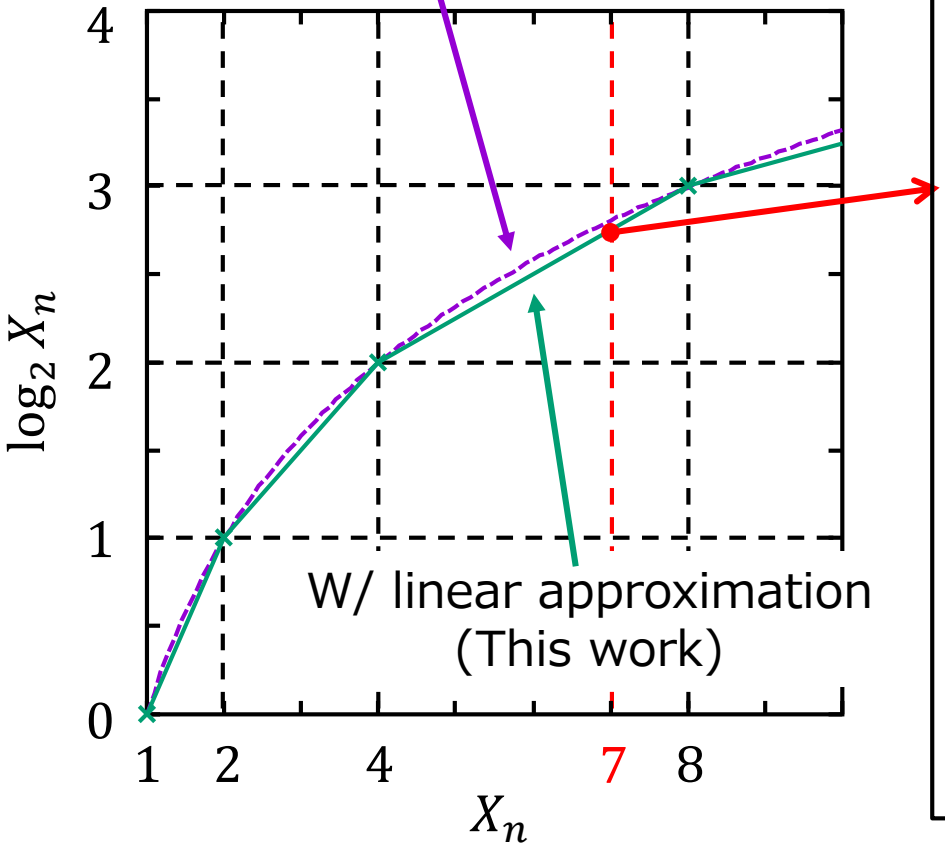
$$X_n \times Y_n = 2^{\log_2 X_n + \log_2 Y_n} \quad (X_n, Y_n \in \mathbb{Z}_+)$$



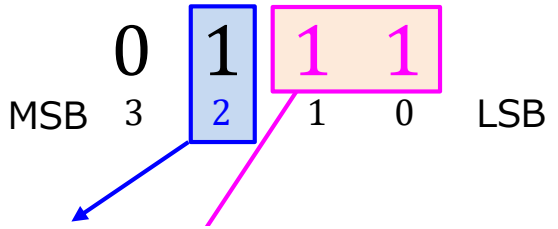
✓ **Three O/E converters** on a critical path **for any bit width n**

Concept of Approximate Logarithm [3]

$$2^{\log_2 X_n + \log_2 Y_n}$$



E.g. $\log_2 7$ approximation



1. Find max. digit that has 1
   ⇒ 10_2 (= **Priority encoder**)
2. Simply return the remainder
   ⇒ 11_2 (= **Shifter**)

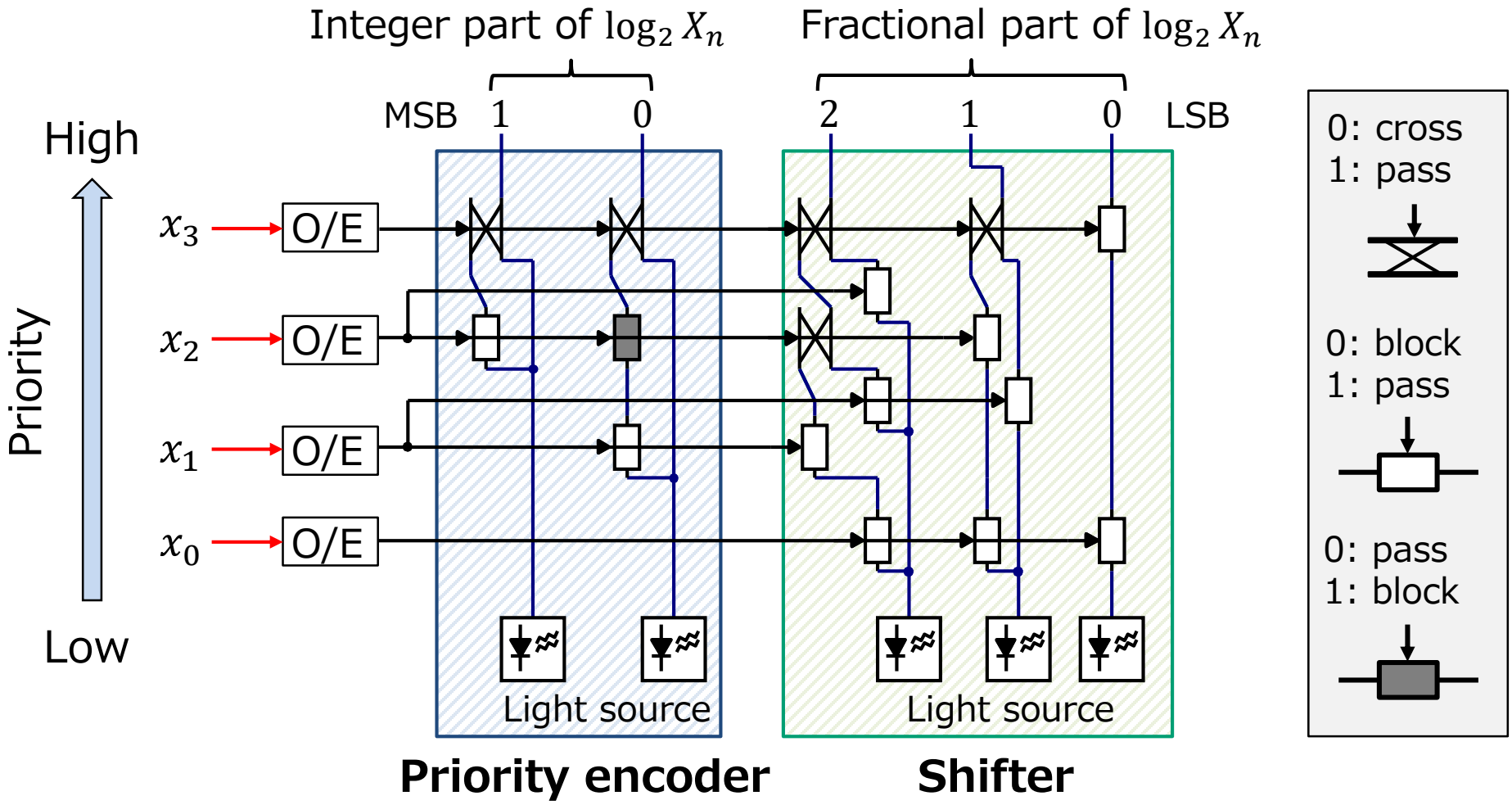
Approximate $\log_2 7$ result:
10.110_2 (Fixed point)

✓ Approximate antilogarithm: Inverse function of the logarithm

[3] J. N. Mitchell, IRE Transactions on Electronic Computers, 1962

Priority Encoder-Based Approximate Logarithm ($n = 4$)

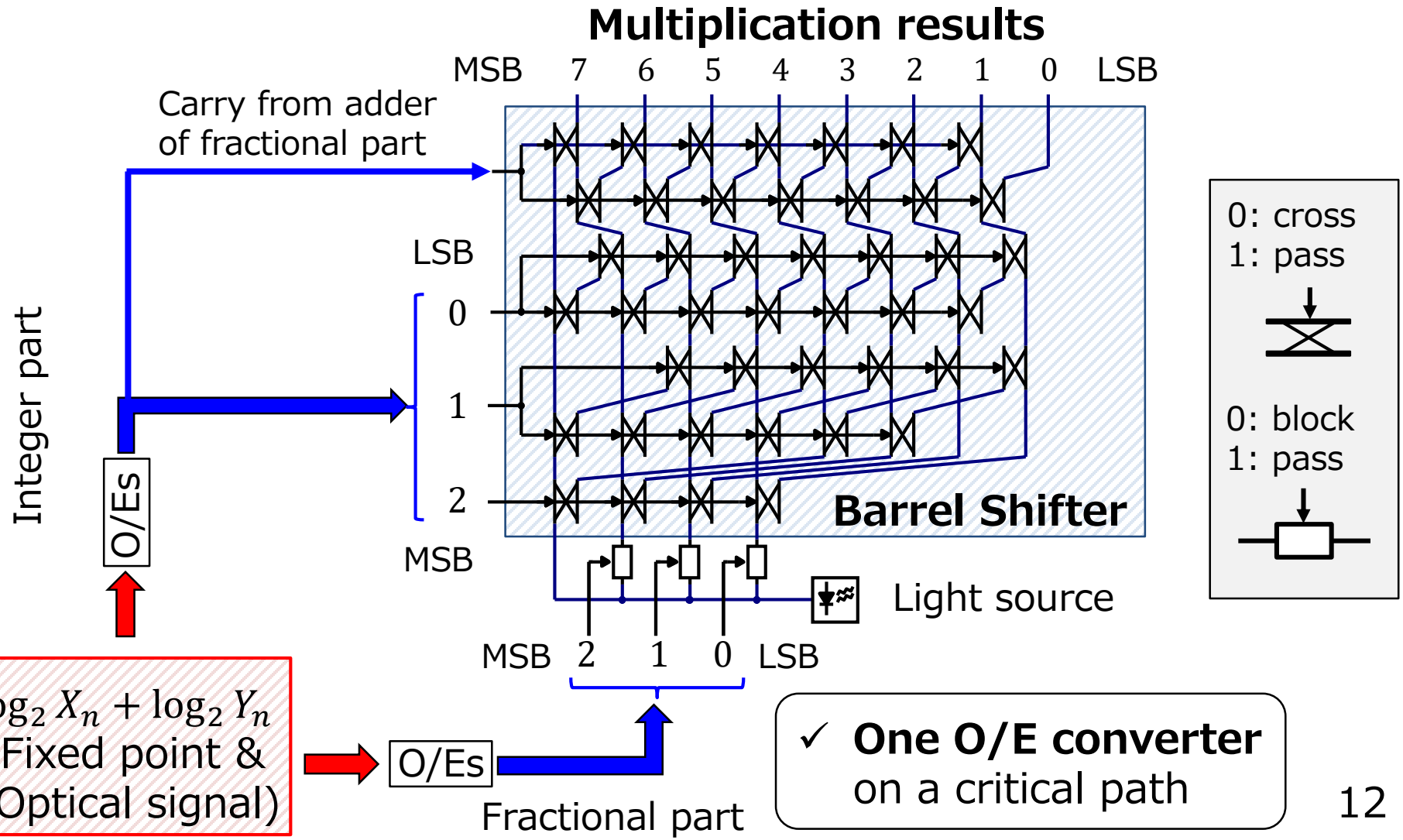
$$2^{\log_2 X_n + \log_2 Y_n}$$



✓ Only one O/E converter on a critical path for any bit width n

Barrel Shifter-Based Approximate Antilogarithm ($n = 4$)

$2^{\log_2 X_n + \log_2 Y_n}$



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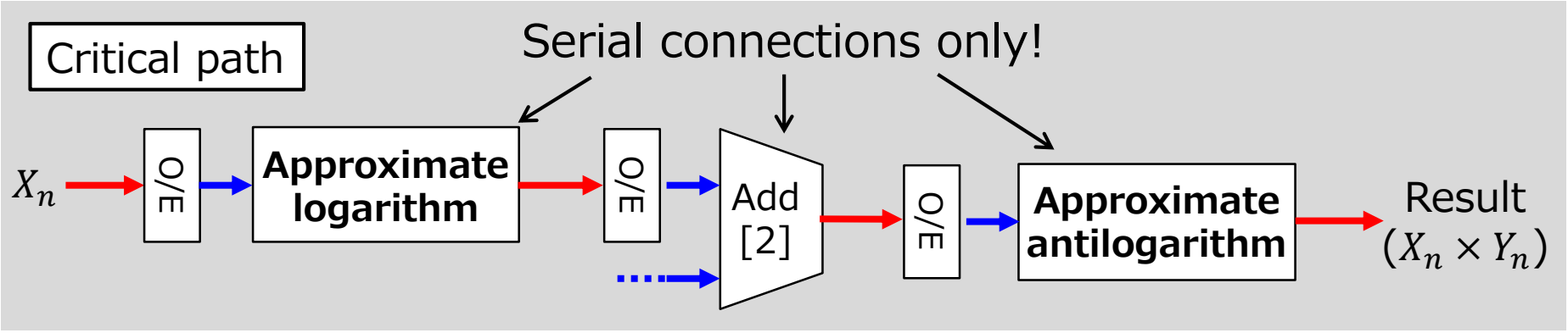
Performance Analysis

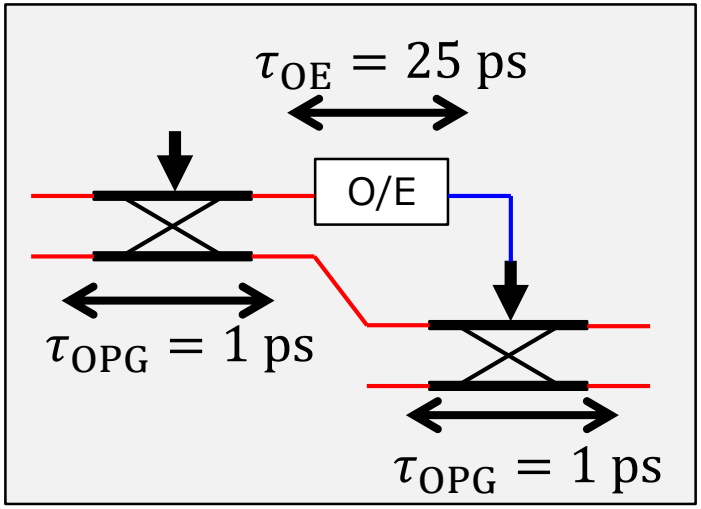


✓ Latency $= \underbrace{3\tau_{OE}}_{25\text{ ps}} + O(\underbrace{n\tau_{\mathrm{OPG}}}_{1\text{ ps}})$

✓ Error: Deterministic [3]

-11% (when $X_n = 3 \cdot 2^i$ and $Y_n = 3 \cdot 2^j$)

0% (when $X_n = 2^i$ or $Y_n = 2^j$) $i, j \in \mathbb{Z}_+$



[2] T. Ishihara, et al., International SoC Design Conference, 2016
[3] J. N. Mitchell, IRE Transactions on Electronic Computers, 1962

Performance Comparison

	Latency	Error
Conventional (array multiplier)	$> n\tau_{\mathrm{OE}}$	0
Proposed	$3\tau_{OE} + O(n\tau_{\mathrm{OPG}})$	$[-11\%, 0\%]$

$n = 32$

Conventional: > 800 ps (< 1.25 GHz)

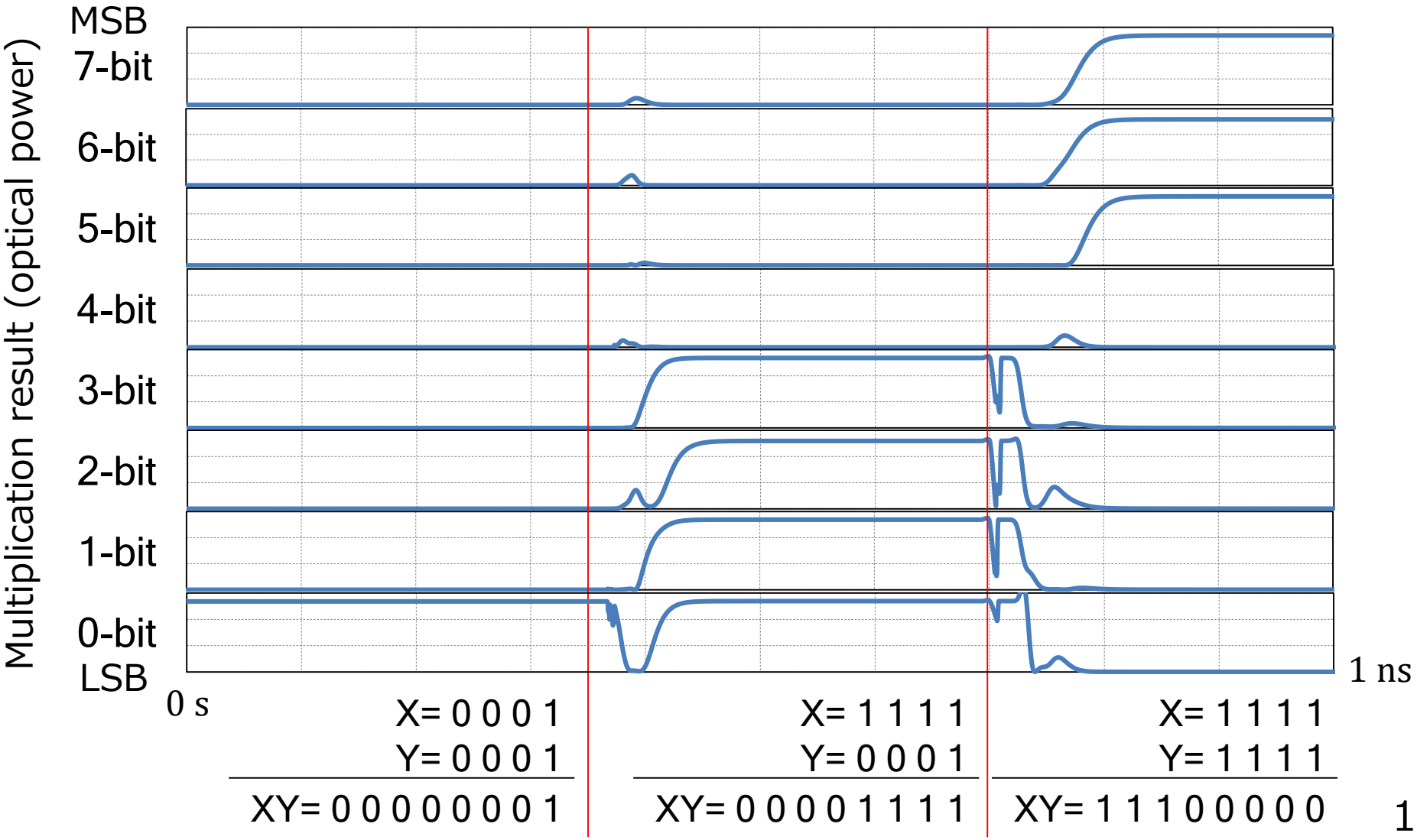
Proposed: 123 ps (8.1 GHz)

6.5 × boost

✓ More than **6.5 × faster** w/ **deterministic errors**

➡ Application: Machine learning, approximate computing

Verification Using Optoelectronic Circuit Simulator ($n = 4$)



Conclusion and Future Work

✓ Approximate parallel multiplier using optical path-gates

- Ultra-fast: $8.1\ \mathrm{GHz}$ ➡ More than $6.5\times$ faster operation
- Deterministic error: From -11% to 0%
- Correct operation confirmed by optoelectronic circuit simulator

• Future work

- Power & area evaluation
- Comparison with CMOS-based parallel multiplier