

SRISHTI PHOTONICS RESEARCH GROUP INDIAN INSTITUTE OF TECHNOLOGY, DELHI

ARCHITECTURE FOR PHOTONIC INTERCONNECTS

Janib ul Bashir and Smruti R. Sarangi

Indian Institute of Technology, Delhi

Need For Interconnection

- Cache Coherence.
 - Send the broadcast signals.
 - Receive the responses from other caches.
- Barriers.
 - Send the barrier status to each other.
- Cores need to communicate with other caches.
 - Cache misses.
 - Cache line migrations

How to Connect these Cores on a Chip?

Point to point Interconnection

- Number of wires required = $N^*(N-1)/2$.
- Will be clumsy.

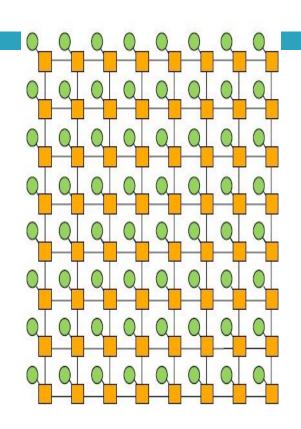


How to Connect these Cores on a Chip?

Point to point Interconnection

- Number of wires required = N*(N-1)/2.
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- Logical point to point links through a network.
- Route packets in a network.
- Will reduce the number of electrical links.



For electrical interconnects:





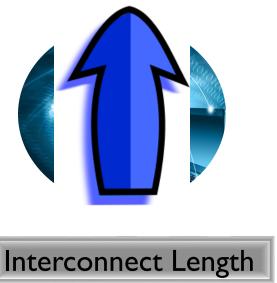






Consumption

For electrical interconnects:



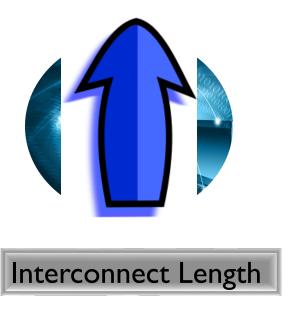






Power Consumption

□ For electrical interconnects:



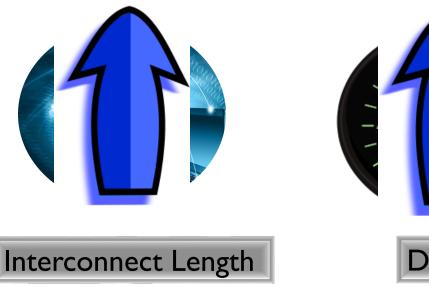


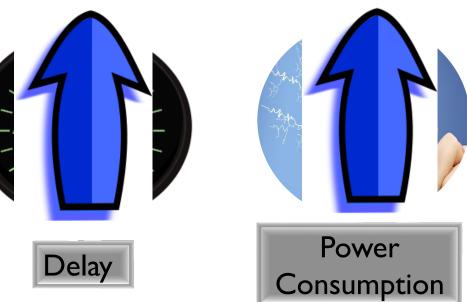




Power Consumption

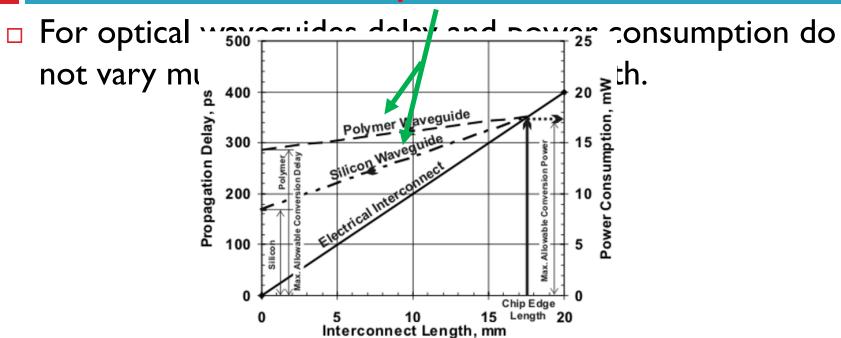
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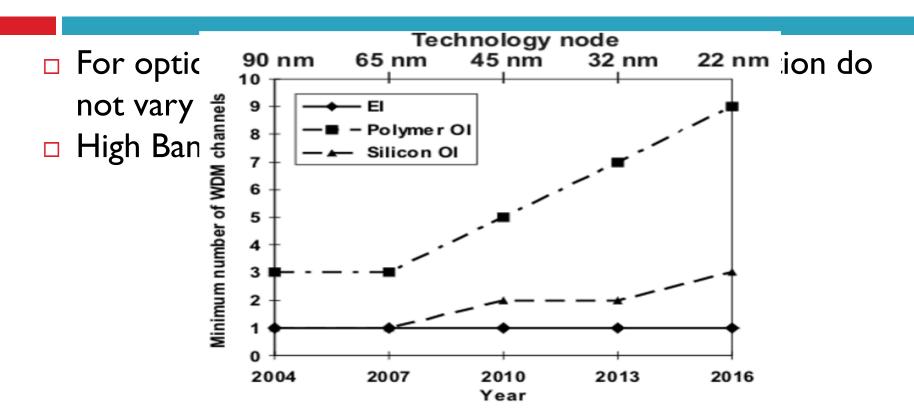
 For optical waveguides delay and power consumption do not vary much with interconnection length.

Optical

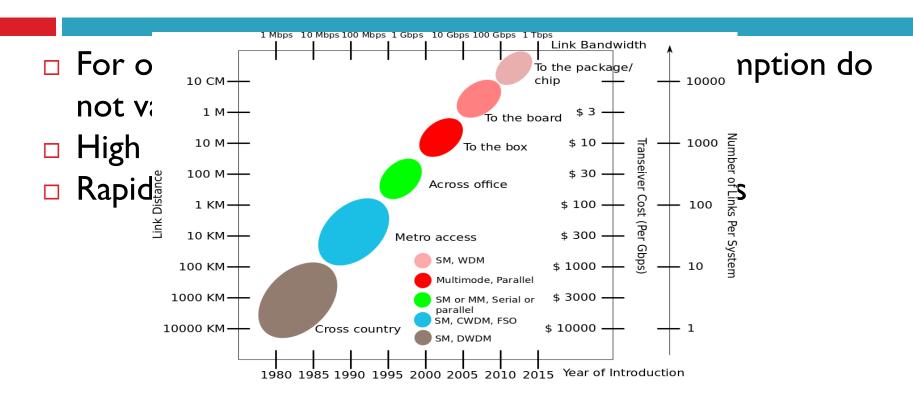


All figures reproduced from Haurylau et al. IEEE Journal of Quantum Elec.

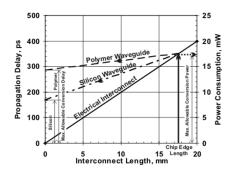
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- High Bandwidth due to WDM.

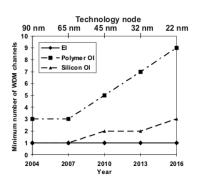


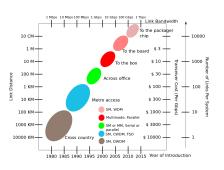
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- Rapid advances in the field of on-chip photonics



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Nanophotonics domain

Optical Devices

Optical components and challenges in their operation and fabrication

Nanophotonics
domain

Architecture

Optical Devices

Optical communication architectures, protocols, topology

Optical components and challenges in their operation and fabrication

Nanophotonics
domain

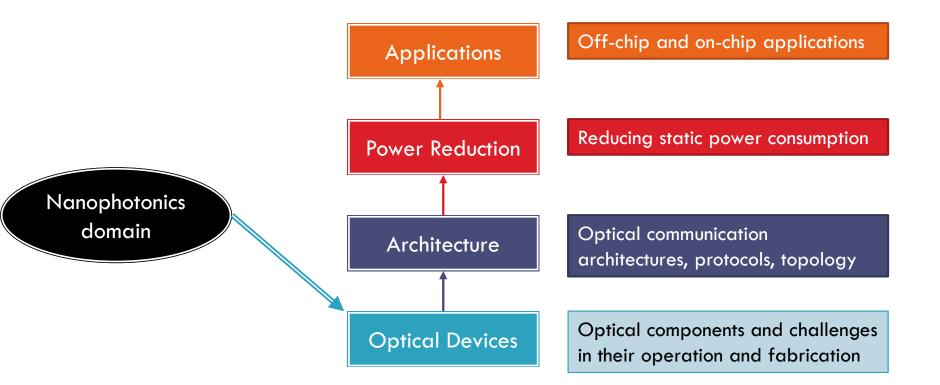
Architecture

Optical Devices

Reducing static power consumption

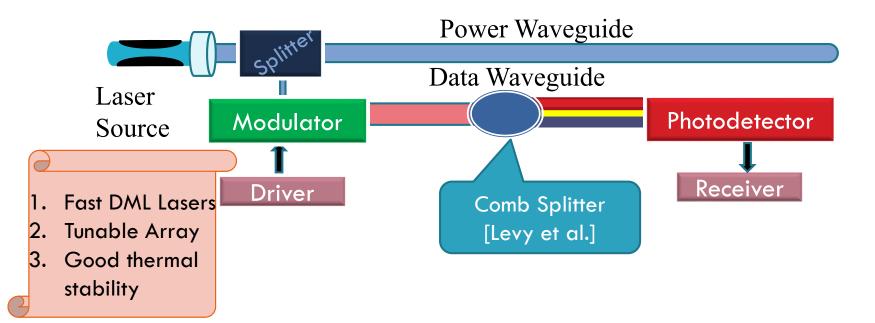
Optical communication architectures, protocols, topology

Optical components and challenges in their operation and fabrication



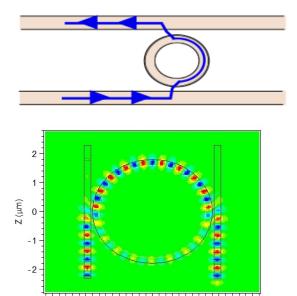
Basic Components of our Architecture

Optical Communication Framework



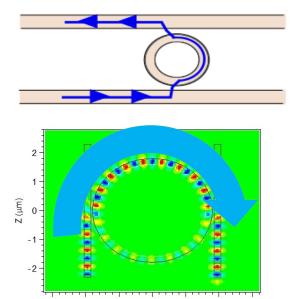
VLSI Design '14

Ring Resonator: filters light, switching and modulation.



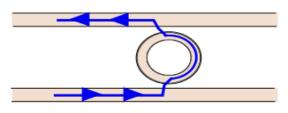
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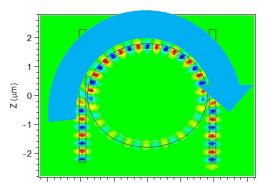
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VLSI Design '14

Ring Resonator: filters light, switching and modulation.





Splitters: split the light

Multimode Interference

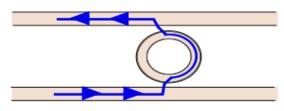
Directional coupler

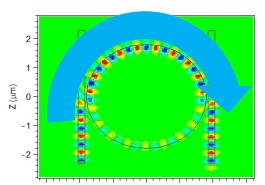
Y Junction



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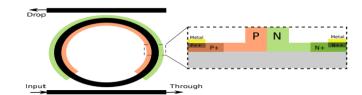
Y Junction

Limitation: Fixed split ratio

High power losses

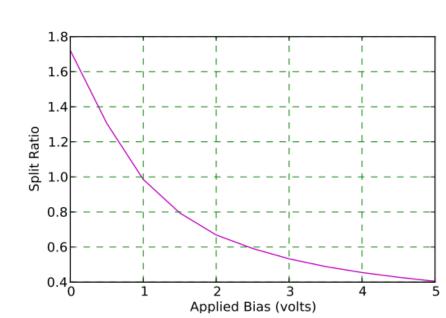
Required: Tunable splitter

Our Solution: Tunable splitter

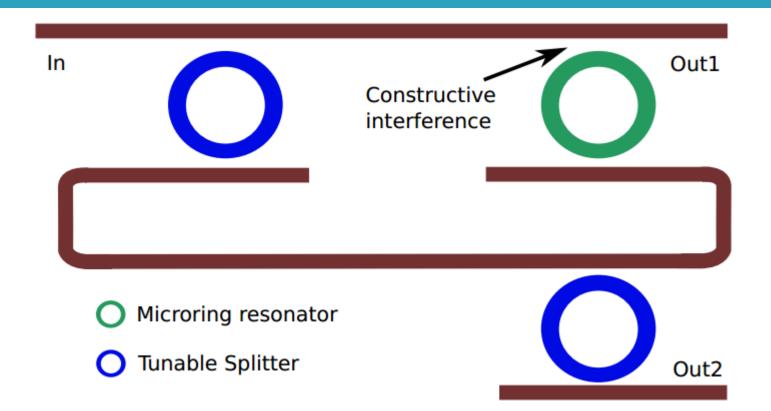


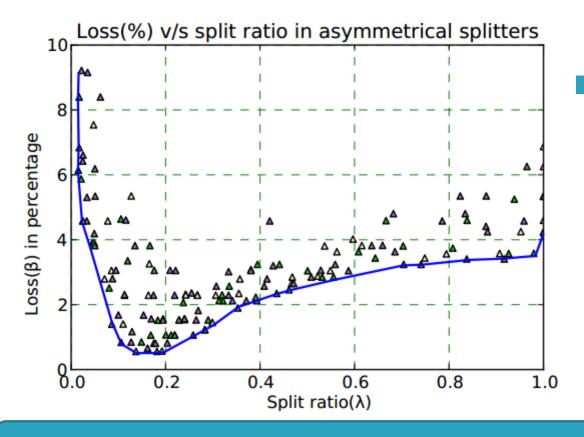
Optics
Communications '16

- ☐ A tunable power splitter which can be tuned on demand.
- □ Idea: Allow ring resonator to work in partial resonant states.
- ☐ Change the refractive index of ring resonator.
- ☐ How: Thermo-optic and Electro-optic effects.
- ☐ Achieved tuning ranges from 0.4-1.8.
- Proposed an algorithm to compute the optimal split ratios [SiPhotonics '15].
- ☐ Currently working on wide tuning range splitter and broadband splitters.



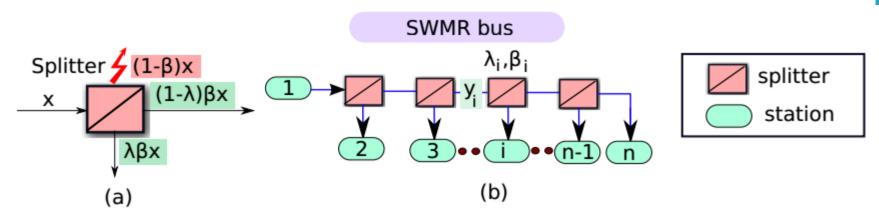
Simple Approach for Extending the Split Ratio Range





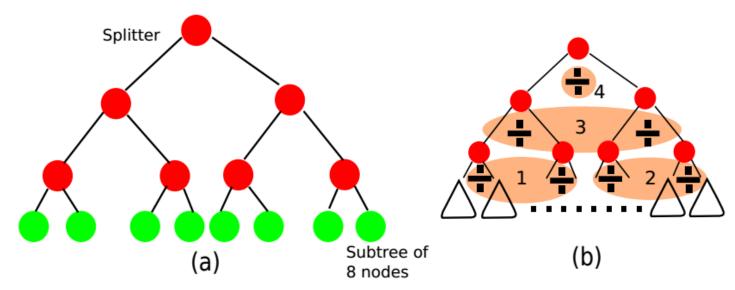
The loss varies with the split ratio

Splitters in Series



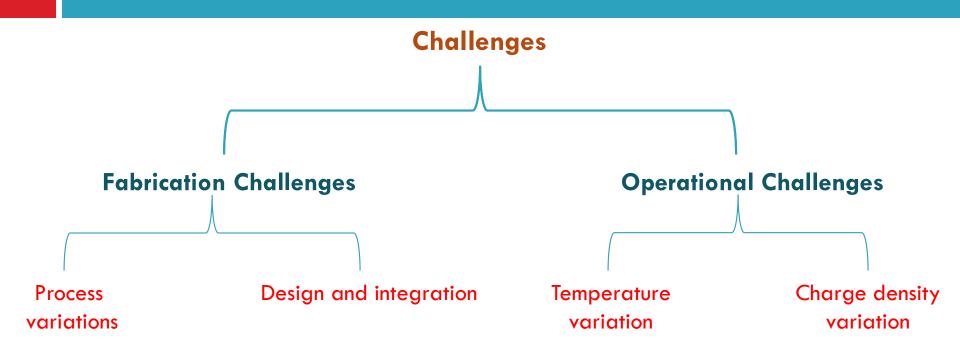
- The loss is a function of the split ratio
- Proposed an O(N) time algorithm for computing the optimal split ratio
- Very fast implementation in hardware using lookup tables

Optimal Split Ratio for Trees

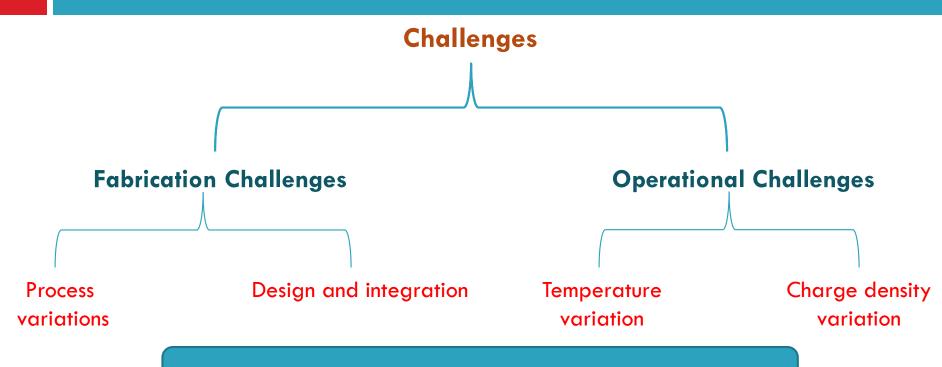


- \square O(N) time algorithm
- \square Takes 32 cycles (@2.5 GHz) for computing the optimal configuration

Optical Devices: Challenges



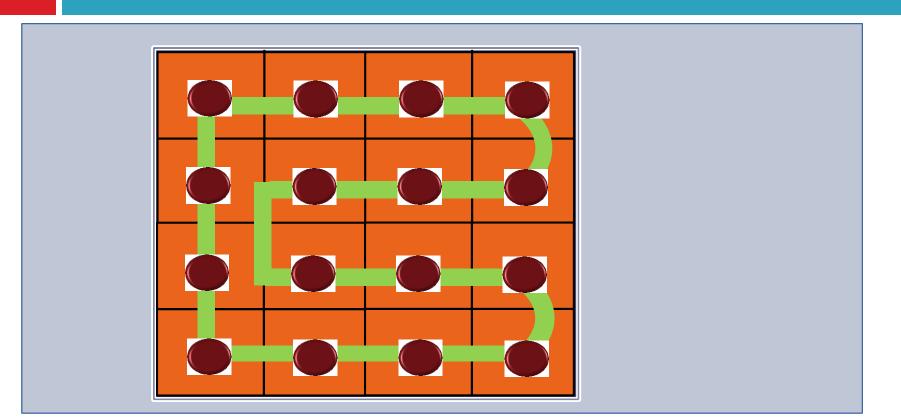
Optical Devices: Challenges

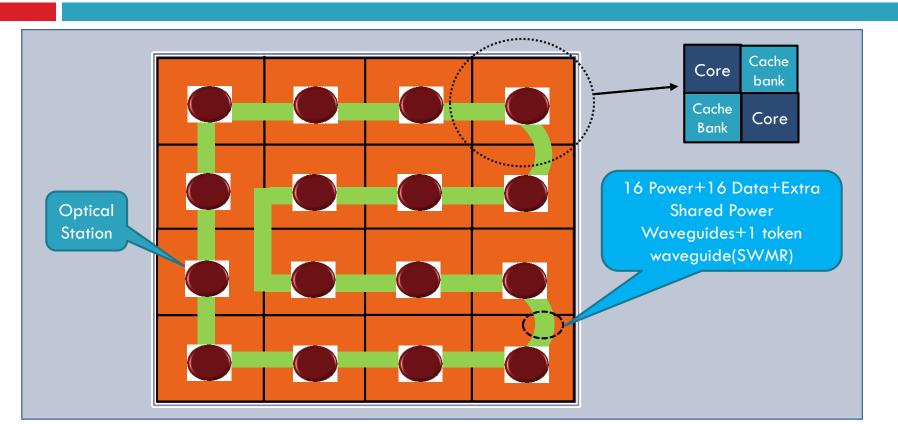


Extend the Varius Toolkit for Optical Networks

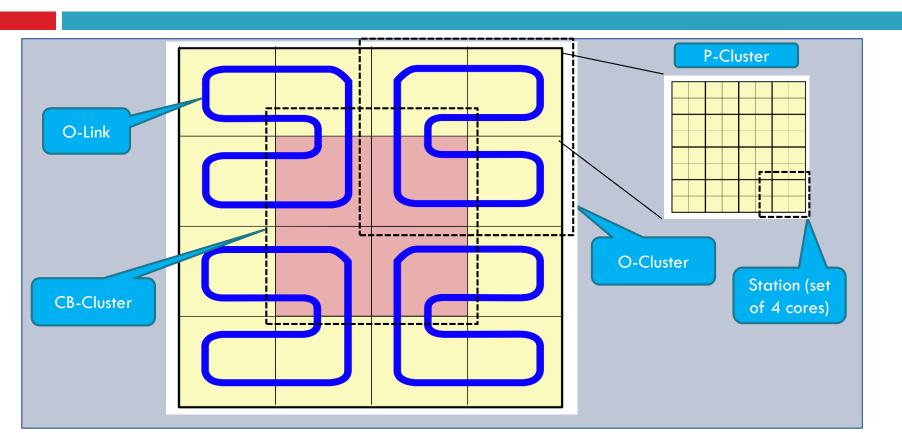
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- ☐ Combined SWMR and MWMR topologies: ColdBus [HiPC '15].



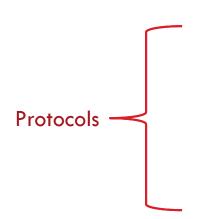


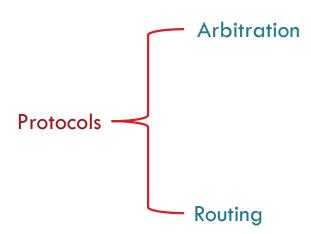
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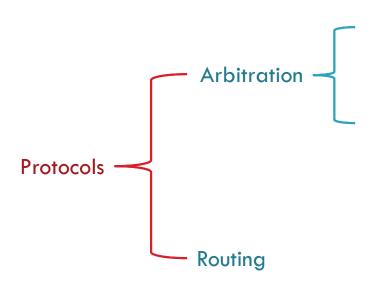


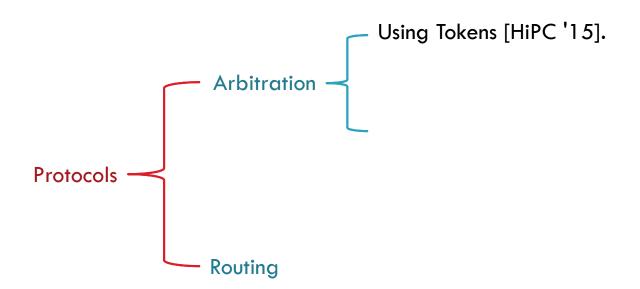
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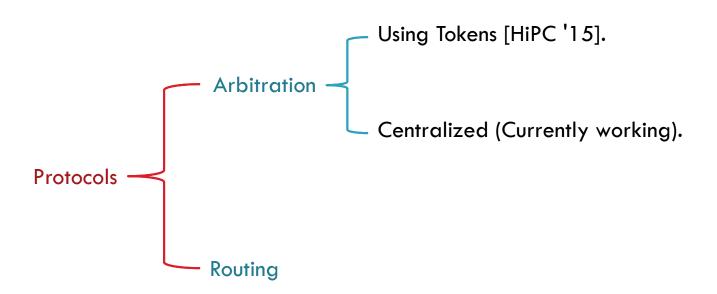
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- ☐ A multi-level architecture for a 1000 node system: BigBus[PACT '17].
- ☐ Proposed an optical architecture for a multi-chip design: NUPLet [ICCD '17].

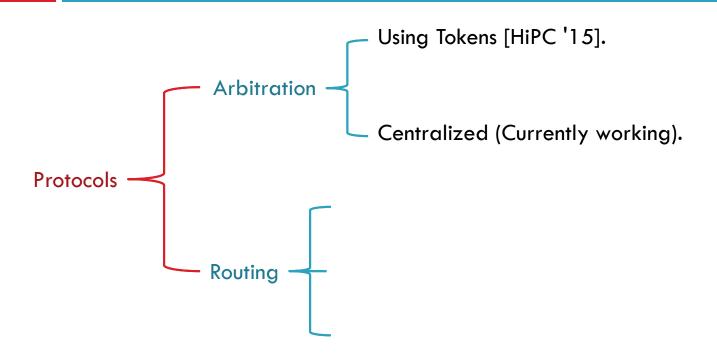


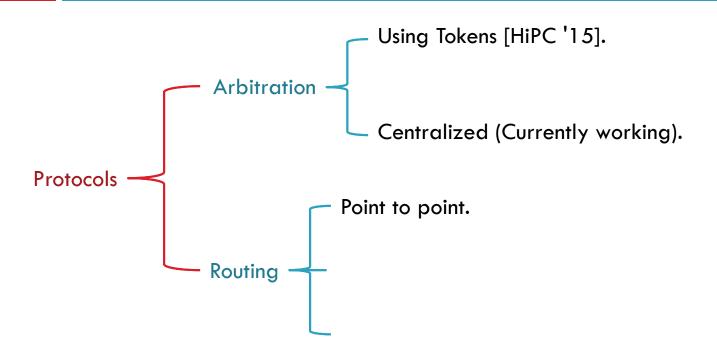


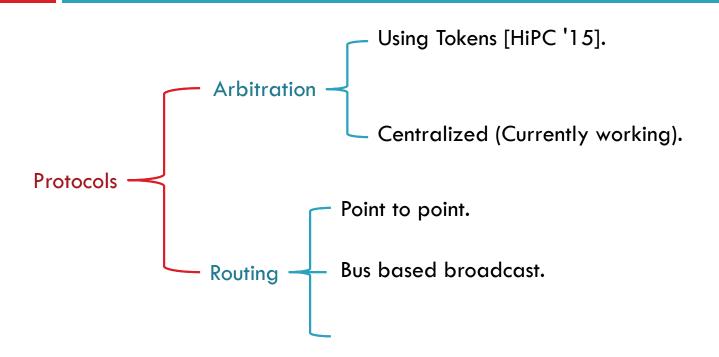


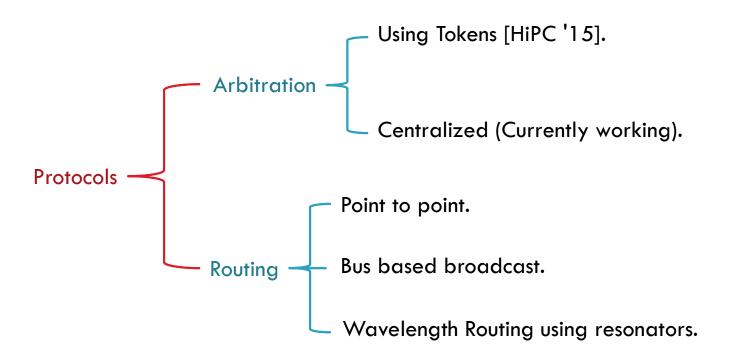




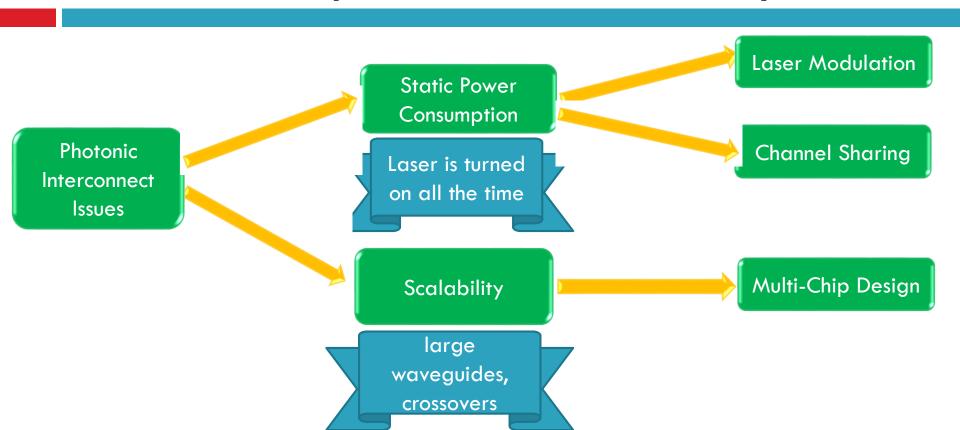




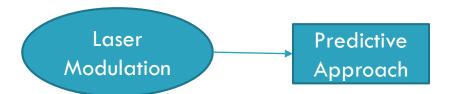


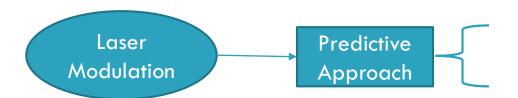


Power consumption and scalability

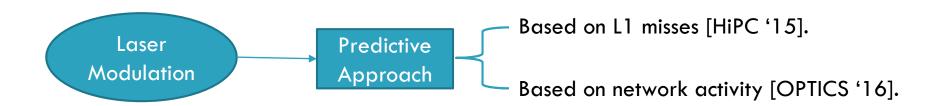


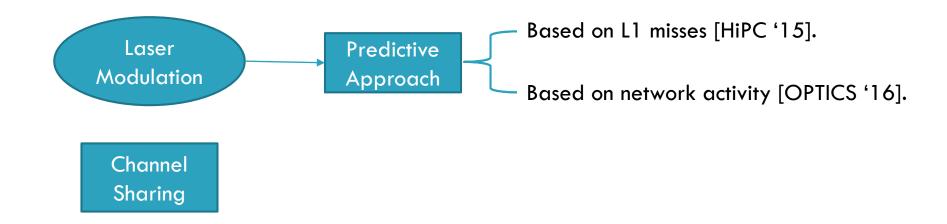
Laser Modulation

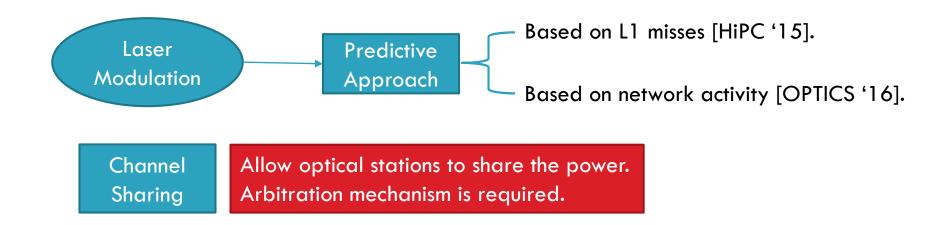


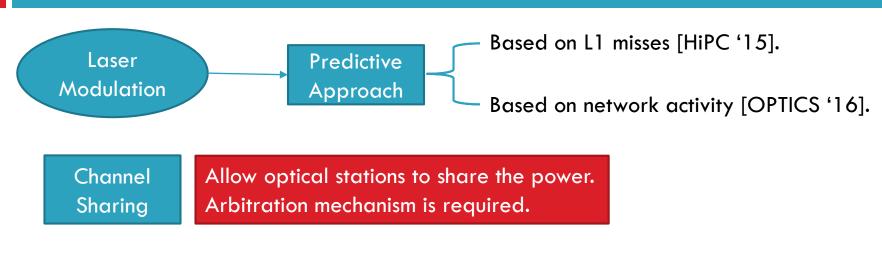




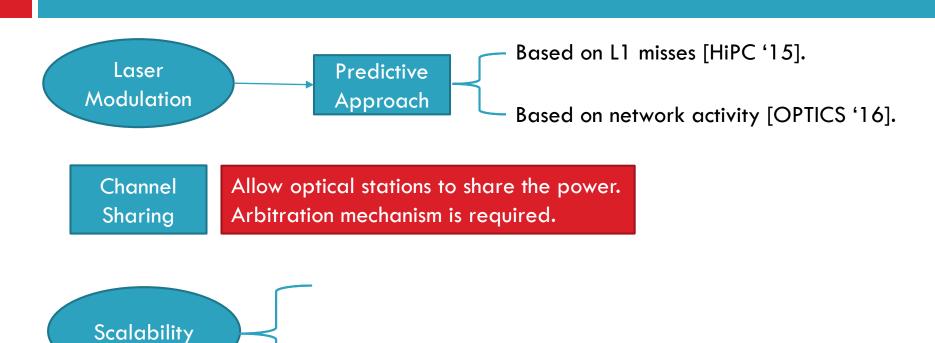


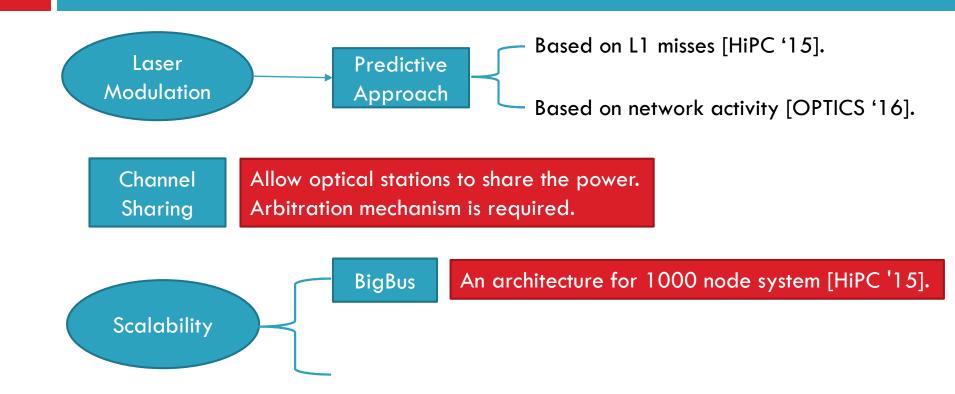


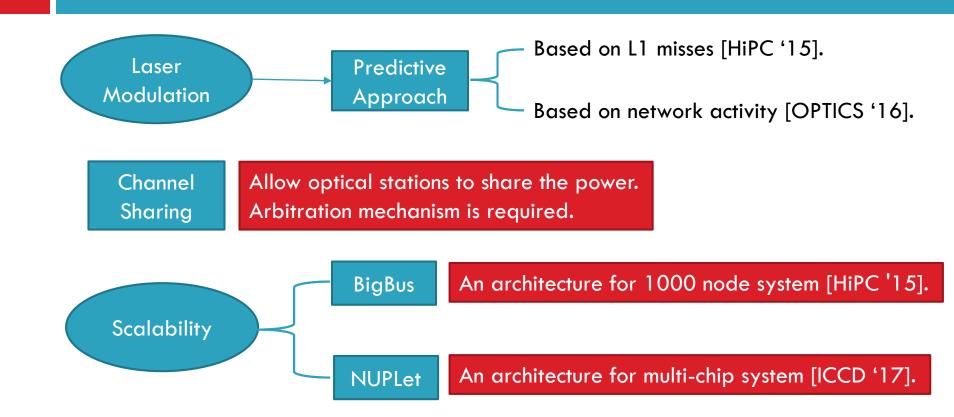




Scalability





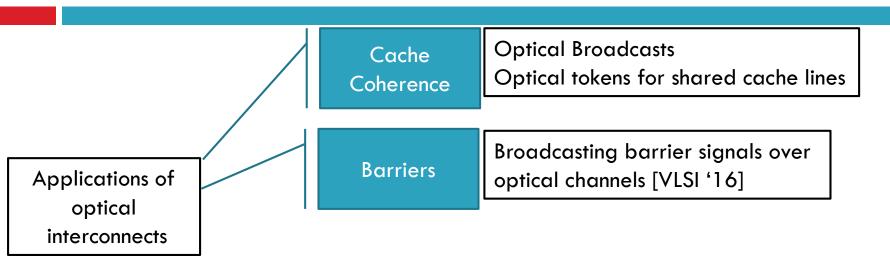


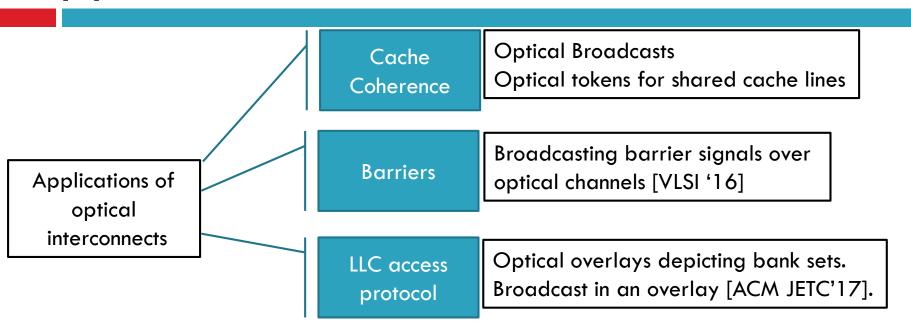
Applications of optical interconnects

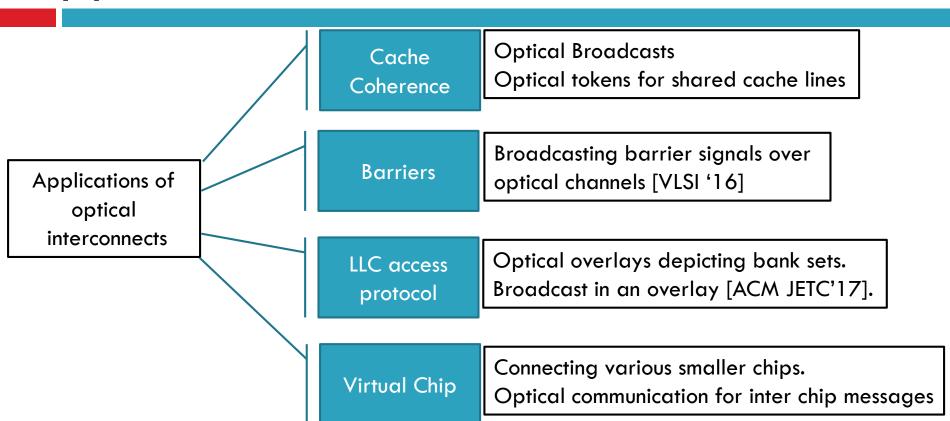
Cache Coherence **Optical Broadcasts**

Optical tokens for shared cache lines

Applications of optical interconnects

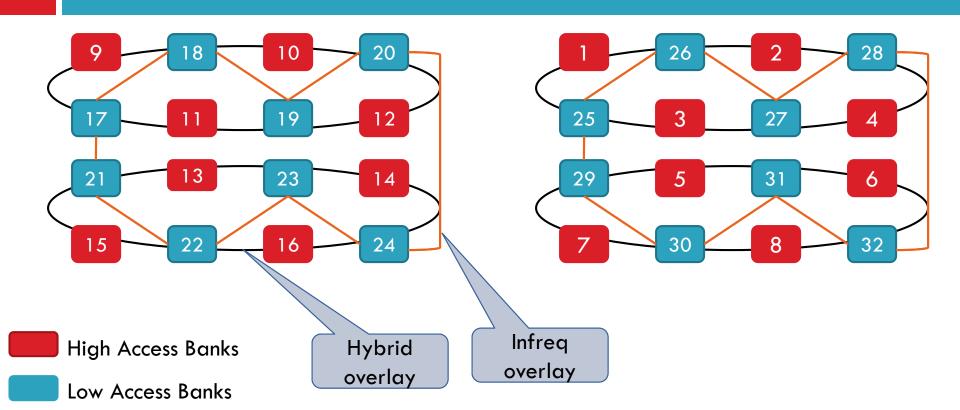


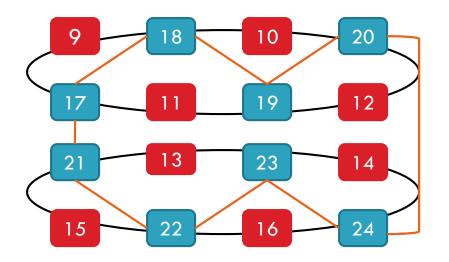


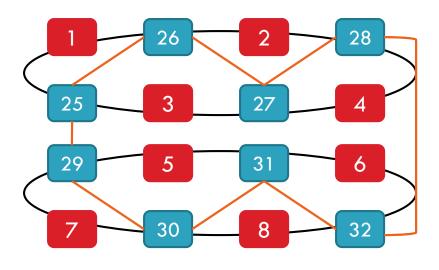


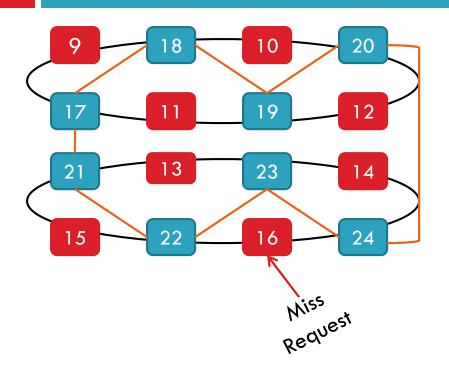
Optical NUCA (Non-uniform Cache)

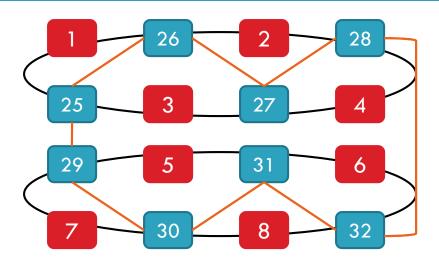
- Traditional NUCA divides banks into bank sets because of wire delays.
- Bank sets are arranged as columns.
- □ However, optical networks allow us to freely choose banks in the bank set. → Low latencies
- Each bank set is called an overlay. → virtual network
 - □ Logic for creating overlays: homogenize the number of accesses
 - Minimize contention

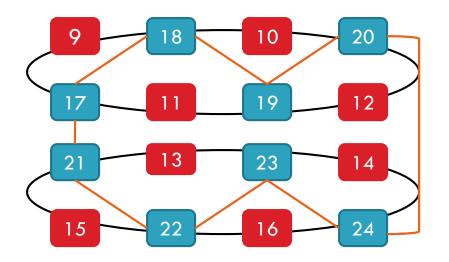


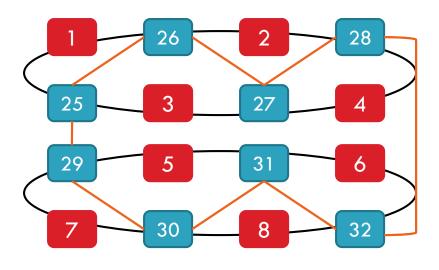


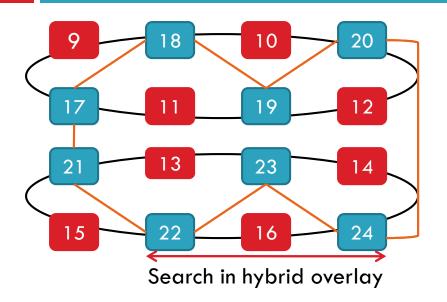


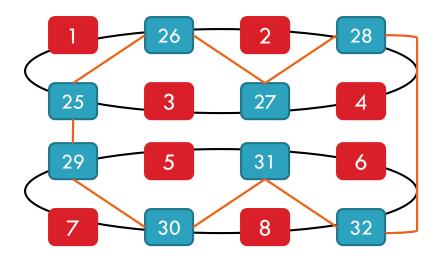


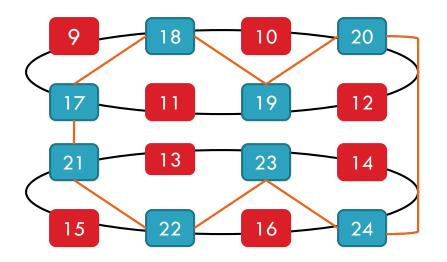


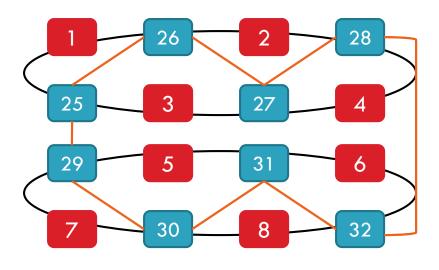


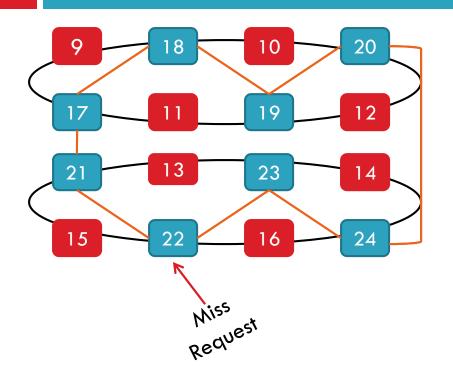


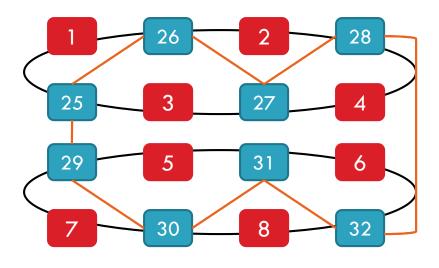


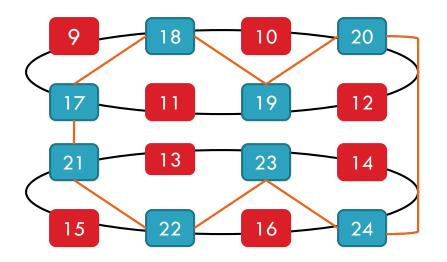


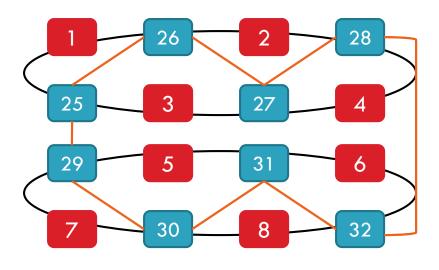


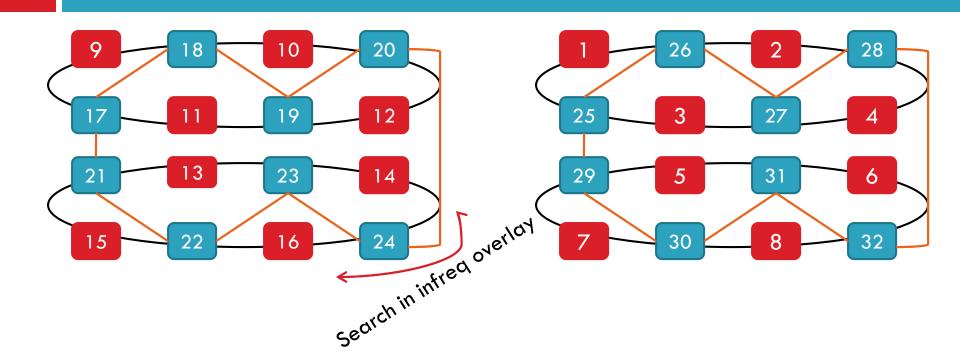


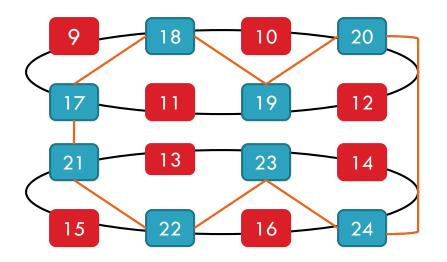


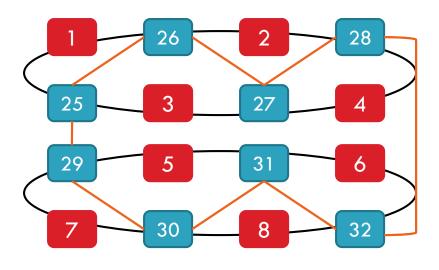






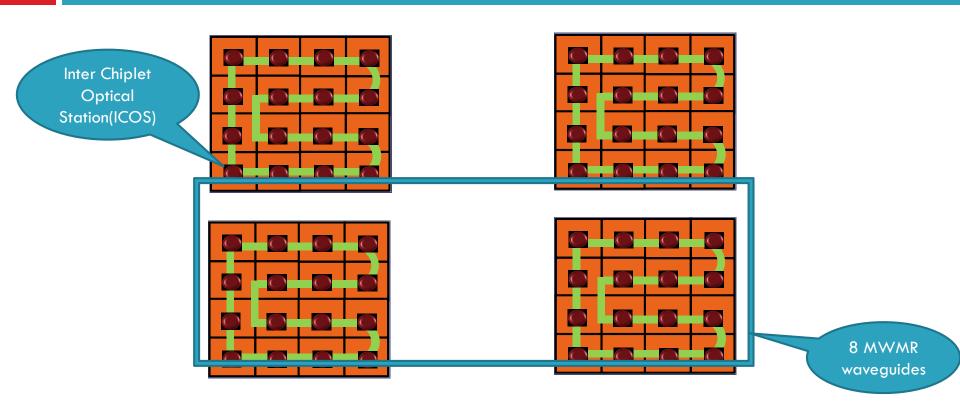


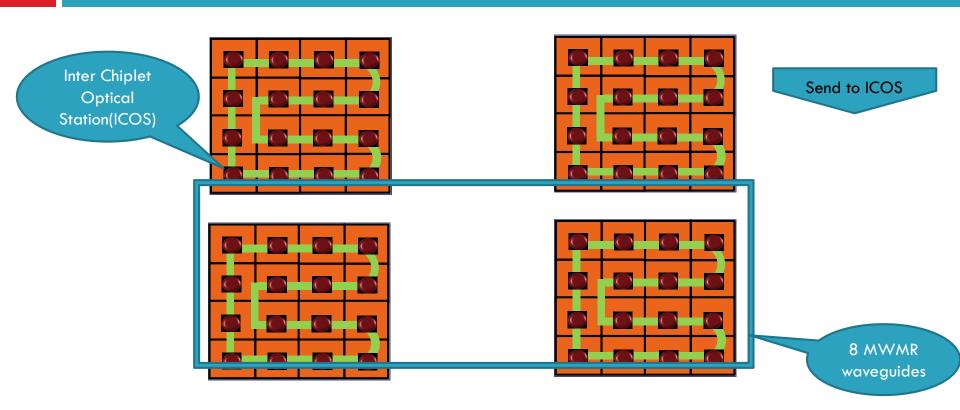


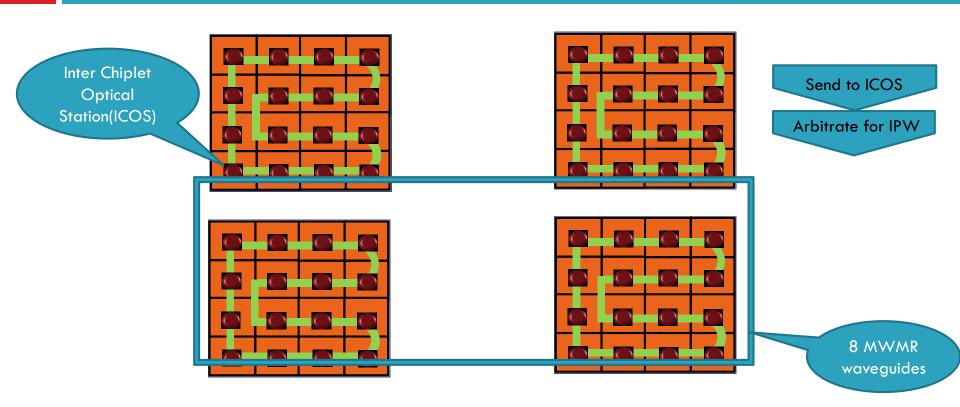


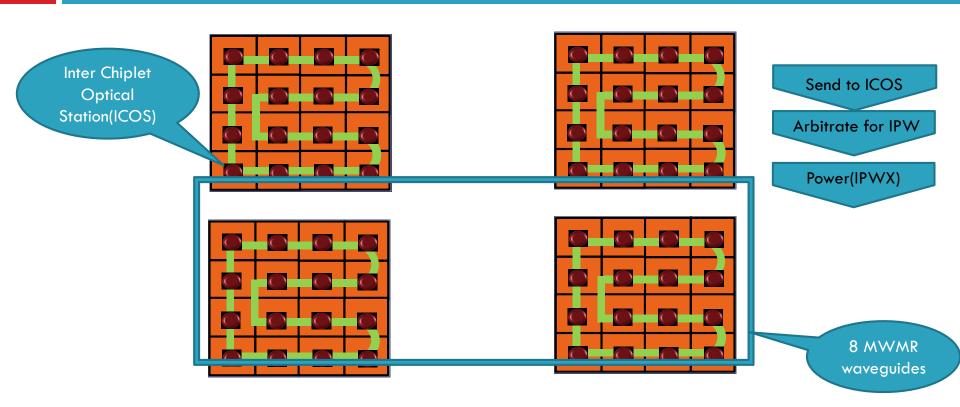
NUPLet: NUCA over chiplet

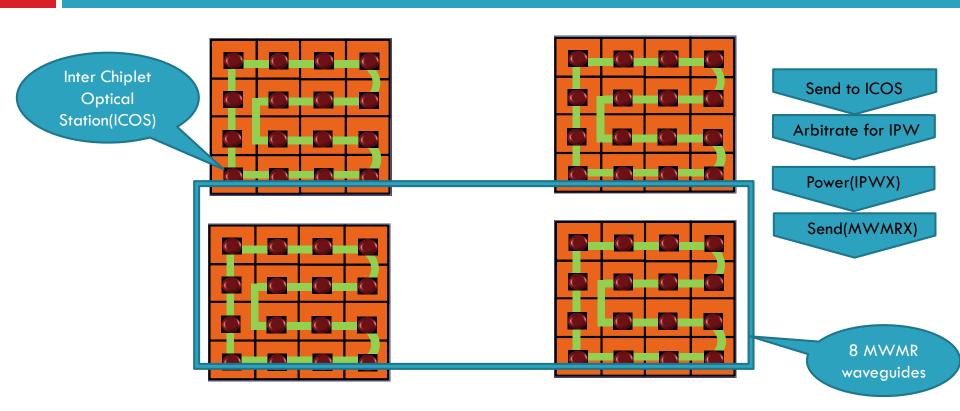
- A Virtual Chip.
- Scalability: Separation of intra and inter chiplet networks, resulting in a scalable architecture for multi-chip designs.
- Reduction in Inter Chiplet Messages: Implementation of a NUCA scheme.
- Power Consumption: A novel prediction mechanism to reduce power consumption of multi-chip networks.











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☐ We presented the issues at each layer.
☐ We proposed various novel mechanisms to handle different issues.
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□ Integrating thousands of optical components at the industrial level remains to be done.
Novel methods are required to handle fabrication and operational
level challenges.
☐ Static power consumption is still 3X more than the ideal power

