EDA for ONoCs: Achievements, Challenges, and Opportunities

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Dresden, March 23, 2018

Outline

Placement
- PROTON (nonlinear)
- PLATON (force-directed)

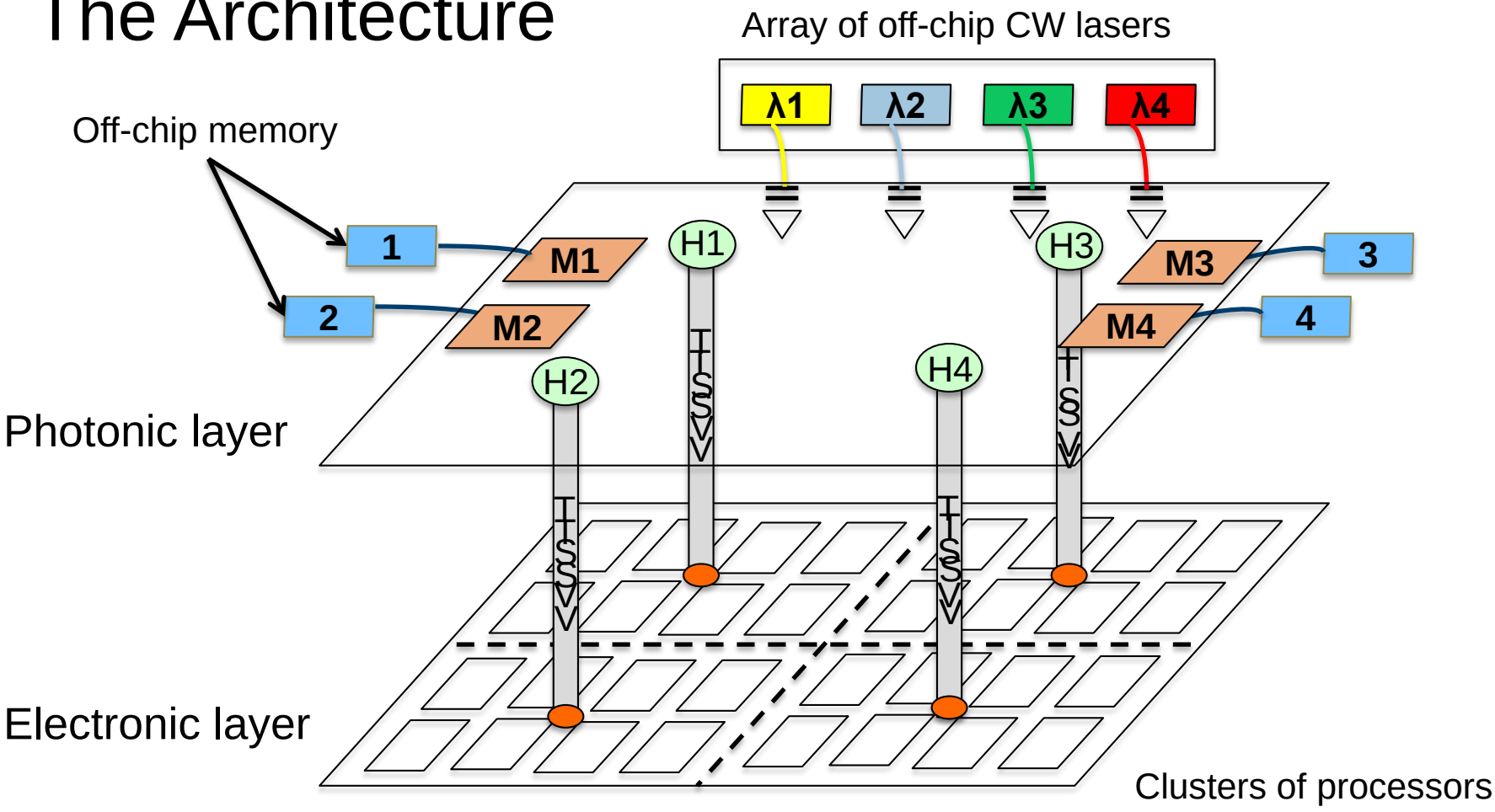
Maze Routing

PlanarONoC

Challenges

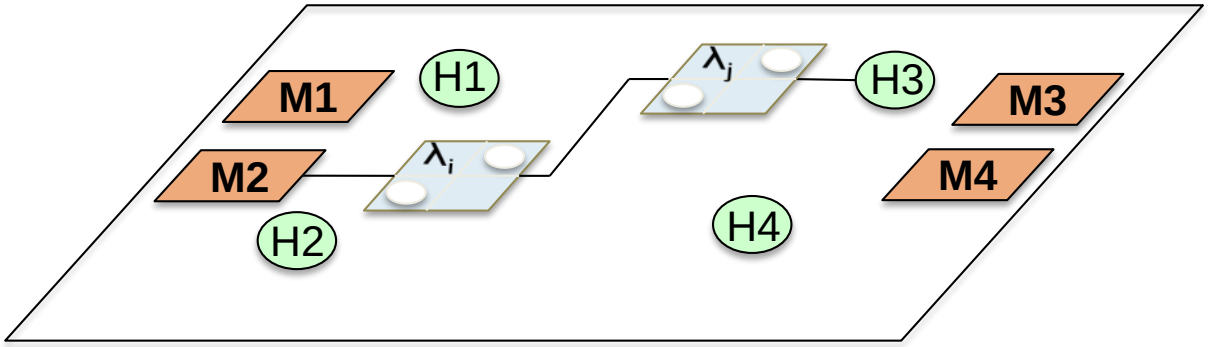
Opportunities

The Architecture

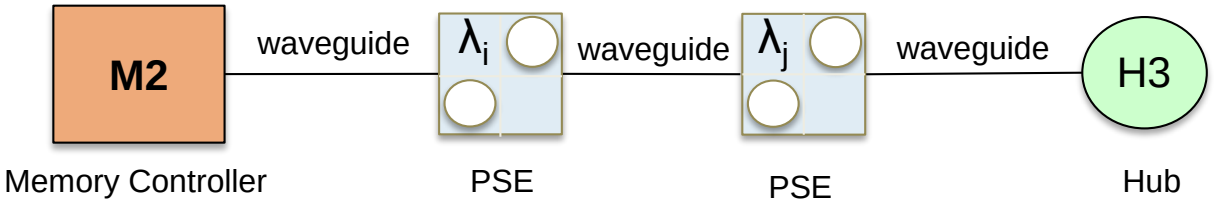


The Photonic Layer

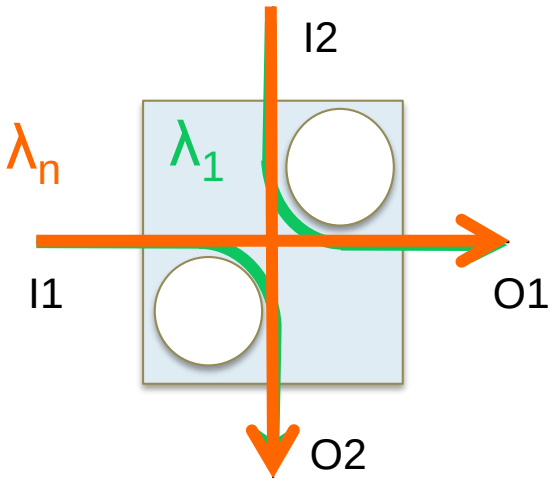
Photonic layer



A **path** connects two hubs or a hub and a memory controller via waveguides and possibly passive Photonic Switching Elements (PSEs)

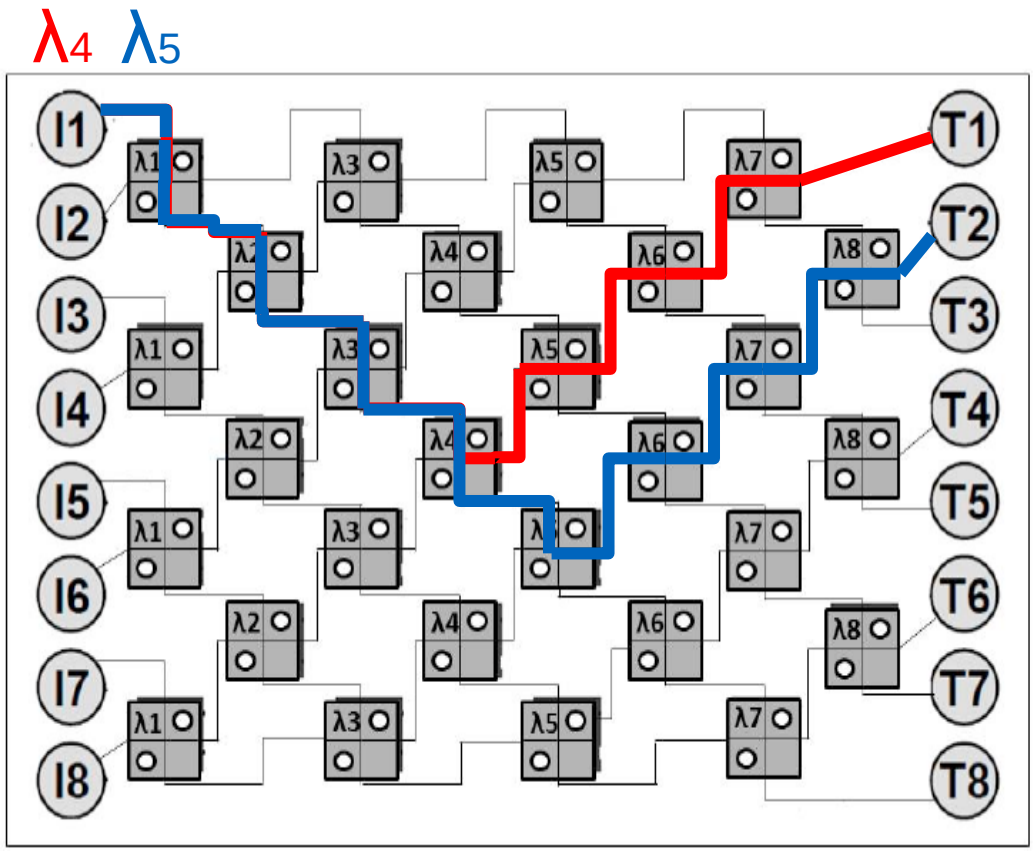


The Logic Scheme of the Optical Layer



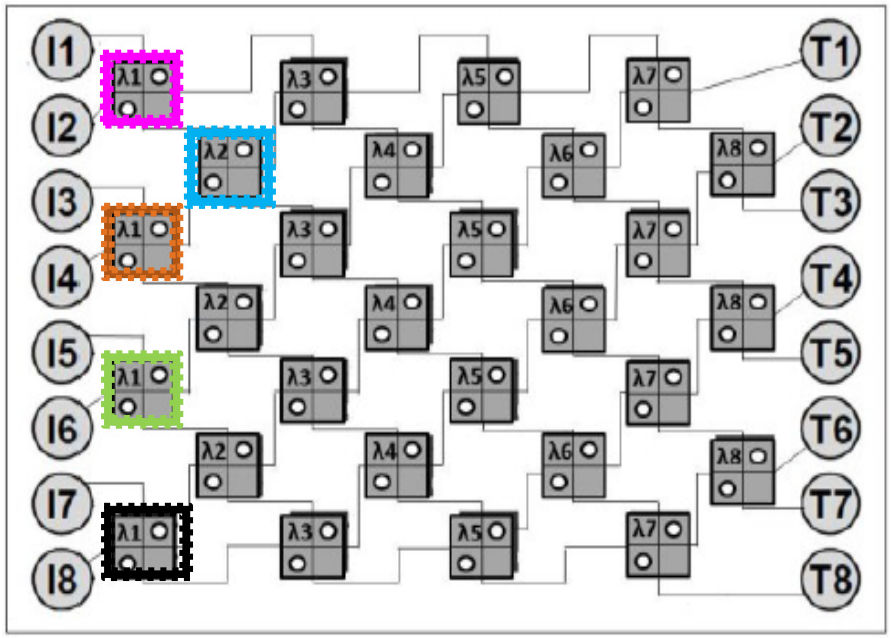
Wavelength λ_1 is redirected

Wavelength λ_n crosses

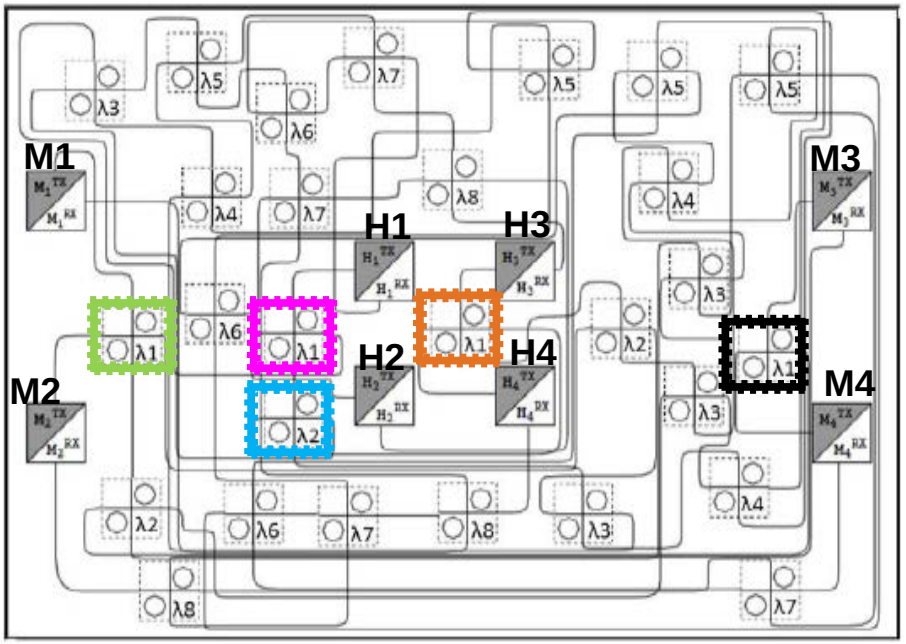


Example: 8x8 λ-Router [Scandurra+ NoCArc'08]

Logic Scheme vs. Physical Design



Logic Scheme

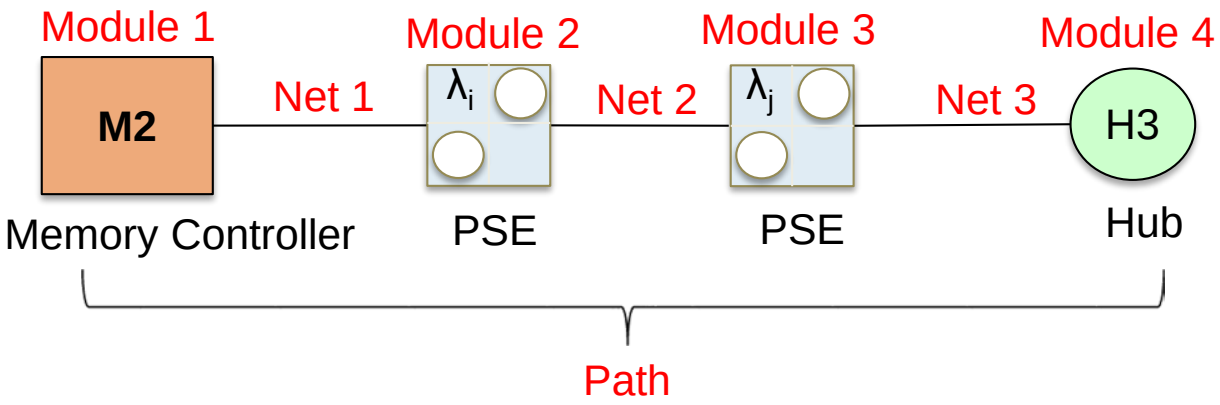


Manually created layout
[Ramini+ NOCS'12]

Creating layout manually is time consuming, error prone and often suboptimal

⇒ Automatic place & route tools for 3D optical NoCs are needed

Conventions



Minimize total laser power consumption:

$$P_{opt} = 10^{\frac{il_{max}+S}{10}} n$$

il_{max} = maximum insertion loss

n = number of wavelengths

S = detector sensitivity

Placement and Routing Problem

Netlist, chip area, positions & dimensions of hubs and memory controllers, dimensions of PSEs

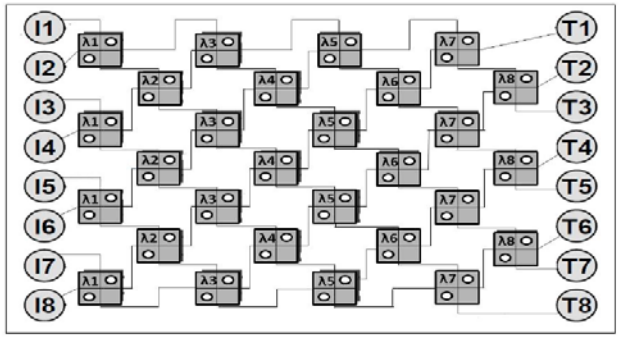
Minimize **maximum insertion loss** over all paths, e.g. minimize

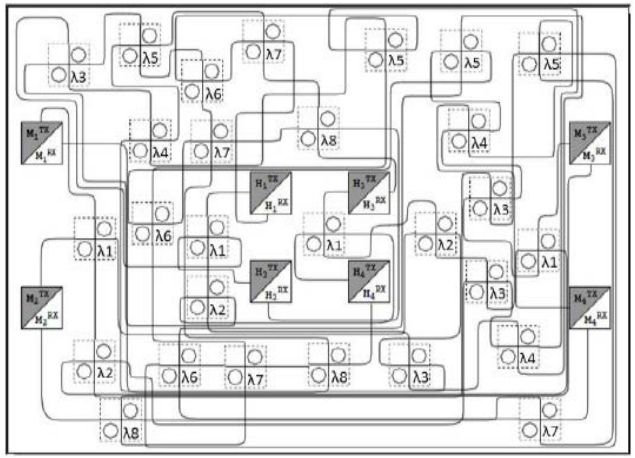
- Waveguide length
- Number of crossings between waveguides
- Number of bends

Constraints:

- Place and route inside chip area
- No overlap

Valid and optimal layout





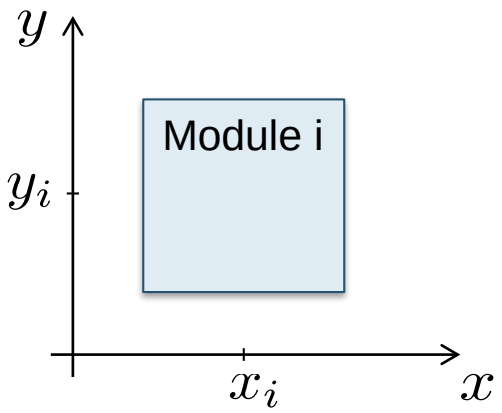
Optimization Problem

Find positions of PSEs $\mathbf{x}$ and location of waveguides $\mathbf{r}$ by

$$\min_{\mathbf{x},\mathbf{r}} \max_{p \in P} il_p(L_p(\mathbf{x},\mathbf{r}), C_p(\mathbf{x},\mathbf{r}))$$

$$\text{s.t. constraints}$$

$\mathbf{x}$: Positions of all PSEs
$\mathbf{r}$: Positions of all waveguides
P : Set of all paths
L_p: Waveguide length of path p
C_p: Number of crossings in path p



Constraints: Place PSEs and waveguides inside chip area without overlap

Placement and Routing Tools for ONoCs

	Place-ment	Routing	3D	Minimize Laser Power Consumption	Speed of Placement
[Seo+ ISQED'05]	✓	✓	✗	✗	N/A
[Minz+ TCPT'07]	✗	✓	✓	✗	N/A
[Ding+ DAC'09]	✗	✓	✓	✓	N/A
[Hendry+ DATE'11]	✗	✓	✓	✓	N/A
[Condrat+ TCAD'14]	✗	✓	✓	✓	N/A
PROTON(+) ([ICCAD'13], [JETCS'15])	✓	✓	✓	✓	○
PLATON ([ISPD'16])	✓	✓	✓	✓	+

PROTON

Placement

- Approximate waveguide length
- Approximate number of crossings
- Solve non-linear optimization problem

Routing

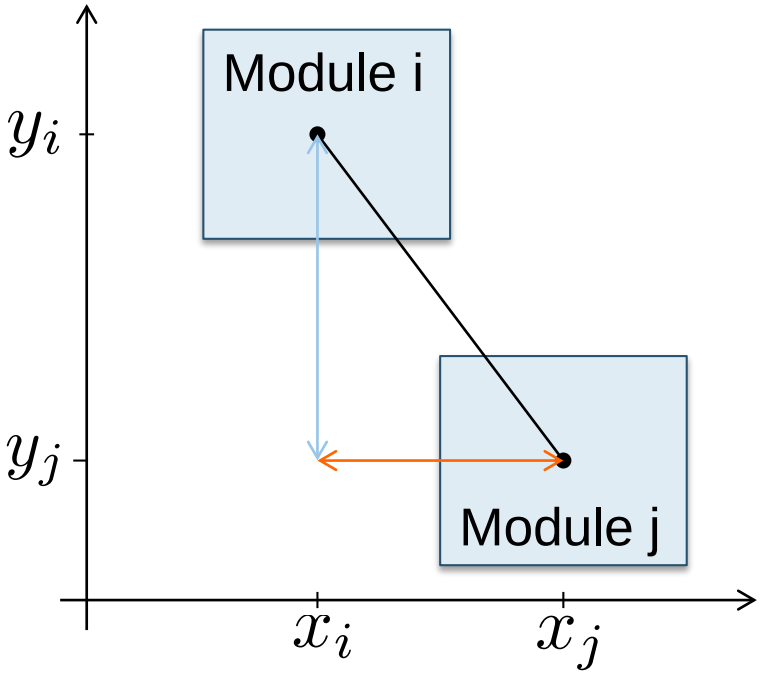
- Route waveguides by allowing but penalizing crossings
- Maze router

Approximation of Waveguide Length

Minimize **Euclidean** distance of optical modules

$\tilde{L}_p(\mathbf{x})$ = approximated waveguide length of path p

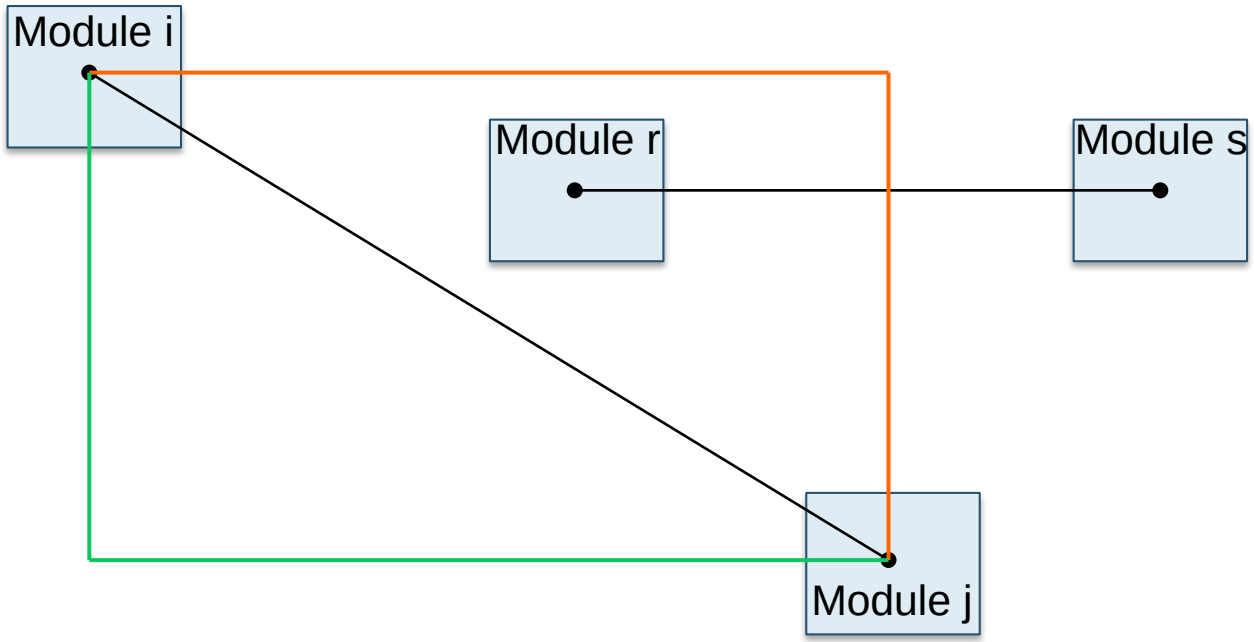
N_p = set of all nets in path p



$$\tilde{L}_p(\mathbf{x}) = \sum_{(i,j)\in N_p} \sqrt{(x_i - x_j)^2 + (y_i - y_j)^2}$$

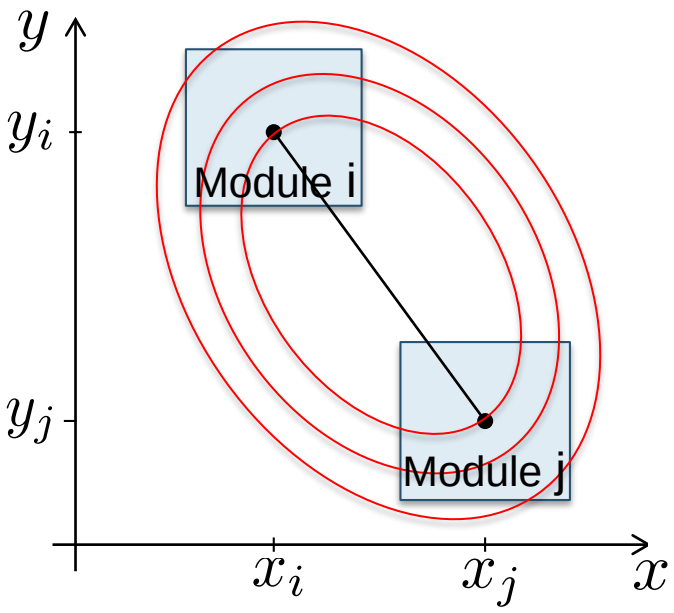
Approximate Number of Crossings 1/3

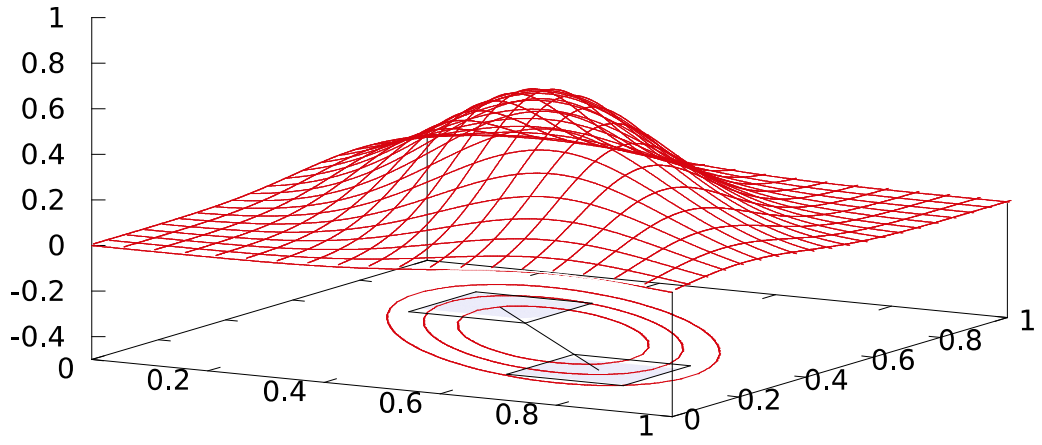
Idea: If straight lines connecting the modules are close to each other, the probability of a waveguide crossing is high



Approximate Number of Crossings 2/3

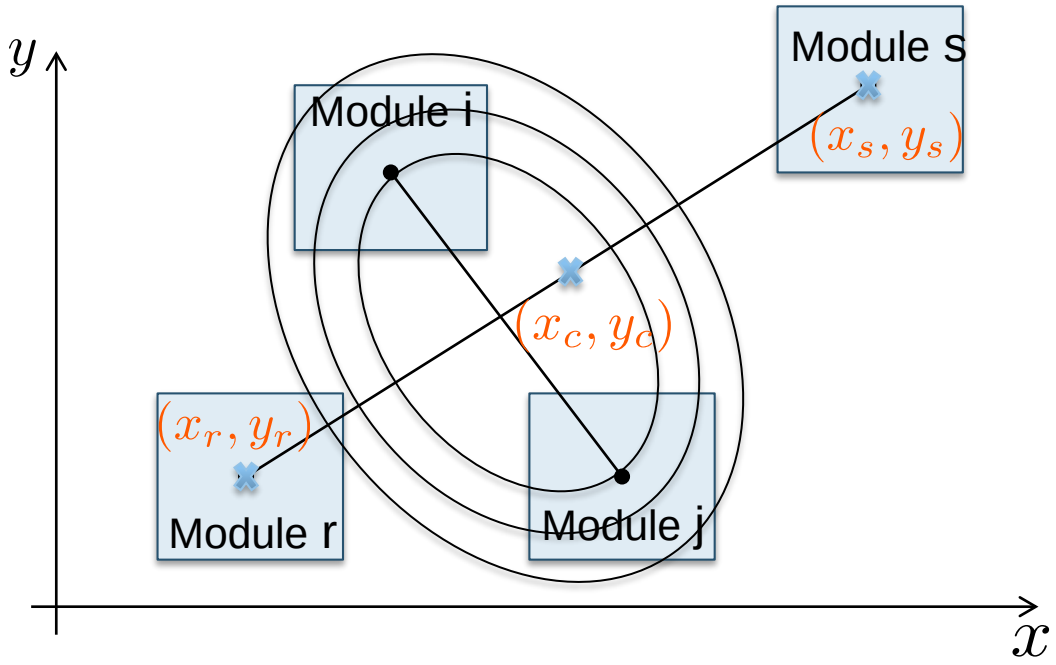
- Smooth function
- Define ellipse around straight line, which is level curve of an **exponential function** $G_{ij}(x, y)$





Approximate Number of Crossings 3/3

Approximated number of crossings $\tilde{C}_p$ is calculated using the weights of Simpson's rule



$$\tilde{C}_p = \sum_{(i,j)\in N_p} \sum_{(r,s)\in N\setminus(i,j)} \frac{1}{6}\left(G_{ij}(x_r, y_r) + 4G_{ij}\,(x_c, y_c) + G_{ij}(x_s, y_s)\right)$$

Solving the Optimization Problem

- Find positions $\mathbf{x}$ of all PSEs

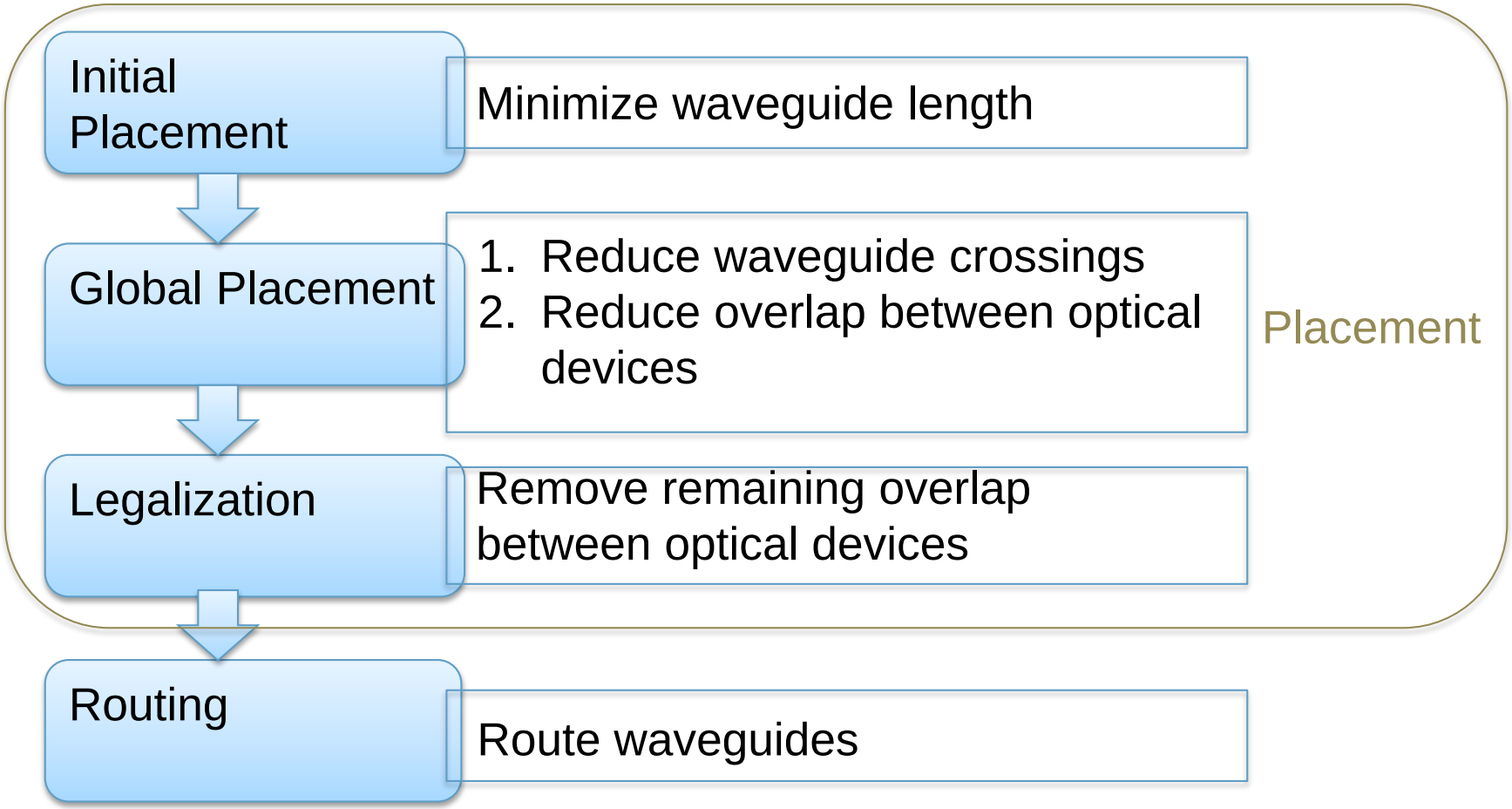
$$\min_{\mathbf{x}} \max_{p \in P} \alpha \cdot \tilde{L}_p(\mathbf{x}) + \beta \cdot \tilde{C}_p(\mathbf{x}) \qquad 0 < \alpha, \beta < 1, \ \alpha + \beta = 1$$

$$\text{s.t. constraints}$$

P : Set of all paths
$\tilde{L}_p(\mathbf{x})$: Approximated waveguide length of path p
$\tilde{C}_p(\mathbf{x})$: Approximated number of crossings in path p

- Constraints: Place all PSEs inside chip area without overlap
- Nonlinear Optimization Problem solver: IPOPT (Interior point method)

PLATON: Force-Directed Placement



Initial Placement

$$\tilde{L}(\mathbf{x},\mathbf{y}) = \sum_{p\in P}\sum_{(i,j)\in N_p} \frac{\omega_{ij}}{2}(x_i - x_j)^2 + \frac{\omega_{ij}}{2}(y_i - y_j)^2$$

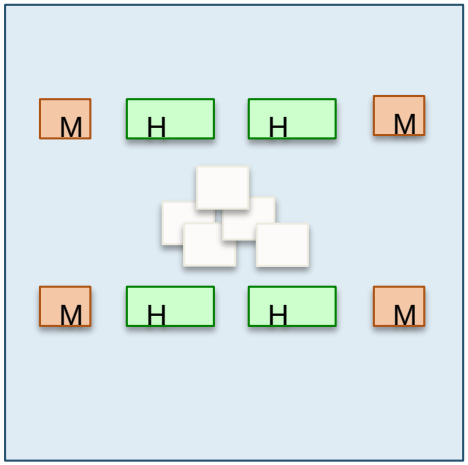
$$= \frac{1}{2}\mathbf{x}^T\mathbf{C_x}\mathbf{x} + \mathbf{x}^T\mathbf{d_x} + \frac{1}{2}\mathbf{y}^T\mathbf{C_y}\mathbf{y} + \mathbf{y}^T\mathbf{d_y}$$

Minimize waveguide length

$$\nabla_x \tilde{L}(\mathbf{x},\mathbf{y}) = \mathbf{C_x}\mathbf{x} + \mathbf{d_x} = \mathbf{0} = F_x^{net}$$

$$\nabla_y \tilde{L}(\mathbf{x},\mathbf{y}) = \mathbf{C_y}\mathbf{y} + \mathbf{d_y} = \mathbf{0} = F_y^{net}$$

Solve linear equation system e.g. by Conjugate Gradient method (CG)



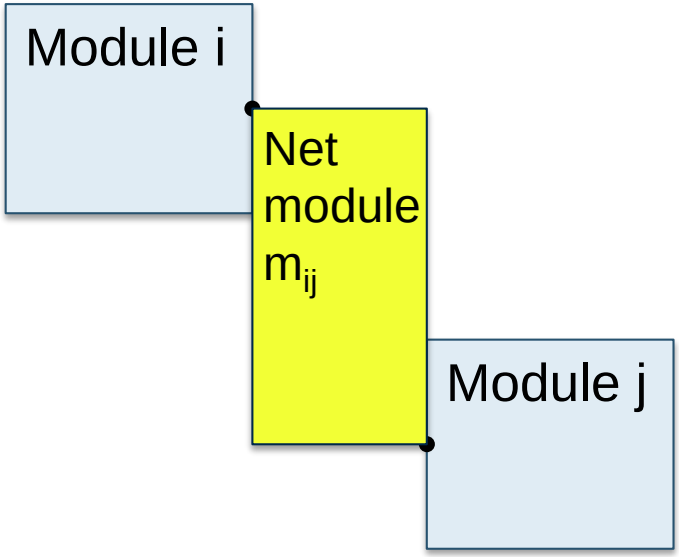
Global Placement

While net module overlap > 20%

$$\mathbf{F}^{net} + \mathbf{F}^{hold} + \mathbf{F}^{move,cross} = \mathbf{0}$$

While overlap between optical devices > 20%

$$\mathbf{F}^{net} + \mathbf{F}^{hold} + \mathbf{F}^{move} = \mathbf{0}$$



Hold force $\mathbf{F}^{hold}$ compensates net force $\mathbf{F}^{net}$

Move force $\mathbf{F}^{move}$ attracts optical devices to empty spaces

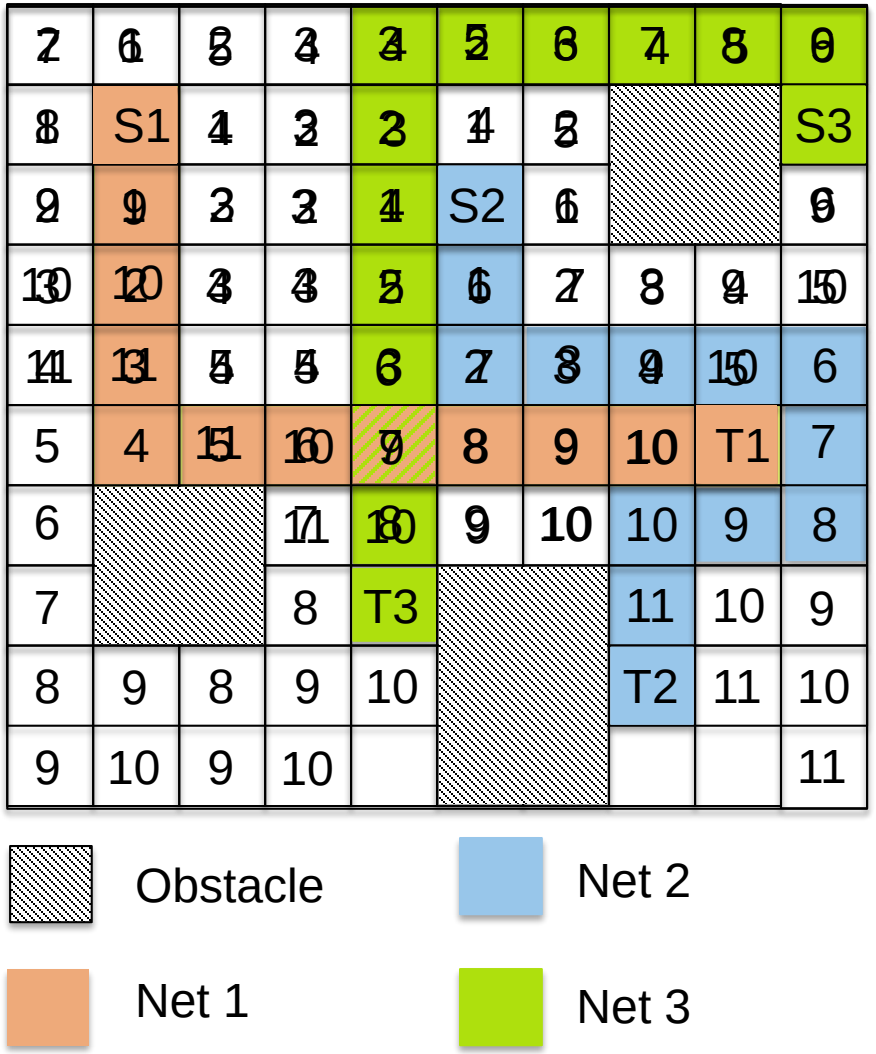
Move force $\mathbf{F}^{move,cross}$ attracts net modules to empty spaces

Routing

Maze router

- Easy to implement
- Fast

Modification for allowing but penalizing crossings



Experimental Results

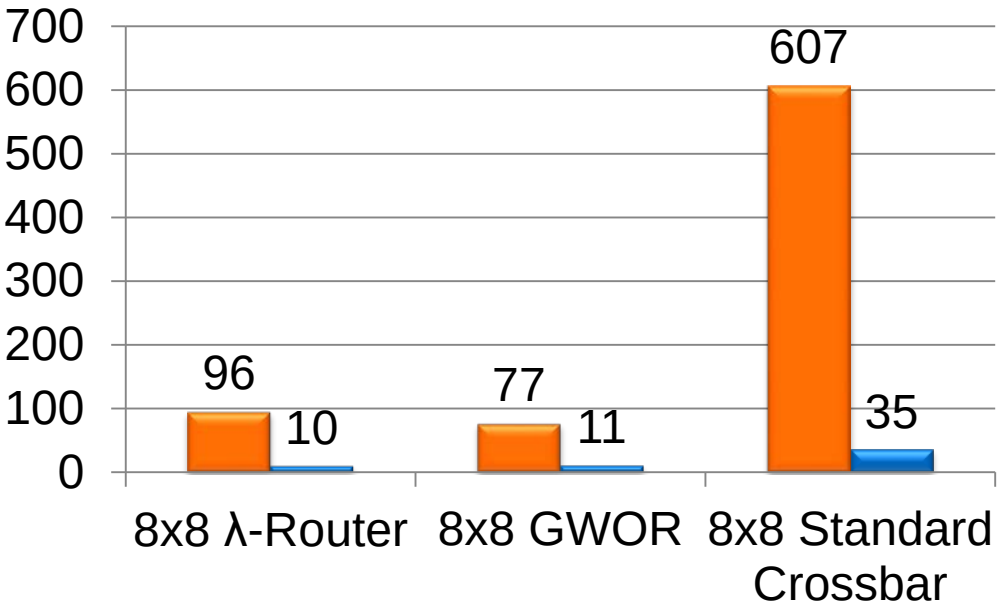
Intel Core 2 Quad CPU with 8GB RAM running at 2.33GHz

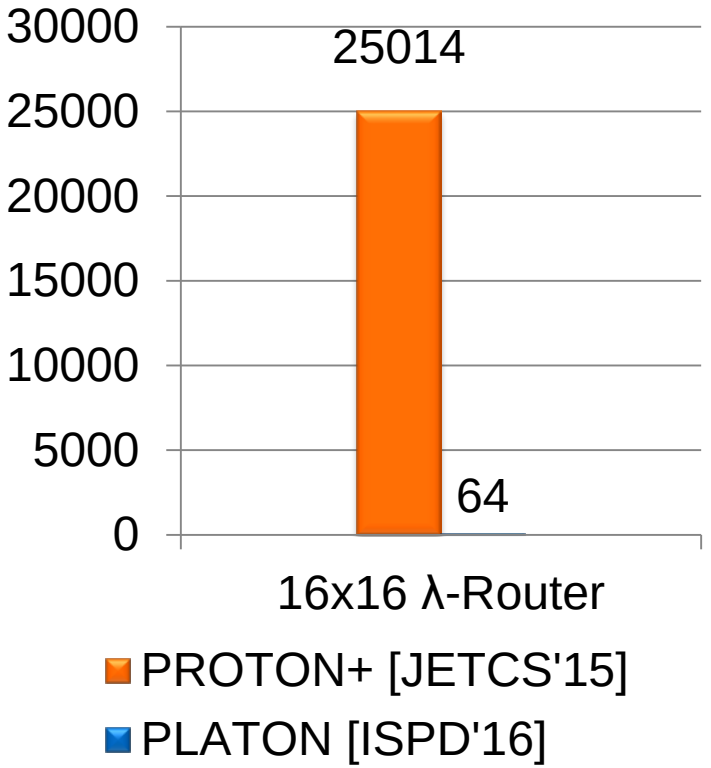
Loss parameters [Chan+ DATE‘10]	
propagation loss	1.5 dB/cm
crossing loss	0.15 dB per crossing
bending loss	0.005 dB per bend
drop loss	0.5 dB per drop

	Number of PSEs	Number of nets
8x8 λ-Router	28	64
8x8 GWOR	24	56
8x8 Standard Crossbar	64	111
16x16 λ-Router	120	256

Maximum Insertion Loss

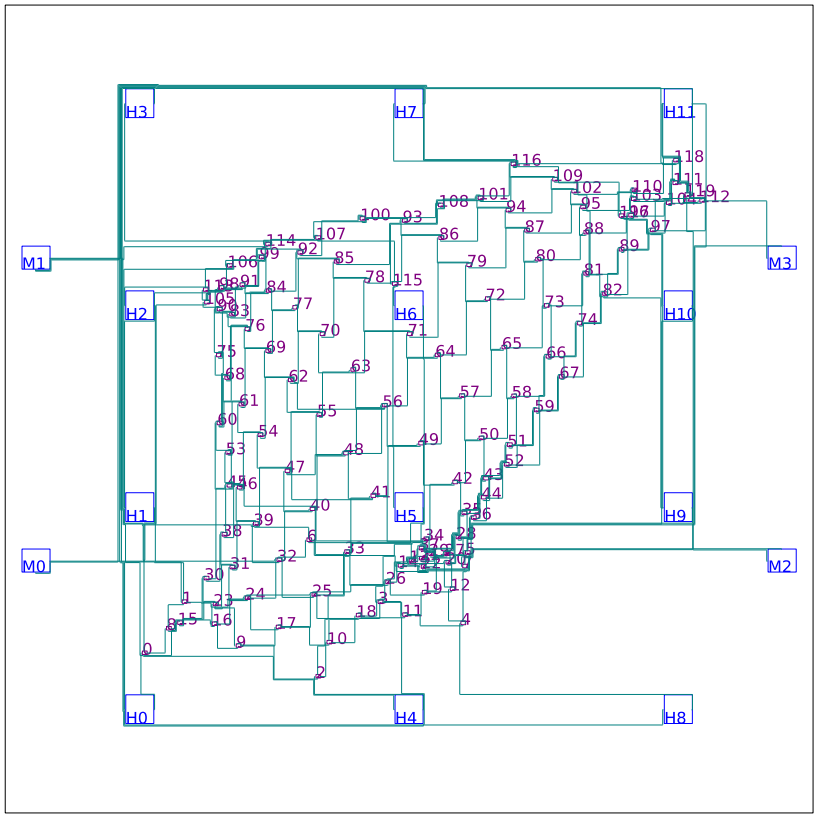
Runtime in Seconds





Resulting Layout of 16x16 λ-Router

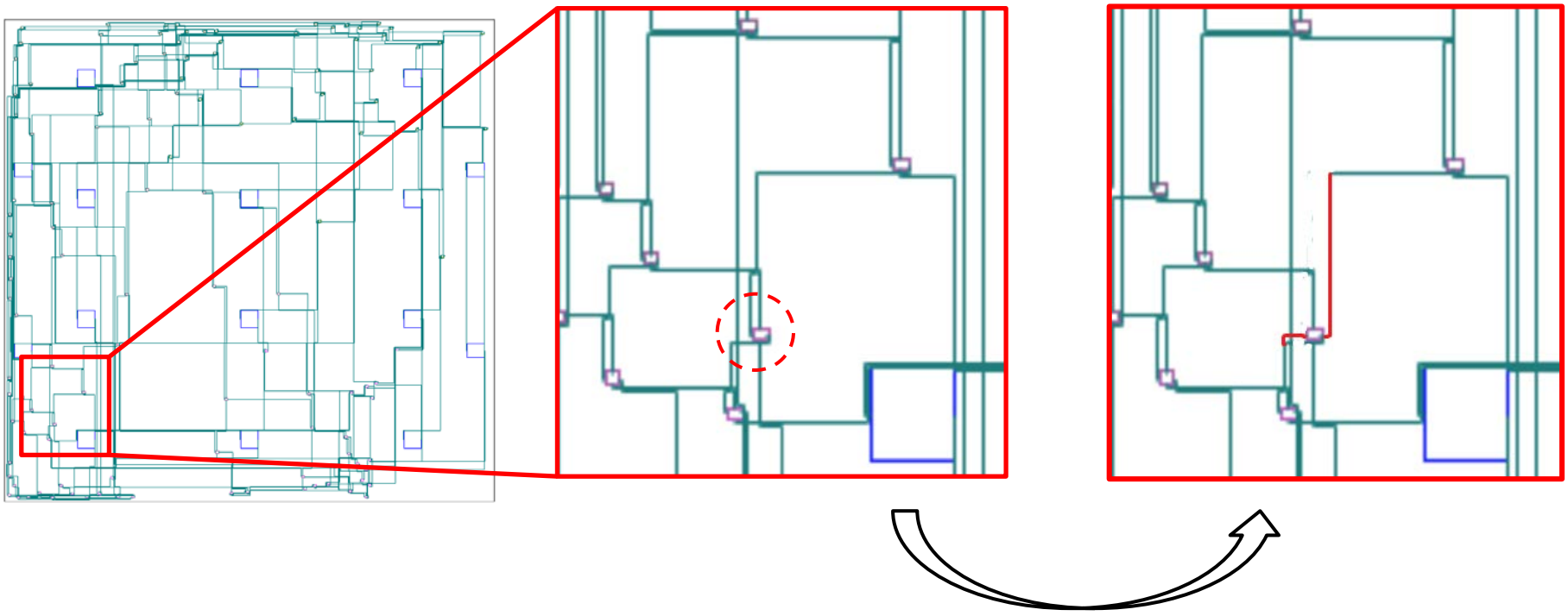
PROTON [ICCAD'13]



PLATON [ISPD'16]

Optimization Potential

Orientation of PSEs is fixed ➔ unnecessary crossings



Optimization Potential

- Orientation of PSEs is fixed ➔ many unnecessary crossings
- Placement and routing are sequentially performed, and thus #crossings can only be estimated during placement
- The non-linear and force-directed approaches require iterative optimization processes, leading to longer runtime

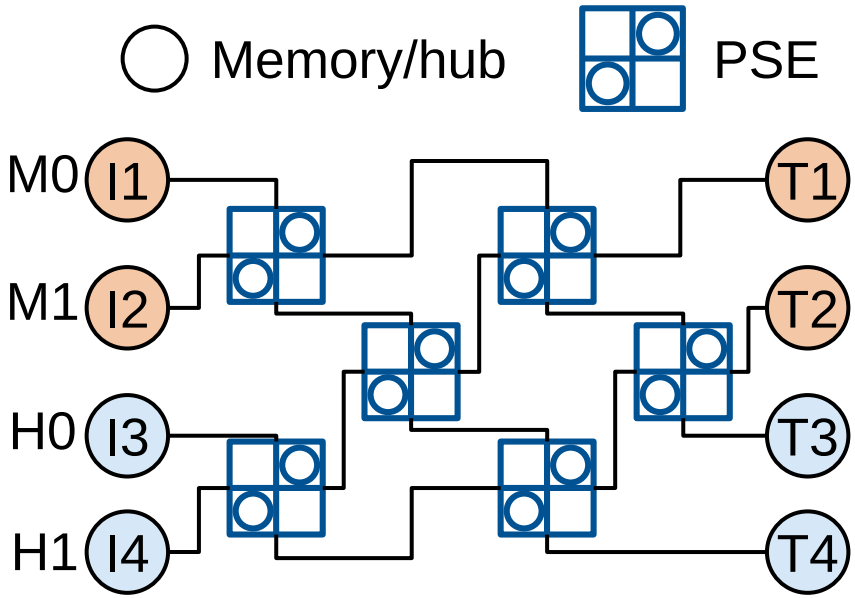
	PLATON				Manual layout				PROTON			
Topology	il_{max}	C	L	CPU	il_{max}	C	L	CPU	il_{max}	C	L	CPU
8x8 λ-Router	9.3	29	26865	9.8	17.5	64	49600	-	8.6	41	10413	95.8
8x8 GWOR	9.7	44	15651	10.7	21.4	72	67500	-	8.4	38	13014	77.1
8x8 Standard Crossbar	12.4	50	26478	35.2	-	-	-	-	8.5	36	15255	606.9
16x16 λ-Router	22.5	86	56912	64.3	-	-	-	-	44.0	255	28636	24425.8

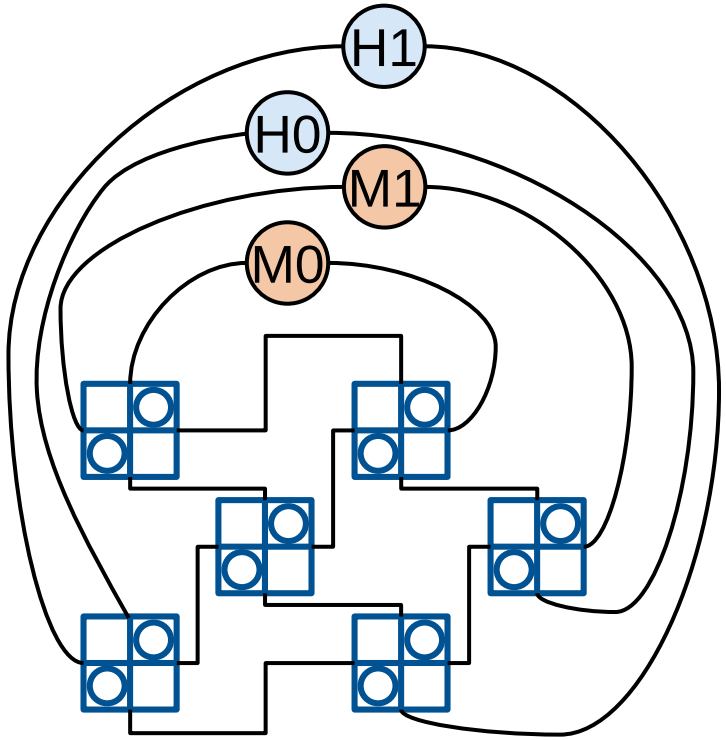
#Crossings on critical paths in logic schemes:
7 in 8x8 λ-router, 15 in 16x16 λ-router

Joint work with Shao-Yun Fang, NTUST: “PlanarONoC: Concurrent Placement and Routing Considering Crossing Minimization for ONoCs”, to appear DAC 2018

Observation and Question:

Logic schemes of λ-router: planar w/o constraint of fixed memory/hub positions



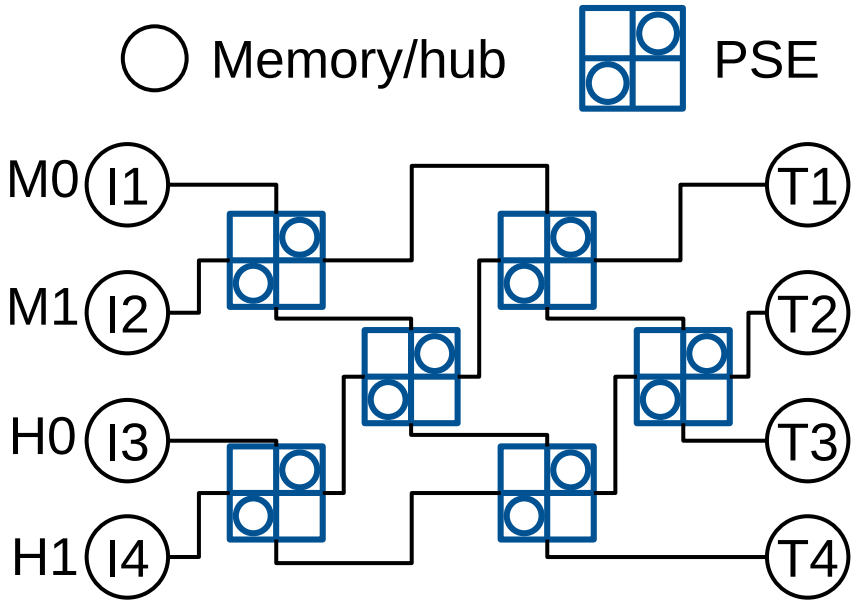


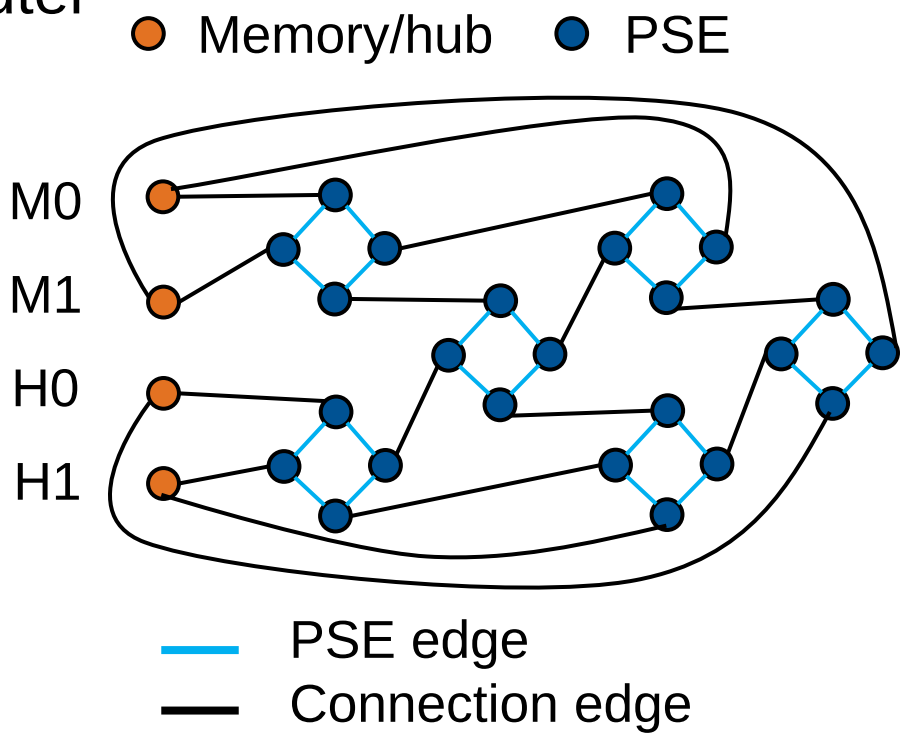
Is it possible to keep the planarity while satisfying the fixed position constraint?

Connection Graph Construction

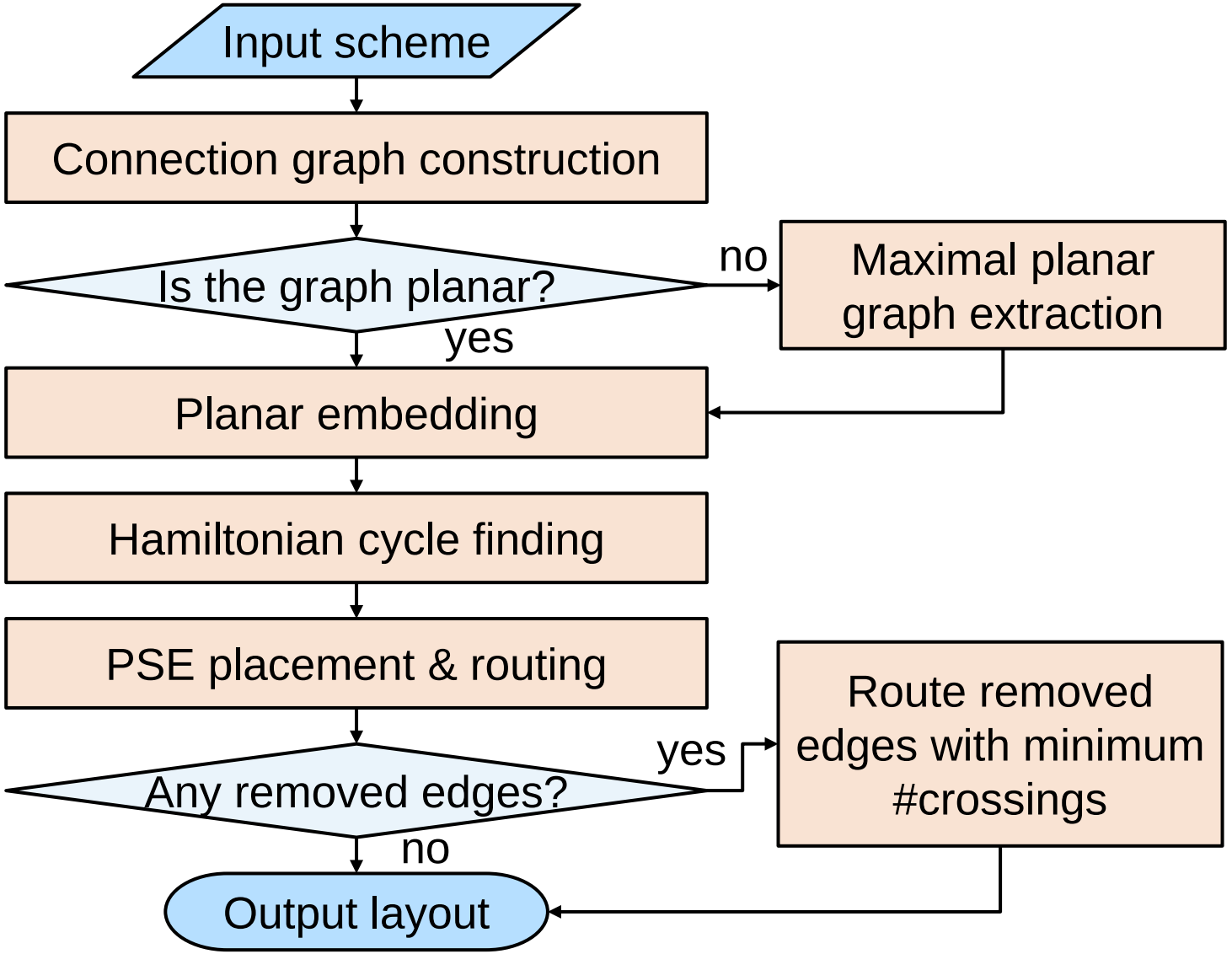
Use a 4-cycle to represent each PSE

An example of connection graph construction from the logic scheme of the 4x4 λ-router





Proposed Algorithm Flow



Results:

Topology	PROTON				PLATON				PlanarONoC			
	il_{max}	C	L	CPU (s)	il_{max}	C	L	CPU (s)	il_{max}	C	L	CPU(s)
8x8 λ	8.6	41	10413	95.8	9.3	29	26865	9.8	5.23	7	24140	0.3
8x8 GWOR	8.4	38	13014	77.1	9.7	44	15651	10.7	6.38	10	28620	0.1
8x8 Crossbar	8.5	36	15255	606.9	12.4	50	26478	35.2	7.35	13	32125	0.2
16x16 λ	44.0	255	28636	24425.8	22.5	86	56912	64.3	16.2	14	89589	0.5
Comp.	1.11	1.49	0.58	103.52	1.00	1.00	1.00	1.00	0.63	0.22	1.38	0.01

Challenges

- “Simultaneous” P&R considering crossings
- Considering Variations
- Temperature Sensitivity of PSEs
  ➔First ideas: Proton+-T (*): Hotspot modeling, reduction
- Extend EDA algorithms to architectures beyond GWOR, Lambda (e.g. ring architectures).

* [Fengxian Jiao et al.: “Thermal-Aware P&R for 3D ONoCs”, to appear ISCAS 2018]

Opportunities

- Comprehensive Synthesis Flow (Bertozzi, OPTICS 2017)
  - Routing Protocol Selection
  - Wavelength Resolution
  - Technology Mapping
  - Wavelength Assignment
  - Topology Connection
  - Device Parameter Selection
  - Physical Mapping Flow
  - Physical Design
- Architectural / Topology Design Space Exploration
- ML ??

References

- [Chan+ DATE‘10]: Chan, J., Hendry, G., Biberman, A., Bergman, K. (2010): PhoenixSim: A Simulator for Physical-Layer Analysis of Chip-Scale Photonic Interconnection Networks, DATE, pp. 691-696.
- [Condrat+ TCAD’14]: Condrat, C.; Kalla, P. & Blair, S. (2014): Crossing-Aware Channel Routing for Integrated Optics, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 33(6), pp. 814-825.
- [Ding+ DAC’09]: Ding, D.; Zhang, Y.; Huang, H.; Chen, R. T. & Pan, D. Z. (2009): O-Router: An Optical Routing Framework for Low Power On-chip Silicon Nano-Photonic Integration, Design Automation Conference, pp. 264-269.
- [Hendry+ DATE’11]: Hendry, G.; Chan, J.; Carloni, L. & Bergman, K. (2011): VANDAL: A Tool for the Design Specification of Nanophotonic Networks, Design, Automation and Test in Europe, pp. 1-6.
- [Minz+ TCPT’07]: Minz, J. R.; Thyagara, S. & Lim, S. K. (2007): Optical Routing for 3D System-on-Package, IEEE Transactions on Components and Packaging Technologies 30(4), pp. 805-812.
- [Ramini+ NOCS‘12]: Ramini, L.; Bertozzi, D. & Carloni, L. (2012): Engineering a Bandwidth-Scalable Optical Layer for a 3D Multi-core Processor with Awareness of Layout Constraints, IEEE/ACM NOCS, pp. 185-192.
- [Scandurra+ NoCArc’08]: Scandurra, A. & O'Connor, I. (2008): Scalable CMOS-Compatible Photonic Routing Topologies for Versatile Networks on Chip, Network on Chip Architecture.
- [Seo+ ISQED’05]: Seo, C.-S.; Chatterjee, A. & Jokerst, N. M. (2005): Physical Design of Optoelectronic System-on-a-Package: a CAD Tool and Algorithms, International Symposium on Quality of Electronic Design, pp. 567-572.
- [JETCS‘15]: von Beuningen, A.; Ramini, L.; Bertozzi, D. & Schlichtmann, U. (2015): PROTON+: A Placement and Routing Tool for 3D Optical Networks-on-Chip with a Single Optical Layer, ACM Journal for Emerging Technologies in Computing Systems 12(4), pp. 44:1-44:28.
- [ISPD‘16]: von Beuningen, A. & Schlichtmann, U. (2016): PLATON: A Force-Directed Placement Algorithm for 3D Optical Networks-on-Chip, ACM International Symposium on Physical Design, pp. 27-34.