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PEACLAB

A System-Level Perspective on Silicon Photonic Network-on-Chips

Workshop on Optical/Photonic Interconnects for Computing Systems, 2019

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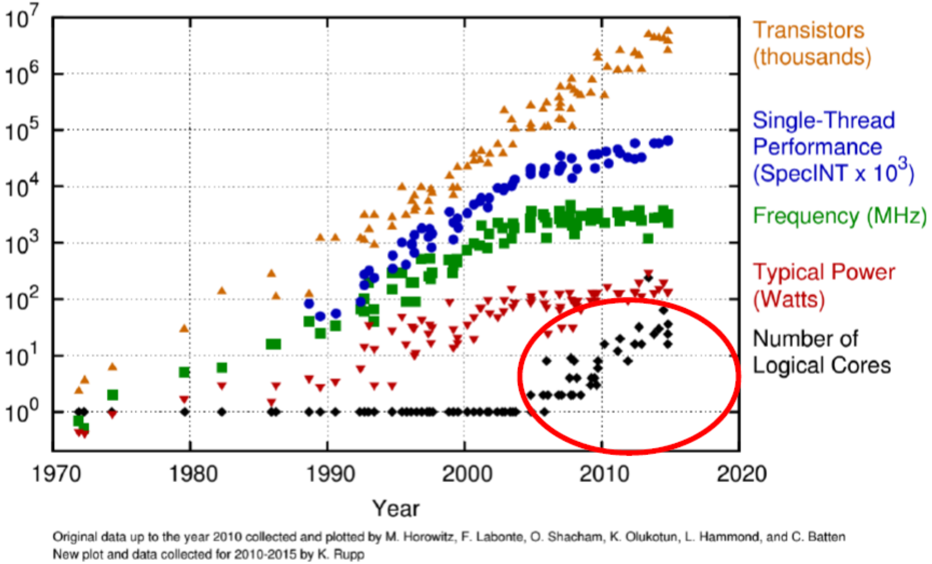
On-chip communication challenges in manycore systems

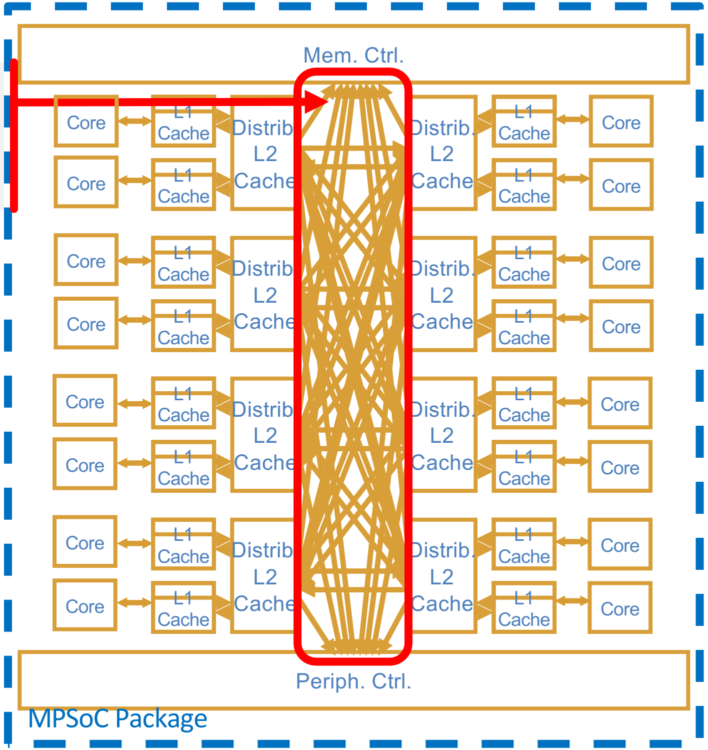
Due to technology scaling & higher computation needs, more resources are integrated on-chip

Communication Bottleneck

BW need increases with #cores



[Rupp, 40 years of microprocessor trend data, 2015]



Photonic Network-on-chips (PNoCs)

Benefits with PNoCs

- Wavelength-division multiplexing
  → Higher bandwidth
- Lower data-dependent energy consumption
  → 0.42pJ/bit for modulation, 0.18pJ/bit for drivers [Zheng *et al*. Optics Express'11]
- Lower latencies with silicon waveguides
  → Data rate density of 320Gbps/μm [Batten *et al*. Micro'09]

Challenges in PNoCs

- High sensitivity to thermal and process variations
  → Higher thermal tuning power
- High PNoC power with more laser wavelengths
- Higher optical loss and lower laser efficiency
  → Increased laser source power

System-level optimizations enable efficient PNoC integration

Energy-efficient computing with PNoCs

System-level optimization by cross-layer modeling of device, design and architecture parameters

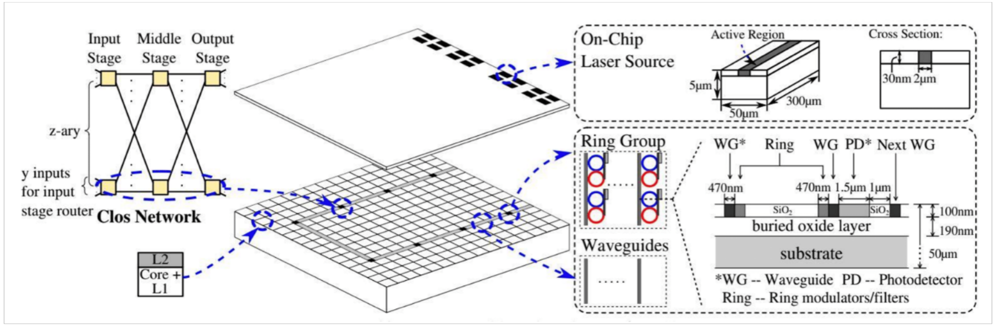
Design optimization
- Laser sharing and placement — **NOCS'14**
- PNoC layout on a chip — **DATE'16**
- Cross-layer optimization of NoCs in 2.5D systems — **DATE'18, ICCAD'18**

Workload allocation
- **RingAware** → Thread allocation to minimize thermal effects — **DATE'14**
- **FreqAlign** → Thread allocation and migration to minimize thermal and process effects — **TCAD'17**

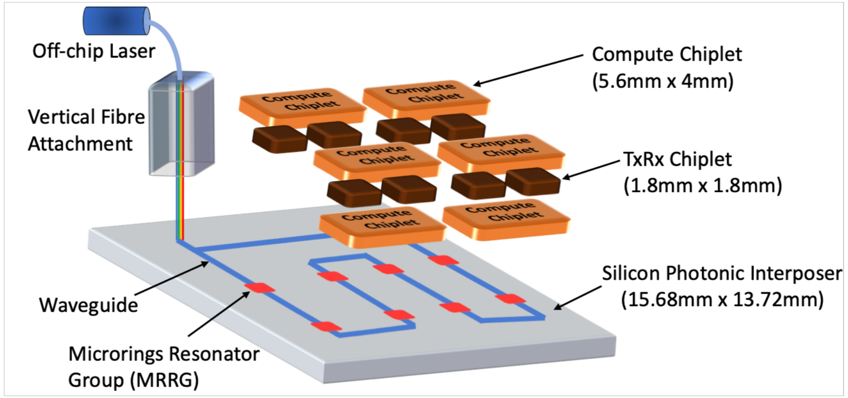
Wavelength selection
- **WAVES** → Activation of minimal laser wavelengths to reduce PNoC power — **DATE'19**

Manycore systems with PNoCs

Monolithic-integrated PNoC



2.5D-integrated PNoC



Outline

Design optimization

Floorplan optimization for PNoCs [DATE'16]

Workload allocation

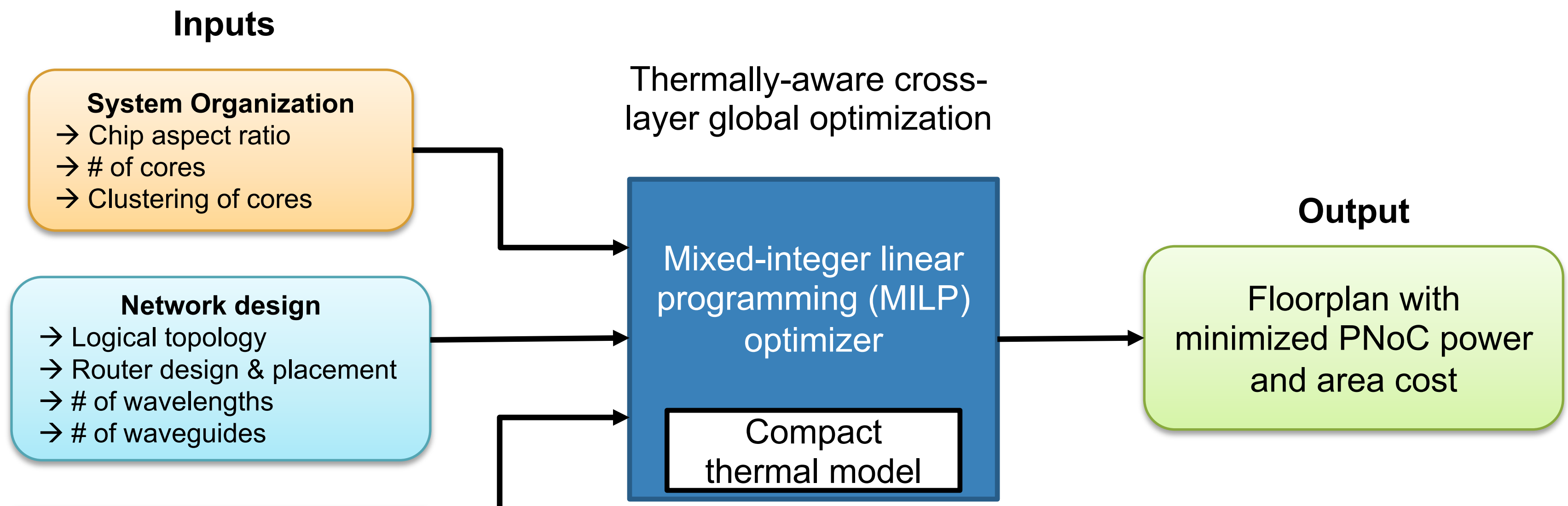
FreqAlign- Thread allocation and migration [TCAD'17]

Wavelength selection

WAVES- Minimal laser wavelength selection [DATE'19]

Floorplan optimization for PNoCs

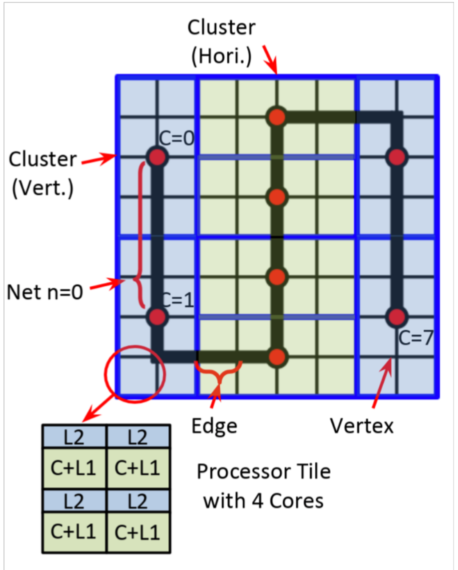
PNoC floorplan optimization flow that is aware of on-chip thermal variations based on various power profiles



Minimize: $\alpha \cdot P_{PNoC} + \beta \cdot AREA_{PNoC}$

$$P_{PNoC} = P_{laser} + P_{tuning} + P_{electrical}$$

Floorplan optimization formulation



- System is formed by tiles
- PNoC is represented by
  - → clusters of tiles
  - → location of router groups
  - → the waveguides

Minimize: $\alpha \cdot P_{PNoC} + \beta \cdot AREA_{PNoC}$

Subject to:

Router group related constraints

$$\sum_{r\in R, q\in Q, f\in\{0,1\}} \gamma^c_{frq} = 1, \qquad \forall c \in C, \quad \gamma^c_{frq} \in \{0,1\}$$

$$r_c = \sum_{r\in R, q\in Q, f\in 0,1} r \cdot \gamma^c_{frq}, \quad q_c = \sum_{r\in R, q\in Q, f\in 0,1} q \cdot \gamma^c_{frq}, \quad \forall c \in C$$

$$f_c = \sum_{r\in R, q\in Q, f\in 0,1} f \cdot \gamma^c_{frq}, \quad \forall c \in C$$

Tile and cluster related constraints

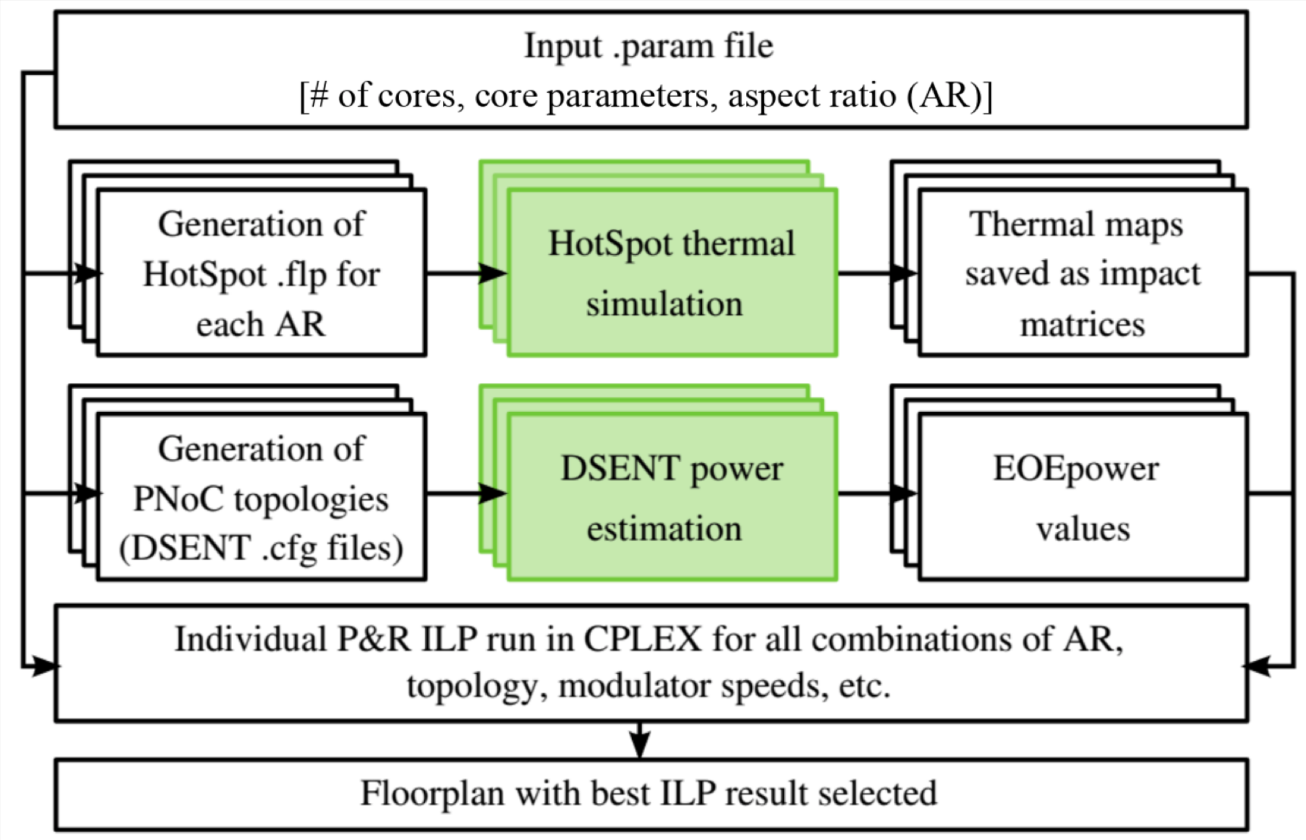
$$o_{crq} = \sum_{r'\in R, q'\in Q, f\in 0,1} o_{fr'q'}(r,q)\gamma^c_{fr'q'}, \quad \forall c \in C$$

$$\sum_{c\in C} o_{crq} \le 1, \qquad \forall q \in Q, r \in R$$

Path related constraints

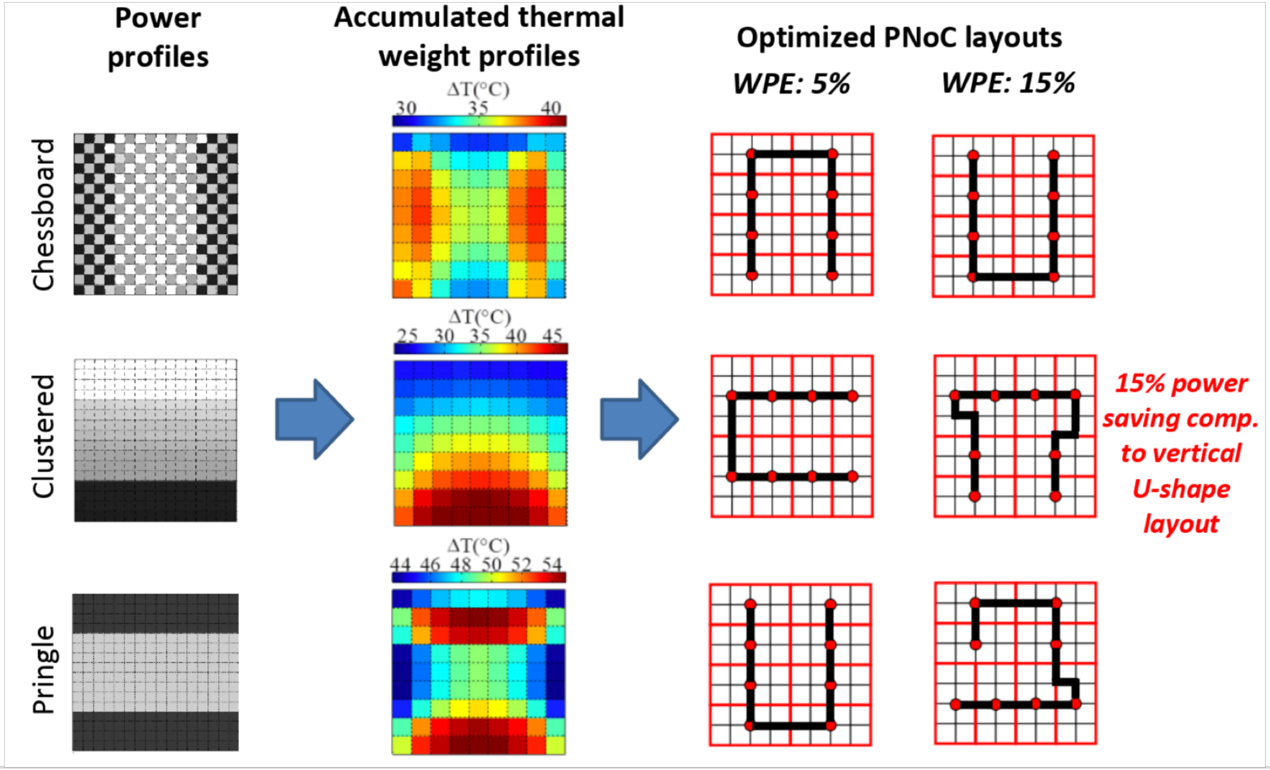
$$2v^n_{rq} - e^n_{hrq-1} - e^n_{vr-1q} - e^n_{hrq} - e^n_{vrq} - \sum_{f\in 0,1} \gamma^{s_n}_{frq} - \sum_{f\in 0,1} \gamma^{t_n}_{frq} = 0,$$
$$\forall n \in N, r \in R, q \in Q$$

Optimization flow



Cross-layer PNoC PnR optimization

Optimized PNoC layouts for different power profiles and laser wall-plug efficiency



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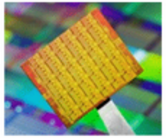
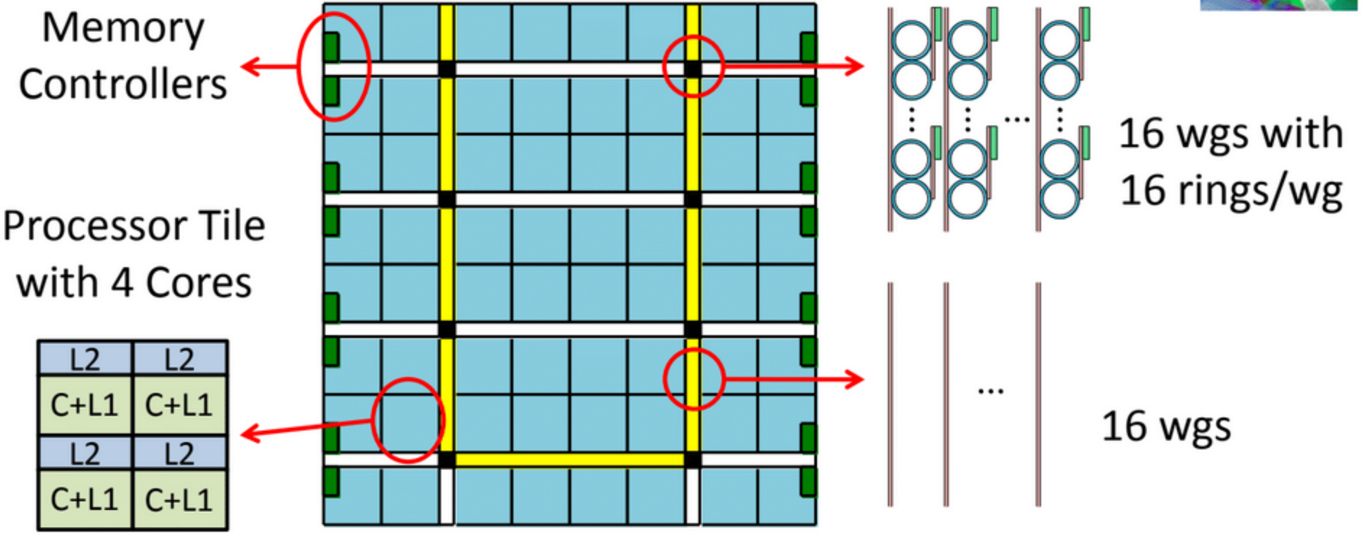
WAVES- Minimal laser wavelength selection [DATE'19]

Target manycore system

- 256-core system with Clos network

Core Architecture: IA-32 core in Intel SCC [*Howard,ISSCC2011*], 16KB I/D L1 cache & 256KB L2 cache; Average power consumption: 1.166W

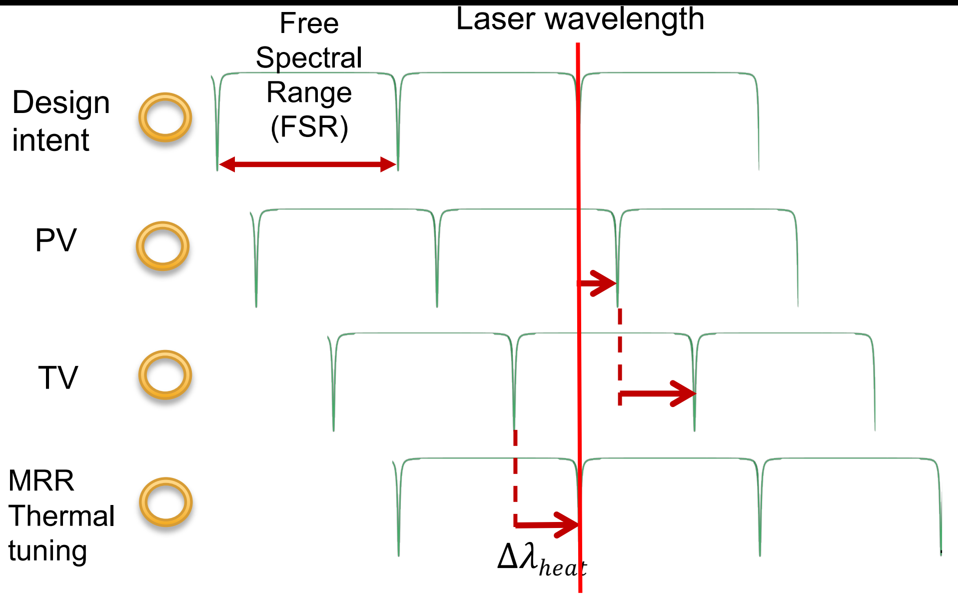




Workload allocation to mitigate MRR resonance shifts

- The resonant frequency shifts because of process variations (PV) i.e., device variability, geometric aberrations

- The resonant frequency shifts because of temperature variations (TV)



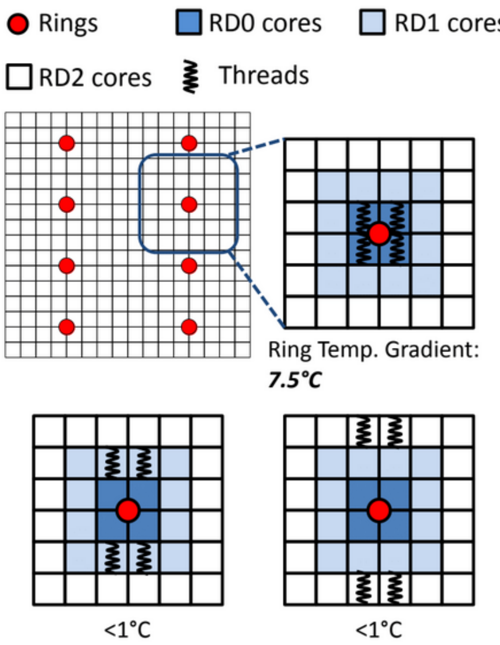
System-level goal

- Minimize the difference among MRR temperatures
- Reduce the overall chip temperature
- Minimize the impact of process variations on MRR resonance shift
- On-chip laser sources' optical frequencies also need to match with corresponding MRR's resonant frequency

Runtime thermal management policies

TCAD'17

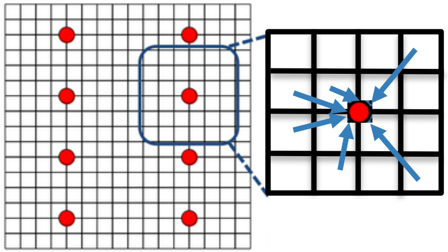
RingAware



Classify cores based on their distance to a ring group

Effectively reduces the RG temperature gradient, which results in a low resonant frequency gradient

FreqAlign



- Create an *M x N* weight matrix
  - Steady state temperature impact per unit of power of core *j* on RG *i*
  - Update the weight matrix with impact of process variations

Frequency tuning techniques

Target frequency tuning (TFT)

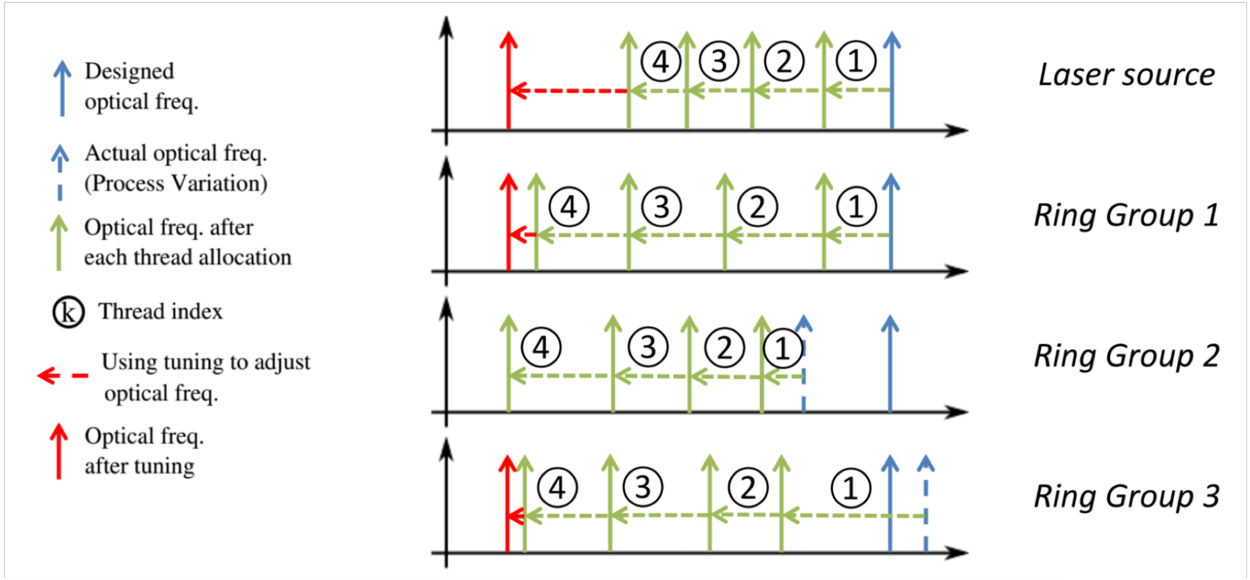
All RGs and laser sources are first tuned to their optical frequencies at the temperature threshold of the target manycore system (90°C)

Limitations
All RGs and lasers have to be tuned

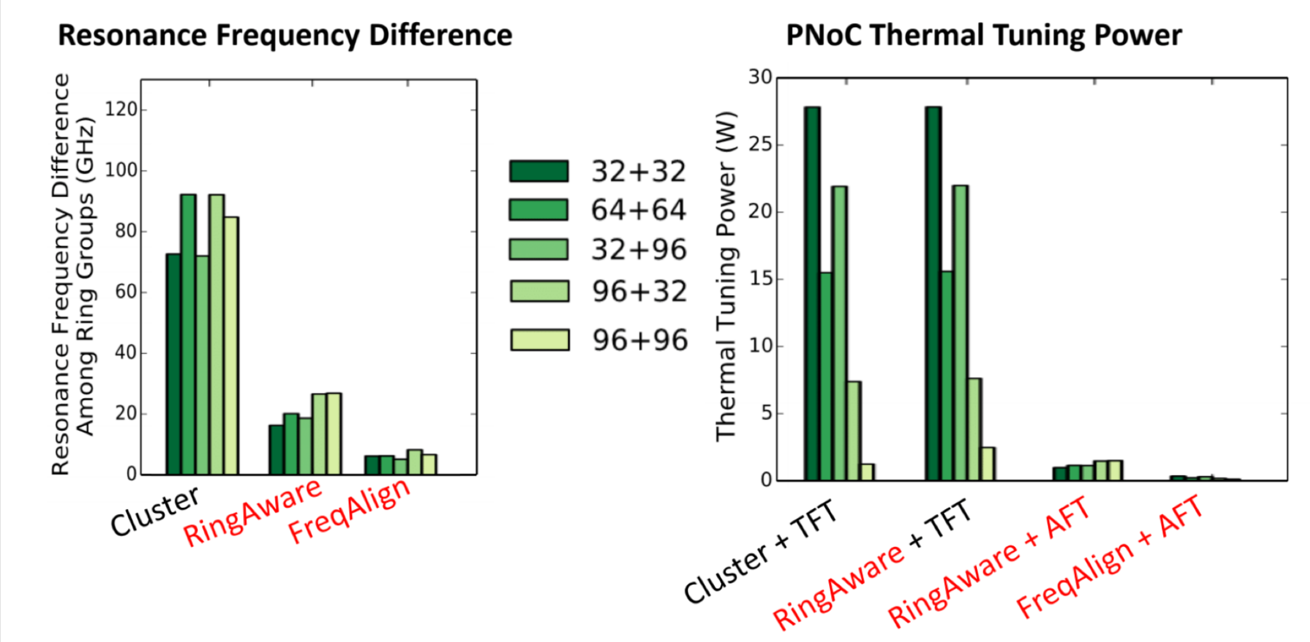
System underutilized
Lower average temperatures
Tuning power increases

Adaptive frequency tuning (AFT)

Set the lowest frequency among the RGs as the target frequency and tune all the other devices to this target frequency
→ Target frequency is adaptive



Experimental results



- Compared to *RingAware*, *FreqAlign* reduces the resonant frequency difference by **60.6%** on average
- Compared to *RingAware+ TFT*, *FreqAlign+ AFT* reduces the tuning power by **14.93W** on average

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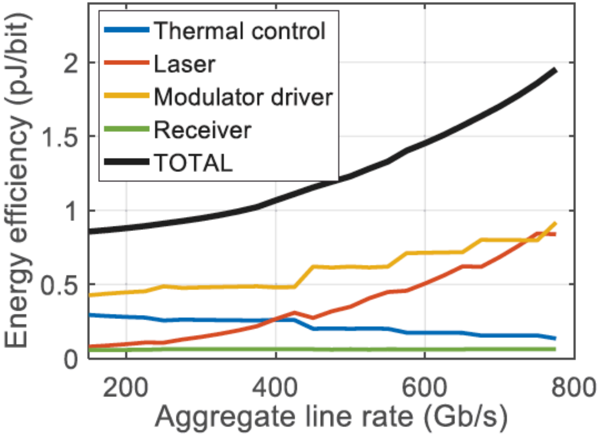
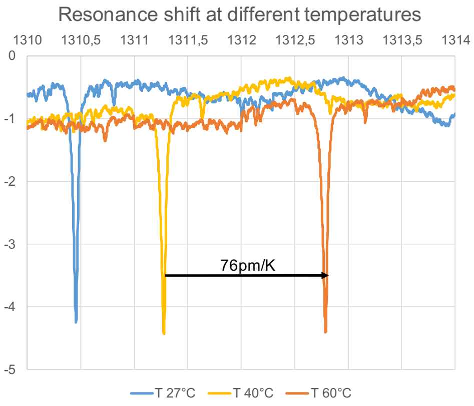
WAVES- Minimal laser wavelength selection [DATE'19]

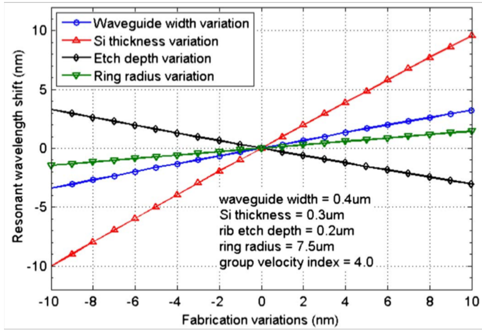
Challenges in designing energy-efficient PNoCs

- ➢ Increased PNoC power for higher aggregate PNoC bandwidth
  → 1.5pJ per bit for 600Gbps line rate [Bahadori *et al.* DATE'17]

- ➢ High sensitivity of optical devices to thermal variations (TV) and process variations (PV)



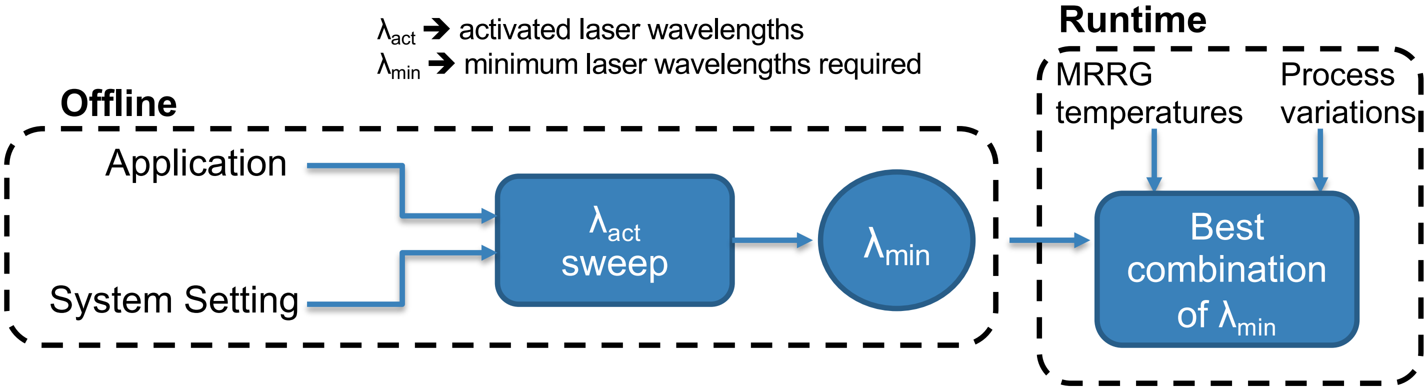




PNoC power increases with the increasing laser wavelengths in the system

The resonant wavelength of MRRs shifts due to TV and PV

Wavelength selection (WAVES)

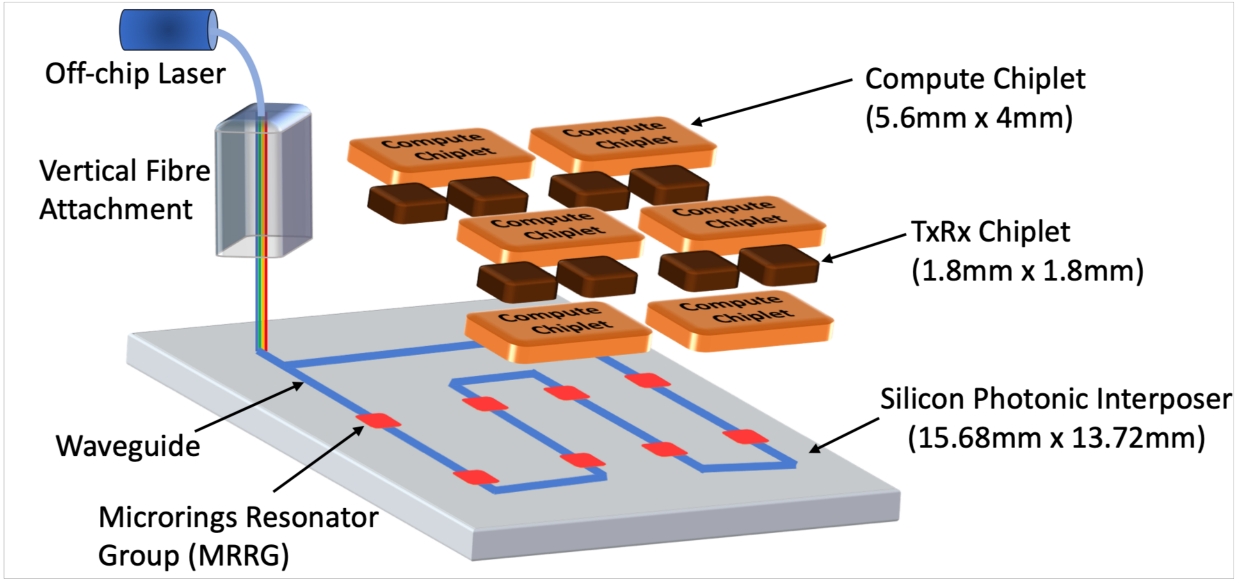


\+ Minimal Storage (200KB)
\+ Low latency (~5ns)

- Identify λ_{min} for an application to provide minimal performance loss
  → Set performance loss threshold (L_{thr})
- Activate best combination of λ_{min} accounting for the on-chip TV and PV
- Cross-layer simulation framework to model the system performance and PNoC power
  → Explore device-level MRR locking under different system-level constraints

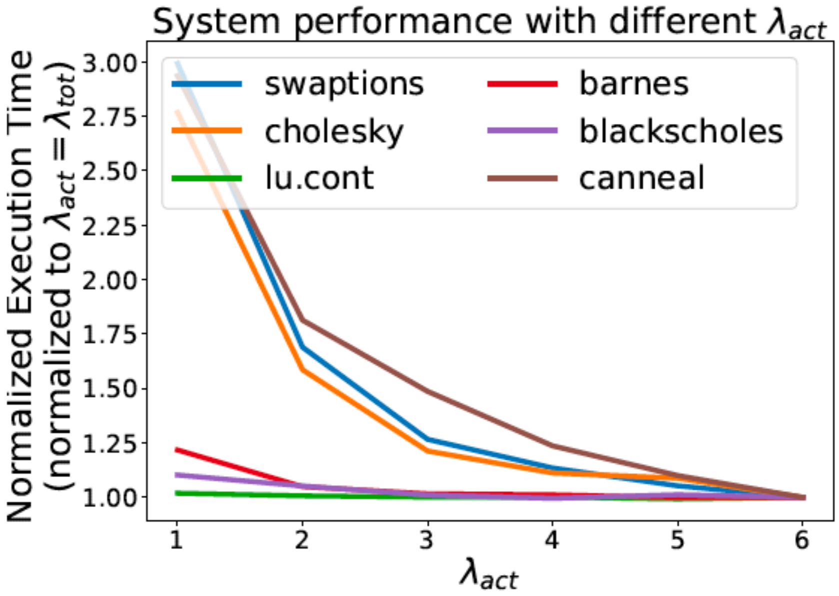
POPSTAR: 2.5D manycore system with PNoCs

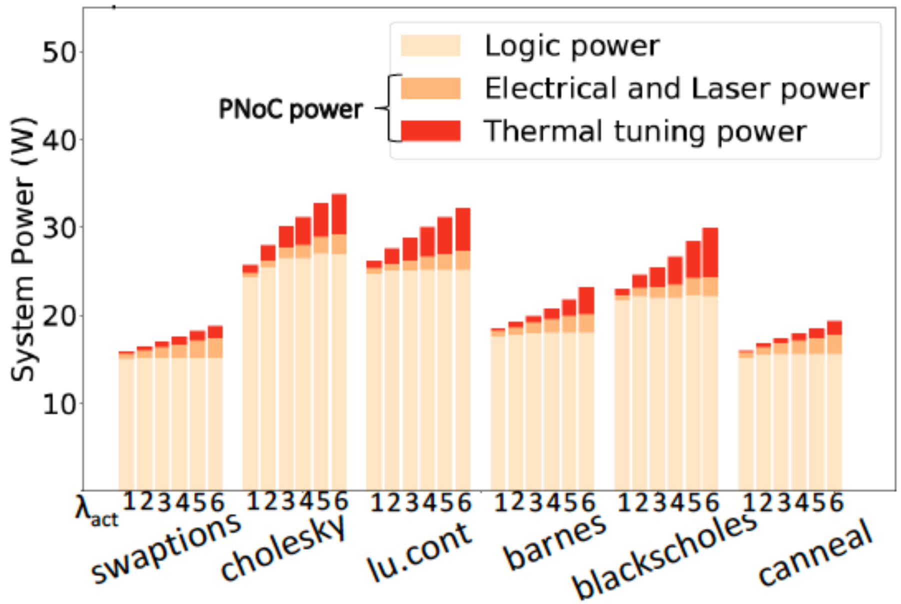
POPSTAR → Processors On Photonic Silicon inTerposer ARchitecture



- 96-core 2.5D manycore system
- Off-chip laser emits up to 6 wavelengths
  → Data rate of 12Gbps
  → Peak aggregate bandwidth of 576Gbps

PNoC power-bandwidth tradeoff

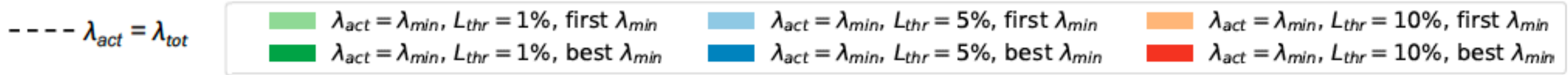




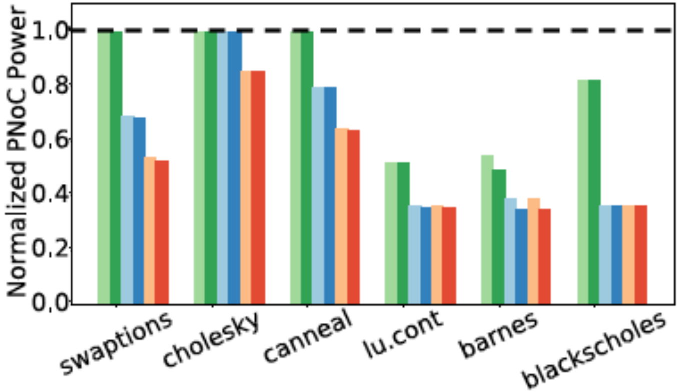
- PNoC power increases with number of activated laser wavelengths (λ_{act})
- System performance saturates at a $\lambda_{min} < \lambda_{tot}$, which is dependent on application's bandwidth requirement

Experimental results

DATE’19



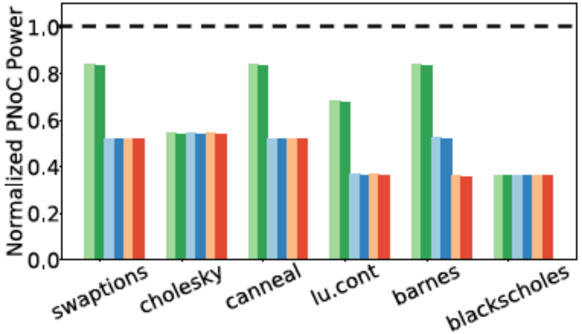
48 threads
50% utilization

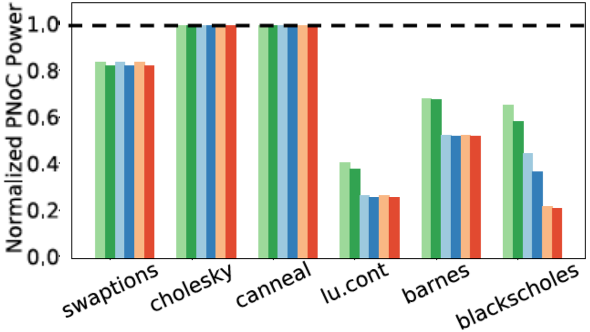


***23%** PNoC power savings with only **1%** loss in performance*

***38%** PNoC power savings with only **5%** loss in performance*

24 threads
25% utilization



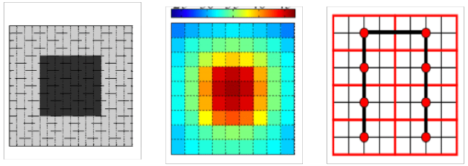


96 threads
100% utilization

System-level optimization → **essential** for PNoCs

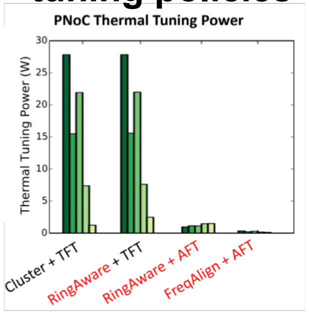
Our work aims at ***reducing the PNoC power (thermal tuning, EOE and laser source power)*** via workload allocation, thermal tuning policies, wavelength selection and design-time techniques.

Design time techniques

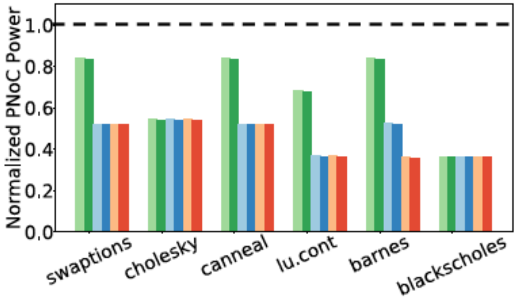


PNoC power and area optimized layout for a given design inputs

Workload allocation and tuning policies



Wavelength selection



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