OPTICS 2019

Optical/Photonic Interconnects for Computing Systems

Panel:

Bringing On-Chip Optical Interconnects into the Real World

Vladimir Stojanovic, *UC Berkeley*
Yvain Thonnart, *CEA LETI*
Bert Offrein, *IBM Zurich*
Laurent Vivien, *C2N*
Ian O'Connor, *ECL*

Moderator: Davide Bertozzi

How would I start a talk on optical networks-on-chip today?

Moore's Law of Optical Links

Photonics-to-electronics integration for optical interconnects in the early 21st century

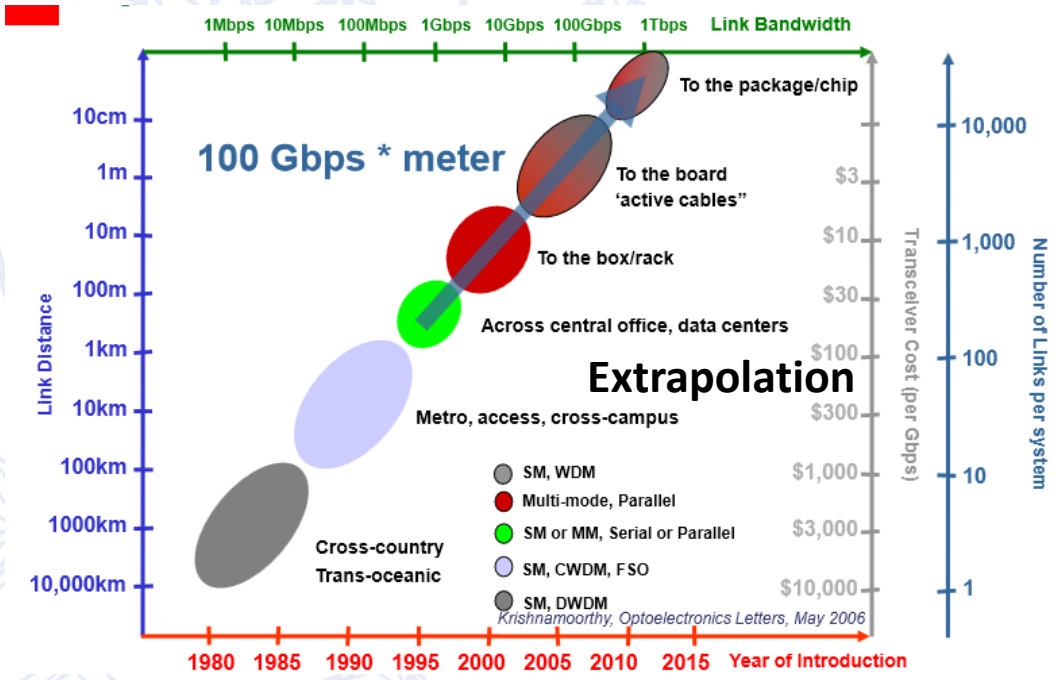
Ashok V. Krishnamoorthy*
Sun Microsystems SSG/Physical Sciences Center, 9515 Towne Center Dr., San Diego, CA, 92121, USA

(Received 2 March 2006)

We discuss the technical rationale, challenges, and potential for achieving "optics-to-the chip" via the intimate integration of photonics components such as lasers, detectors, and modulators with VLSI electronics. We review the progress made towards commercializing this technology for high-density optical transceivers and switching products.

CLC number: TN256 **Document code**: A **Article ID**: 1673-1905(2006)03-0163-06

One order of magnitude deeper penetration into the communication hierarchy every 5 years.



History of penetration of optical data link into communication

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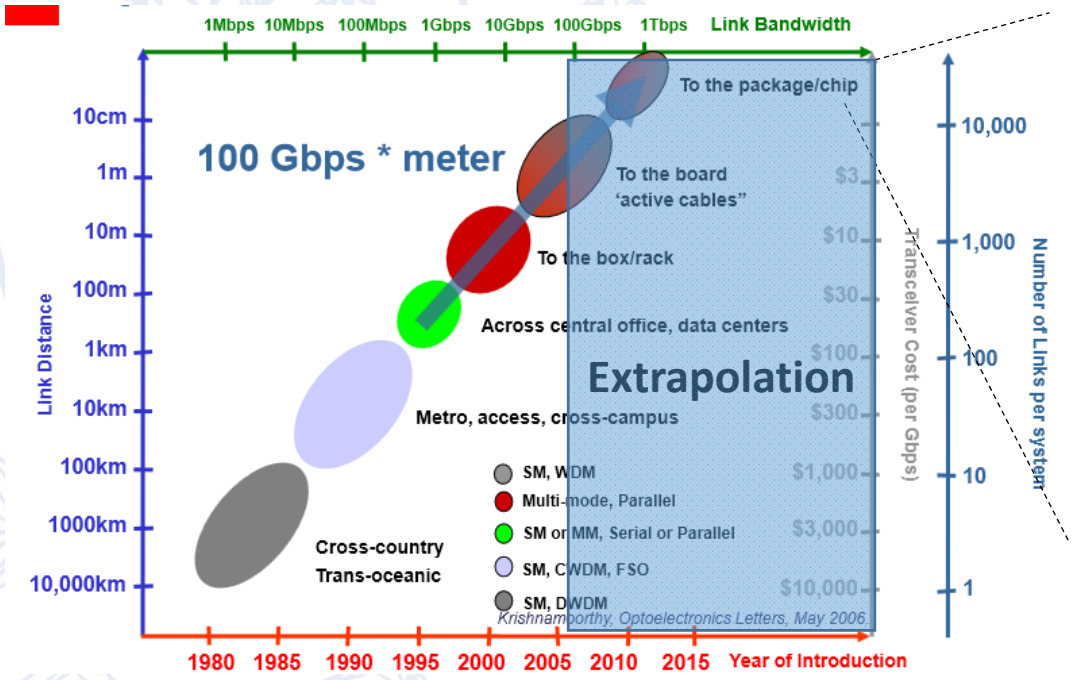

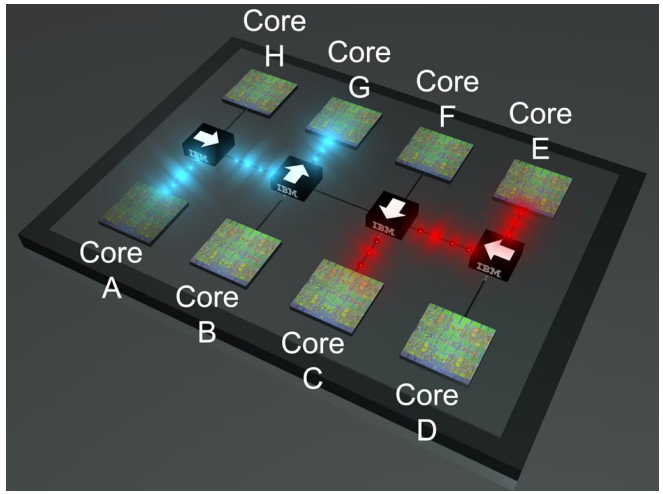

Source: IBM

If extrapolation were true, Optical NoCs would be currently mainstream!

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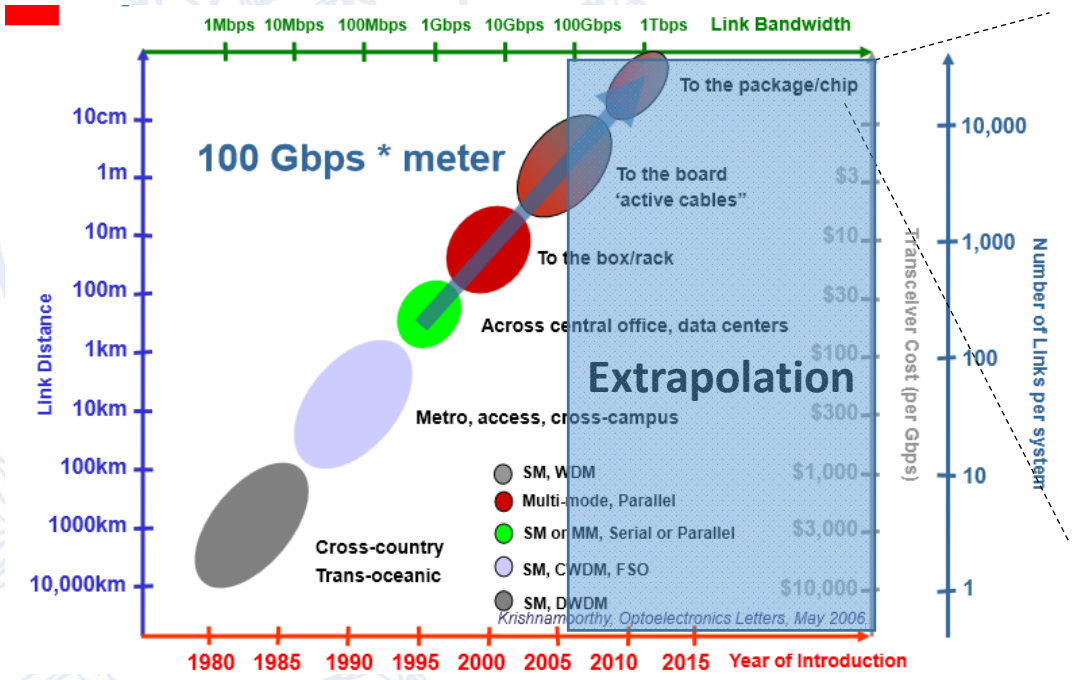
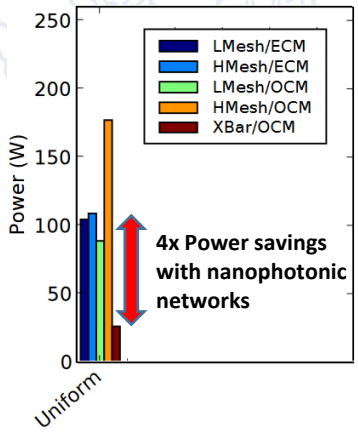
But this is the reality

(apart from papers)

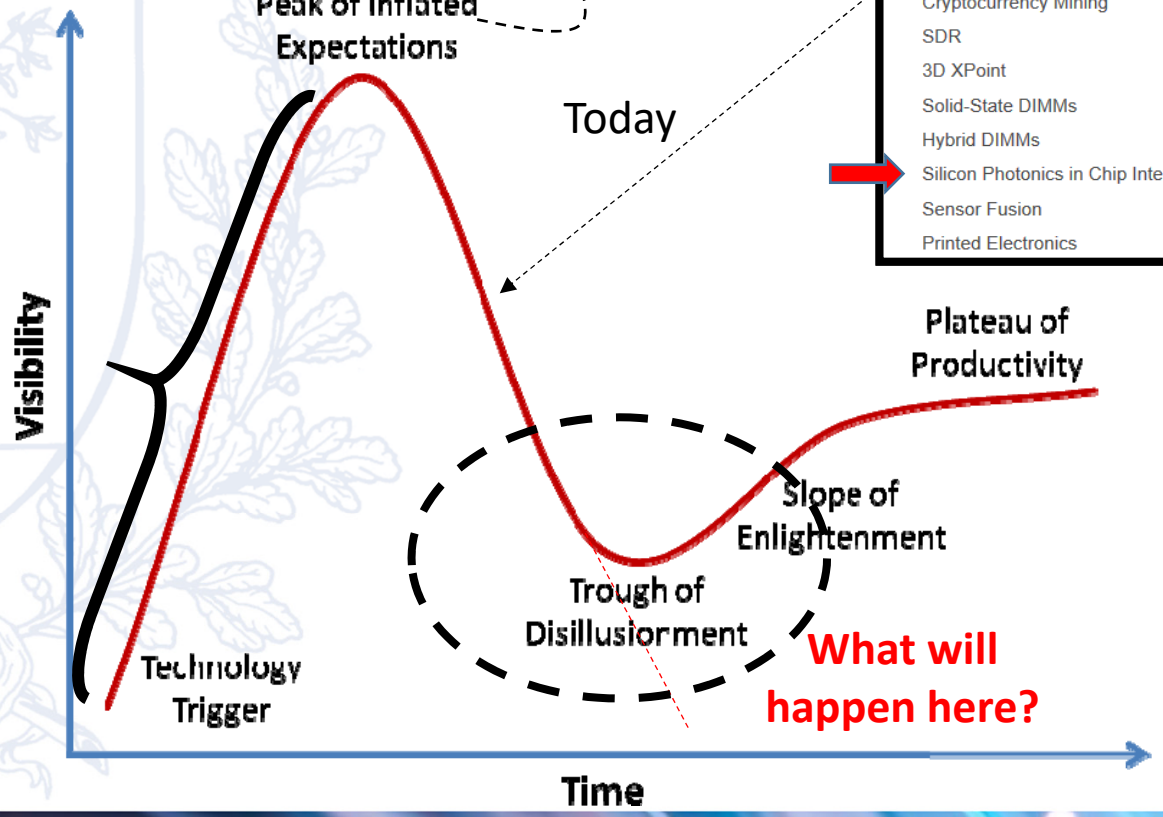


History of penetration of optical data link into communication

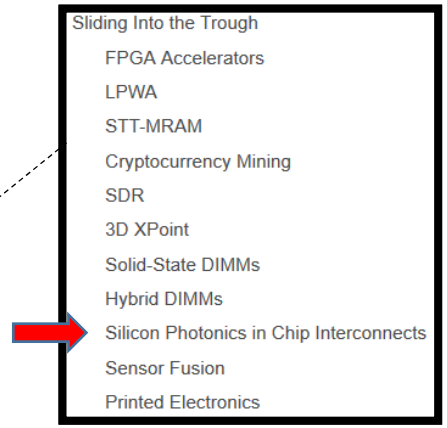
Hype Cycle



Photonic Device Parameter	Value
Optical fiber loss	0.5e-5 dB/cm
Coupler loss	0.5–1 dB
Splitter loss	0.2 dB
Non-linearity loss at 30 mW	1 dB
Modulator insertion loss	1 dB
Waveguide loss	2–4 dB/cm
Waveguide crossing loss	0.05 dB
Filter through loss	1e-4–1e-3 dB
Filter drop loss	1 dB
Photodetector loss	1 dB
Laser efficiency	30–50%
Receiver sensitivity	-20 dBm



Golden age of architecture exploration (2007-2014)



Hype Cycle for Semiconductors and Electronics Technologies, 2018 - Gartner

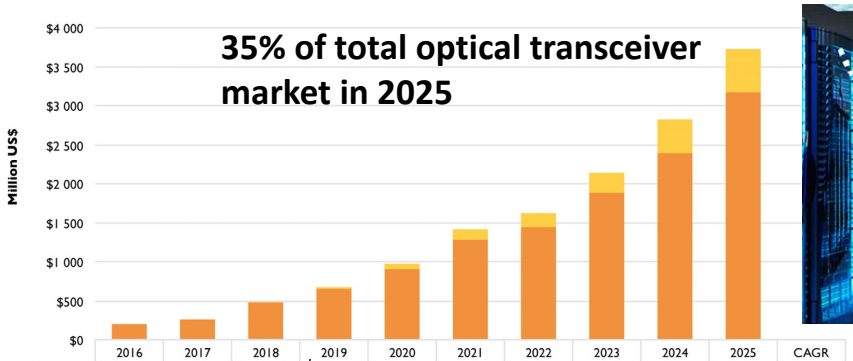
At least there is a hope, and a task for the research community as well!

Silicon Photonic Transceivers have survived the trough of disillusionment, and are now in high demand on the market!

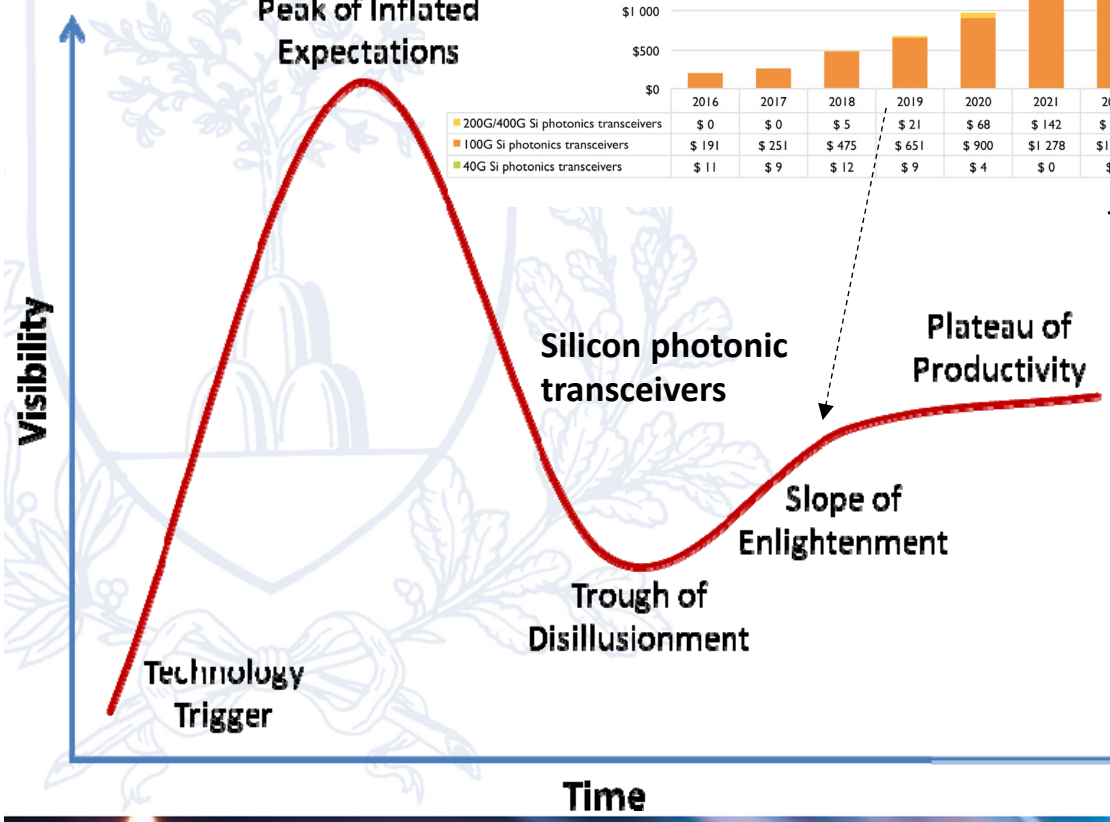
Hype Cycle

Silicon photonics transceivers market forecast

(Source: Silicon Photonics 2018 report, Yole Développement, January 2018)



	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	CAGR
200G/400G Si photonics transceivers	$ 0	$ 0	$ 5	$ 21	$ 68	$ 142	$ 179	$ 257	$ 424	$ 559	95,9%
100G Si photonics transceivers	$ 191	$ 251	$ 475	$ 651	$ 900	$1 278	$1 448	$1 884	$2 401	$3 169	37,3%
40G Si photonics transceivers	$ 11	$ 9	$ 12	$ 9	$ 4	$ 0	$ 0	$ 0	$ 0	$ 0	<1%



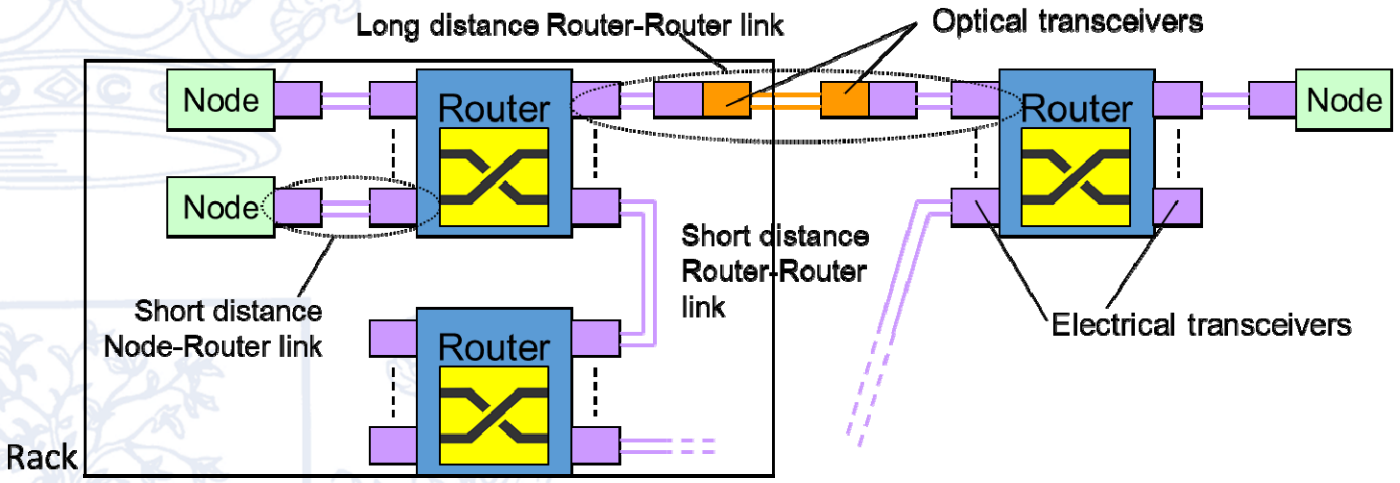
The proof: there are concrete target metrics!

<<The next evolution is to develop a 400G optical port over a single fibre across 500m at less than $1 per gigabit and with power <5mW/Gb>>

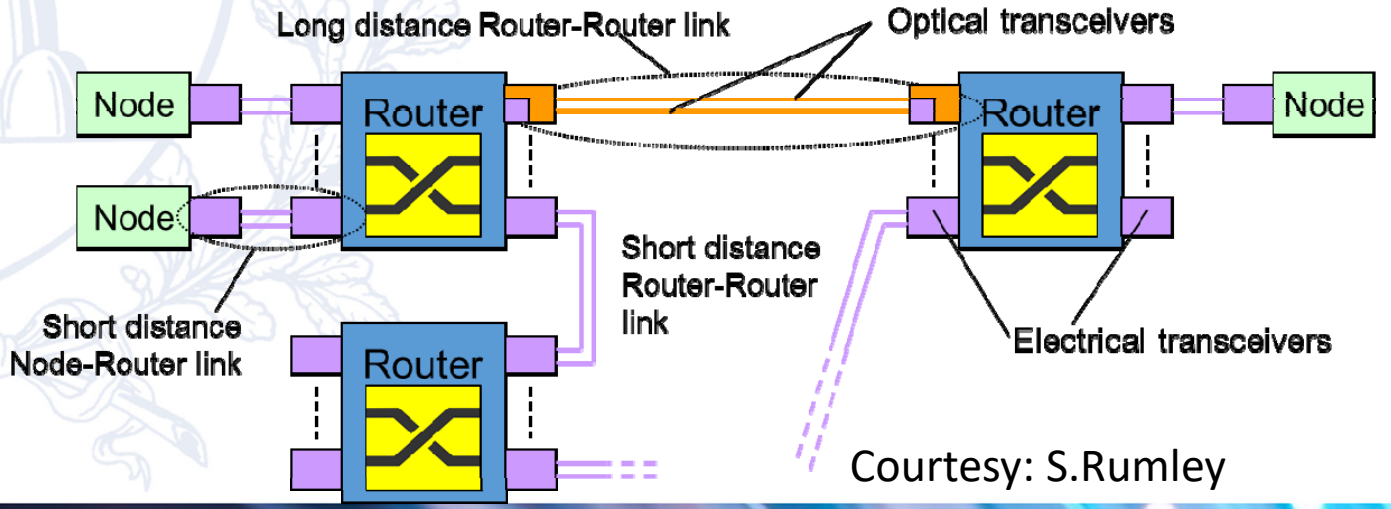
<<Silicon photonics is at the maturity level of the electronics industry in the 1980s and there are still challenges to overcome>>

(Yole Developpement, 2018)

Where Silicon Photonic Links Are Now



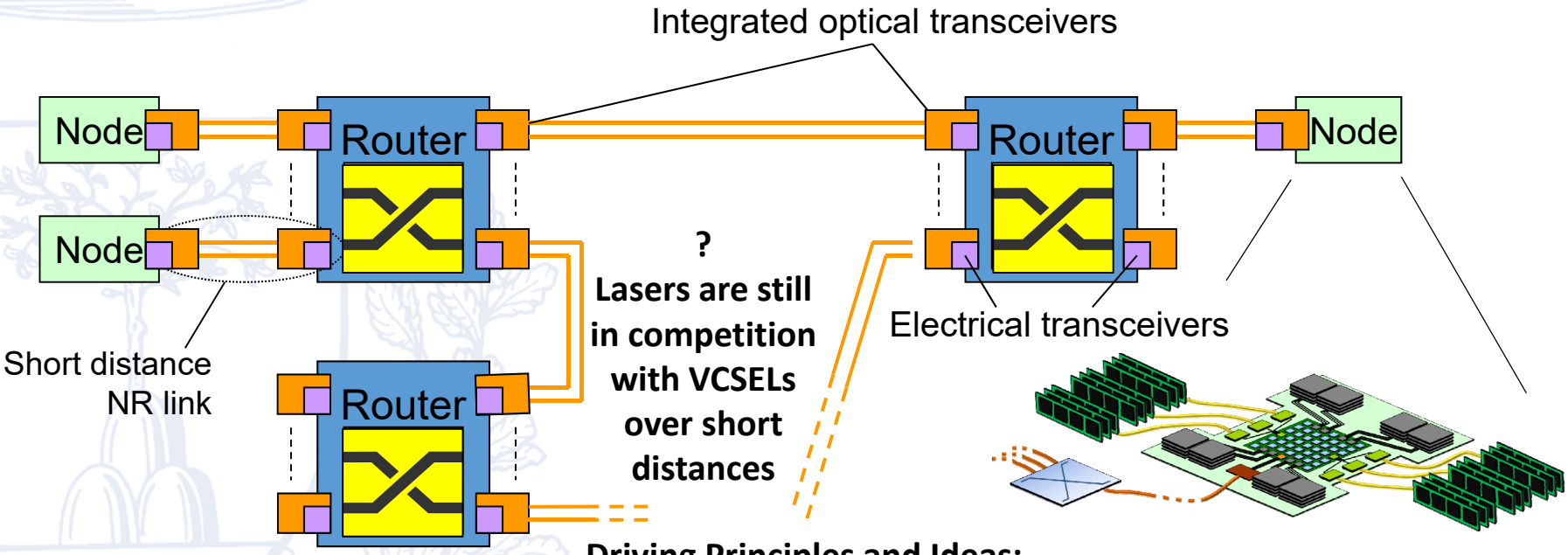
Silicon photonics uses co-integration techniques of optical components and/or transceivers with standard CMOS manufacturing process



Courtesy: S.Rumley

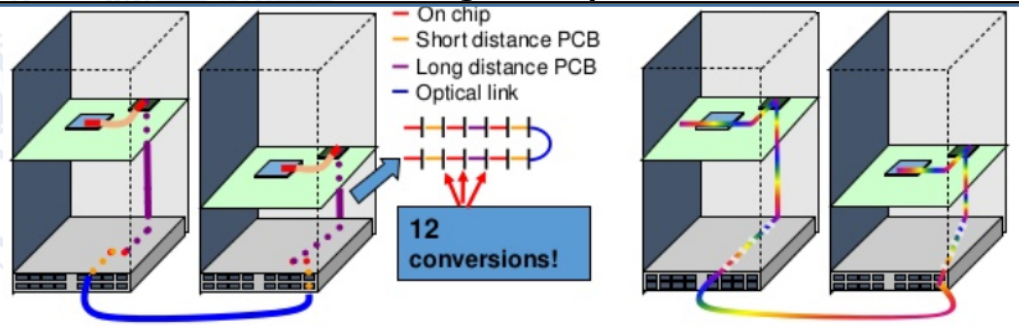
Silicon Photonics: Game Changer?

Silicon photonics is delivering integrated optical transceivers and holds promise of bringing optical communications closer to and deeper into the processing node



Driving Principles and Ideas:

Conventional hop-by-hop data movement



Flattened end-to-end data movement

Courtesy of K.Bergman

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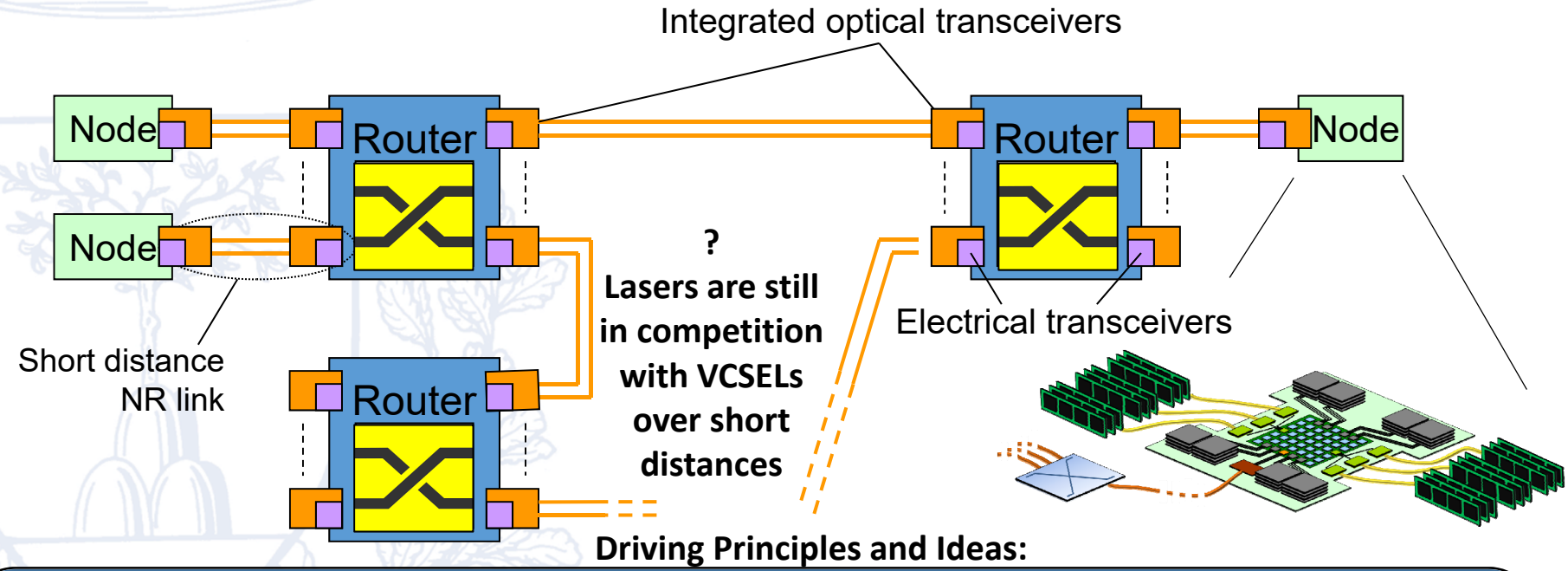
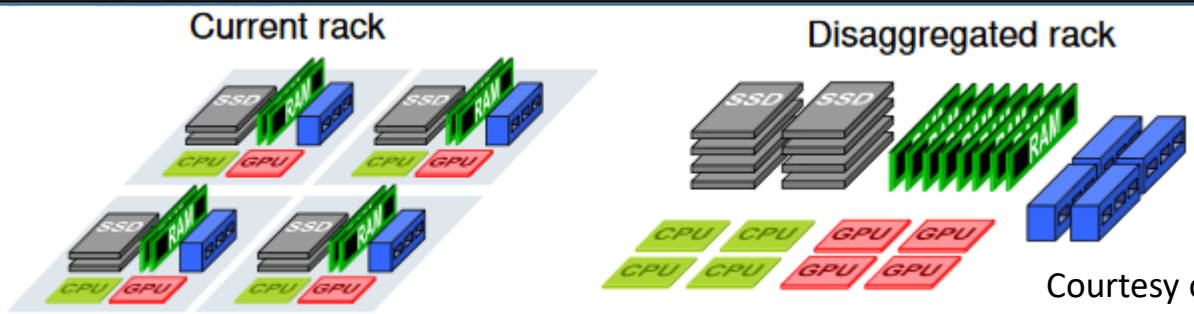


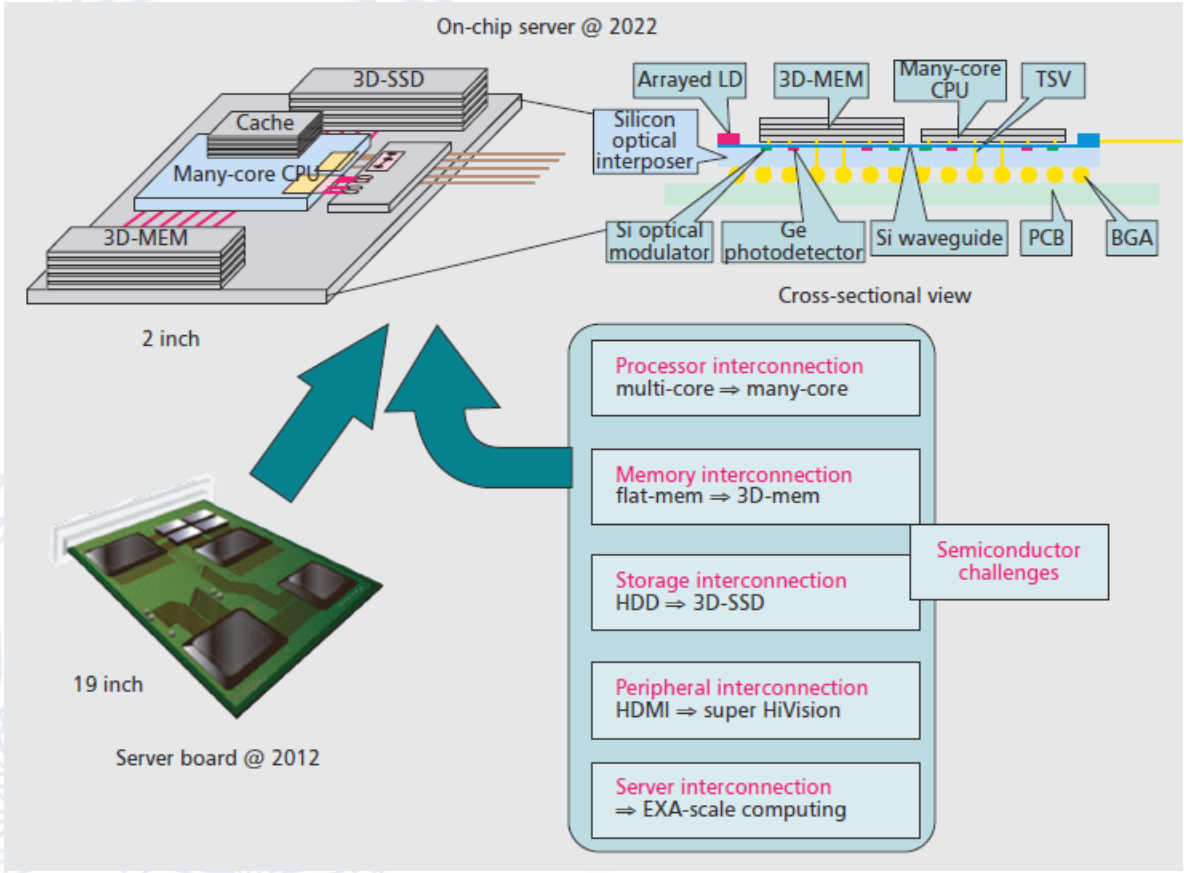
Driving Principles and Ideas:

Disaggregated architectures



Courtesy of K.Bergman

Looking Forward: Photonically-Integrated On-Chip Server



Key Advantages:

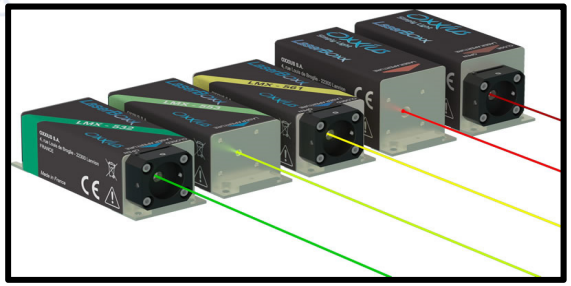
- **19 inches server boards shrink to 2 inches**
- **Huge Bandwidth: 6.6Tbps/cm²**
- **Si-Photonics Interposer's Size : 30 x 30 mm²**
- **Reduced Power**

On Chip Server through Silicon Photonics Interposer
Reference: "Silicon Photonics for next generation System integration Platform"
Y.Arakawa et al., IEEE Communications Magazine, vol.51, Issue 3, pp.72-77, March 2013

Challenge

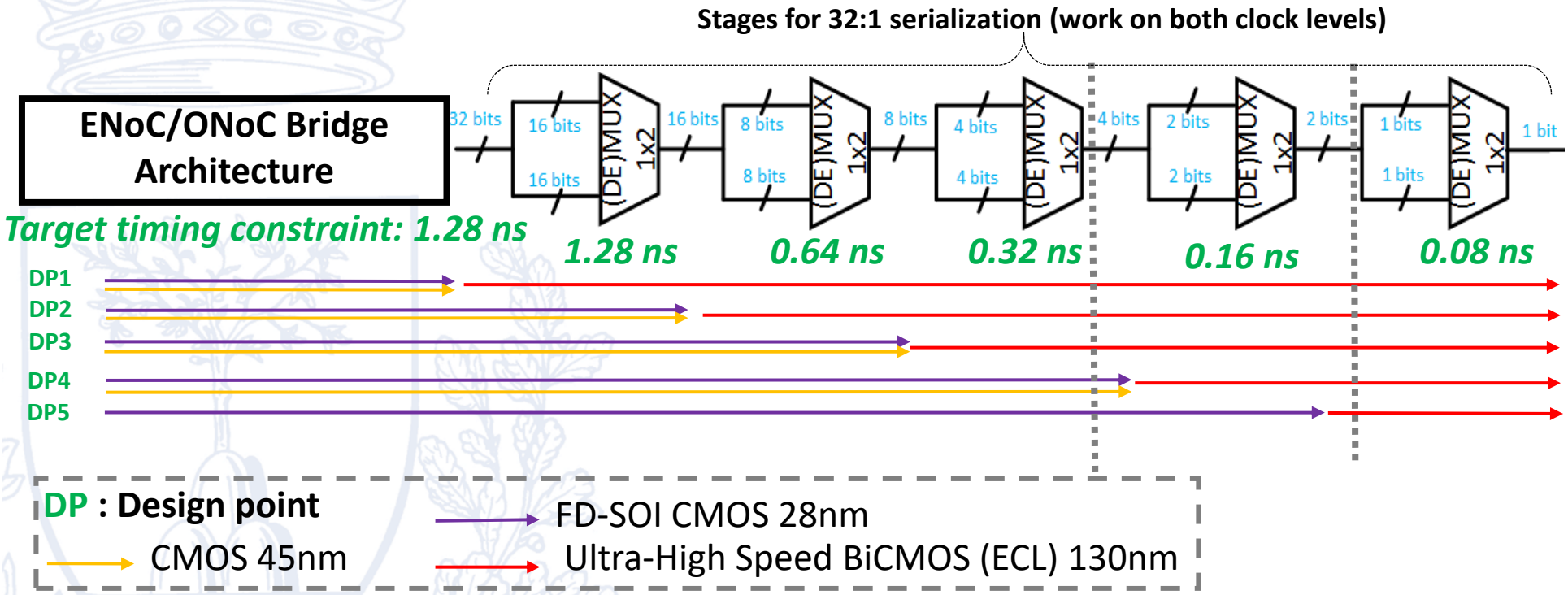
Silicon Photonics is not
as low-power as it is advertised

It is a static-power dominated technology, and makes sense only if you are able to fully utilize it!



The Optical Channel Configuration Dilemma

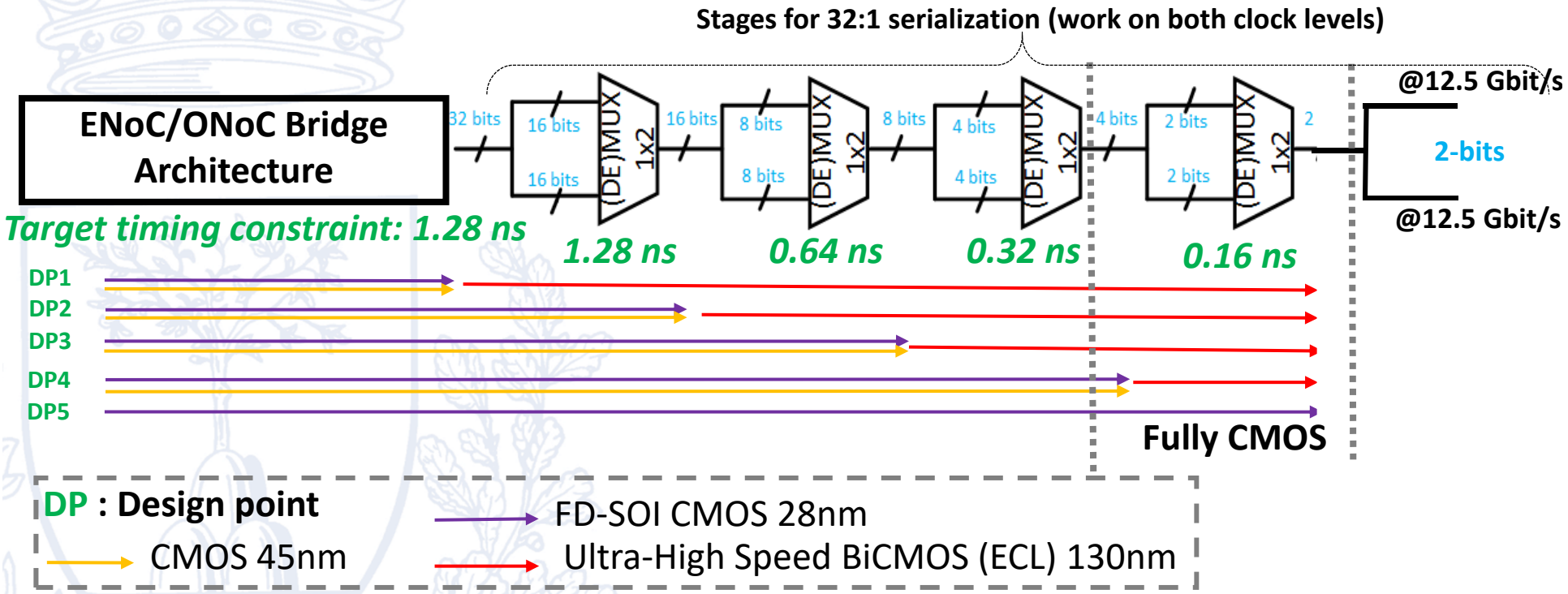
Example Target Data Rate for source-destination connection*: 25 Gbit/s*



Higher signaling rates are paid with more power-consuming high-speed electronics at the interface

The Optical Channel Configuration Dilemma

Target Data Rate for source-destination connection: *@25 Gbit/s*



Only higher bit parallelism in optics can make fully-CMOS interface implementations feasible

The Optical Channel Configuration Dilemma

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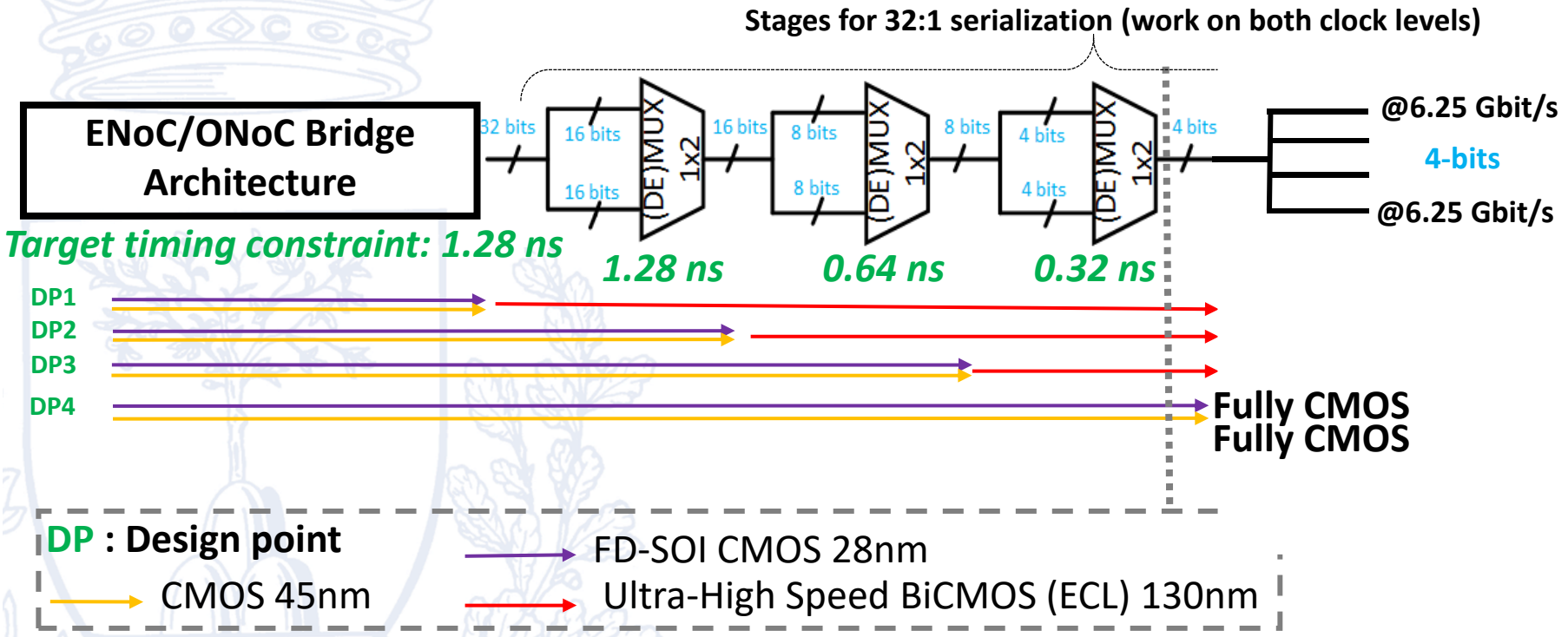
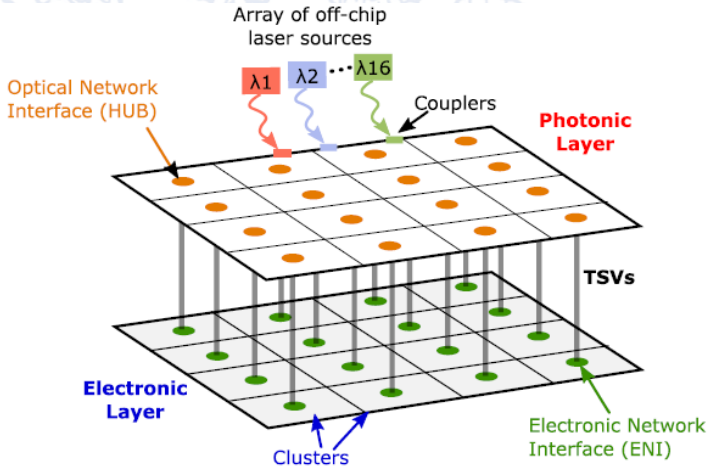


Further Increasing Optical Bit Parallelism makes more fully-CMOS design points feasible

The Optical Channel Configuration Dilemma



So, why not using more parallelism in optics through WDM?

Network-Level Trade-Offs Arise!

	No. of TSVs		No. of Laser Sources		Total Network Power [W]		Worst-case SNR	
	25 Gbit/s	40 Gbit/s	25 Gbit/s	40 Gbit/s	25 Gbit/s	40 Gbit/s	25 Gbit/s	40 Gbit/s
1 bit	1216	2176	32	32	65.6	83.4	16.2	16.14
2 bits	1216	2176	48	48	7.4	79.7	13.13	13.1
4 bits	2176	2176	80	80	9.6	11.01	8.8	8.8

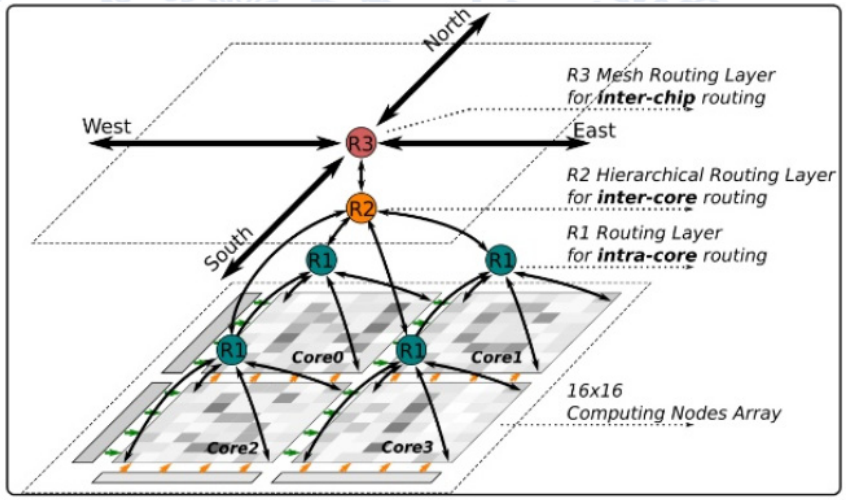
Optical parallelism comes with cost and signal integrity concerns, which are the price to pay for lower total power!

Some Other Challenges

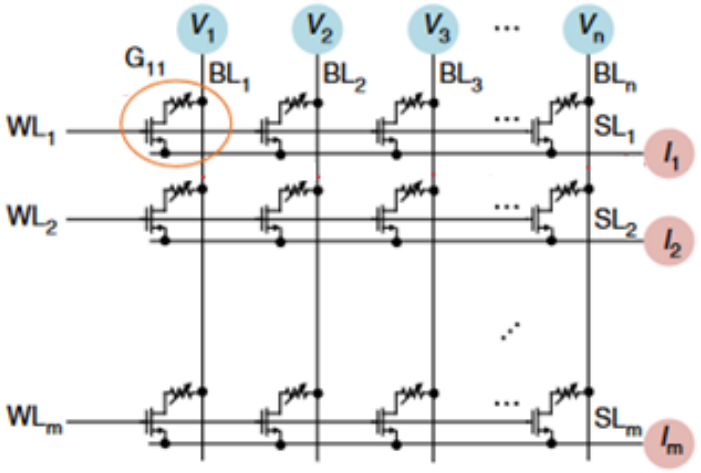
- Laser source integration
- Smaller size modulators are required
- Lower cost packaging and wafer-level testing
- Design and software
- Supply chain maturation similar to the semiconductor supply chain.
- New manufacturing solutions: zero-change approach on CMOS lines
- Temperature-aware design from the ground up

Not Only Communication!

- The brain seems to have something very special about energy efficiency
- Brain-inspired computing may be the killer application for non-conventional and/or emerging technologies



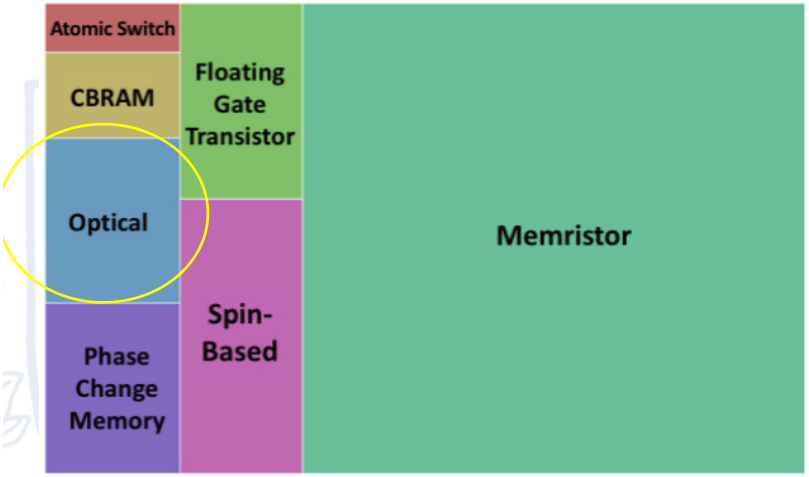
Asynchronous networks-on-chip



Memristors

The Role of Optics

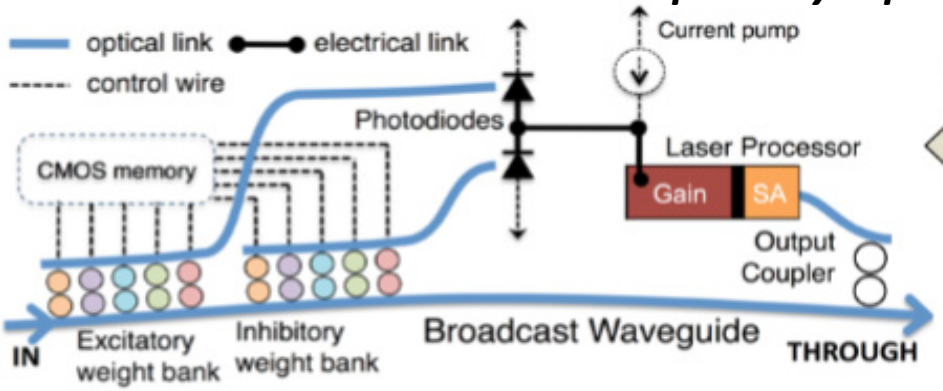
- Non-standard device-level or circuit-level components for neuromorphic engineering



Promising technology for ultra-low fast operation, programmability and relatively low complexity.

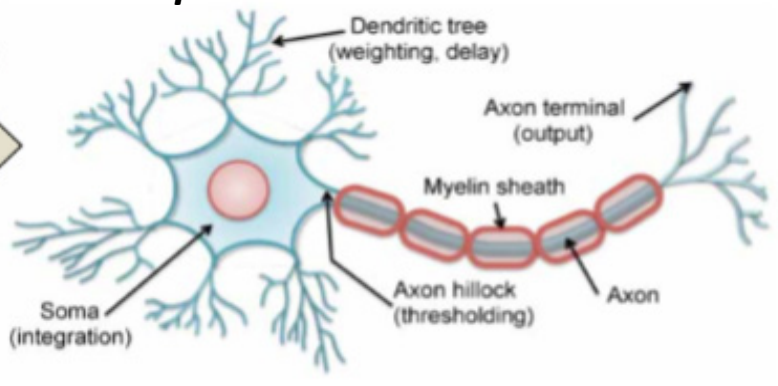
C.D.Schuman et al., 2017
reports number of papers on neuromorphic computing making use of a specific technology (see box sizes)

Case studies as optical synapses and neuron implementation



Laser Model

Analogy



Biological Model

B.J.Shastri et al., 2014

Questions for Discussion

- Optics deeper into the communication hierarchy?
  - ✓ Can optics replace multiple electronic conversions with 1 «major» conversion?
  - ✓ Can optics enable new system-level design paradigms?
- Optical networks-on-chip: a means of writing papers or a technology of practical relevance?
  - It may also depend on us!
- Optics as a «way to compute»: heading to the peak of inflated expectations? This would be a good sign….
- Electronics-photonics integration
  - ✓ monolithic integration vs. 2.5D vs. 3D integration?
  - ✓ Serdes-free interfaces? How to alleviate resynch. overhead?
- Design automation
  - ✓ Supporting technology or enabling it? Really beyond CMOS EDA, or reuse?
- We typically say that technology maturity has to improve
  - ✓ How far are we from such entry-level maturity level?
  - ✓ What about cost?

THANK YOU