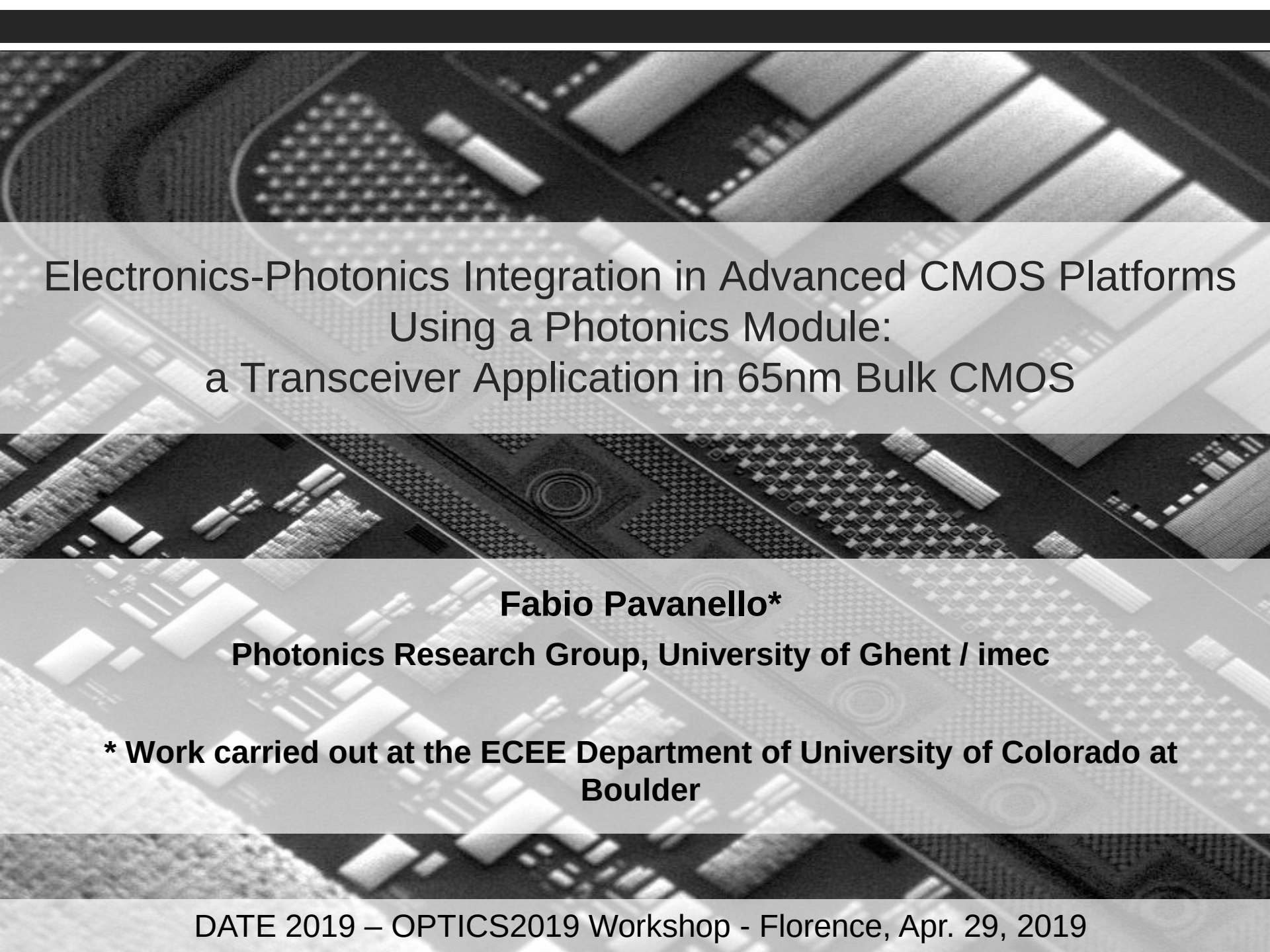


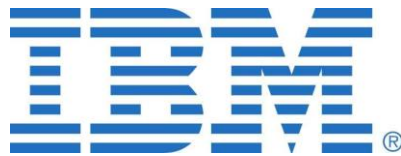
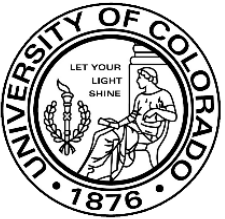


Electronics-Photonics Integration in Advanced CMOS Platforms Using a Photonics Module: a Transceiver Application in 65nm Bulk CMOS

Fabio Pavanello*

Photonics Research Group, University of Ghent / imec

*** Work carried out at the ECEE Department of University of Colorado at Boulder**



- **Why photonics in bulk CMOS platforms?**
- **Current approaches for photonic transceivers**
- **Introducing a photonics module in CMOS platforms: challenges and benefits**
- **Basic building blocks**
- **Energy-efficient and high-BW density transceivers in a 65 nm bulk node**

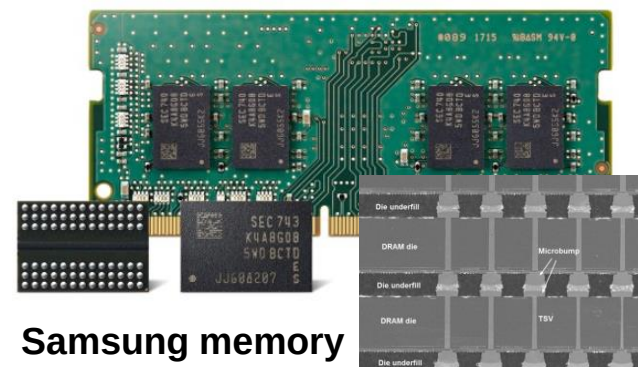
- Computing performance are limited by the electrical I/O bandwidth
- Optical transceivers on CMOS can address I/O limitation



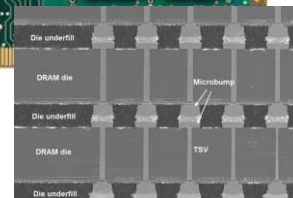
Broadcom Tomahawk Switch
16 nm FinFET



NVidia P100 GPU
16 nm FinFET



Samsung memory
10 nm LPP FinFET

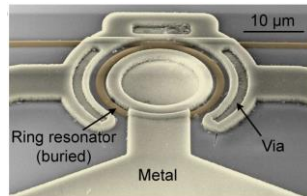


DRAM stacks

Polysilicon exists in every CMOS technology
and can be used for photonics

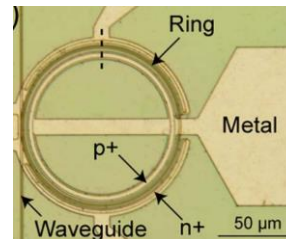
- Discrete passive and active components

Modulator



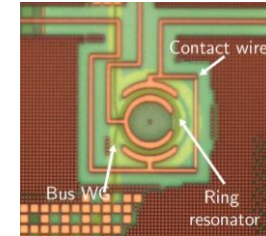
K Preston Opt. Ex. 2009
Lipson Group

Photodetector



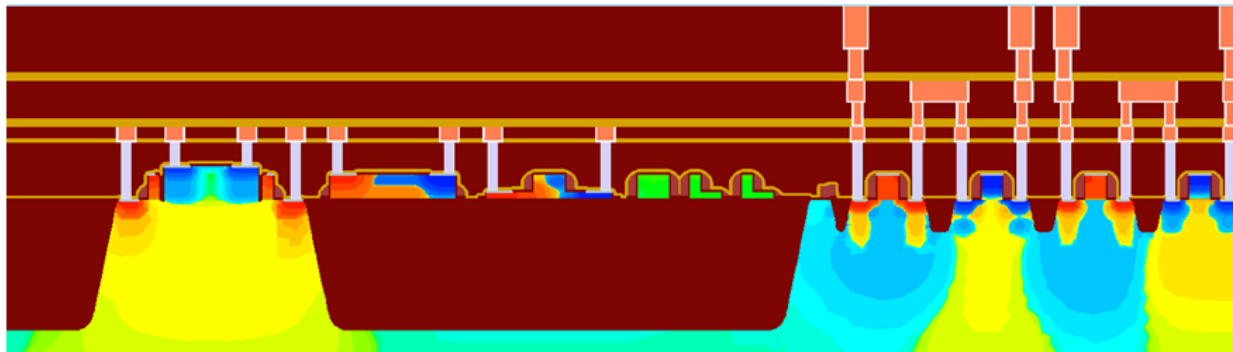
K Preston Opt. Lett. 2010
Lipson Group

Photodetector



K Mehta Opt. Lett. 2014

- Electronic-photonic integrated systems in 0.18 μm CMOS



Sun et al., JCCS 2015

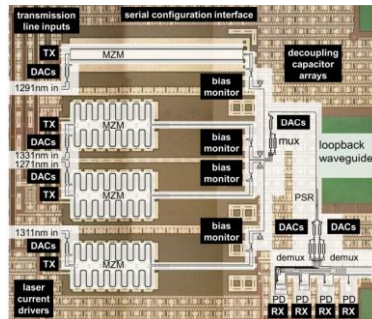
R. Meade, VLSI 2014

Moving towards integration with state-of-the-art CMOS

Transceiver solutions:

Monolithic (SOI)

- High sensitivity receivers
- More power efficient

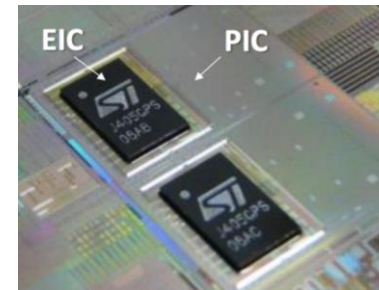


IBM

Orcutt et al.,
OFC 2016

Heterogeneous (SOI+Bulk Si)

- Flexibility in choosing photonics and CMOS separately

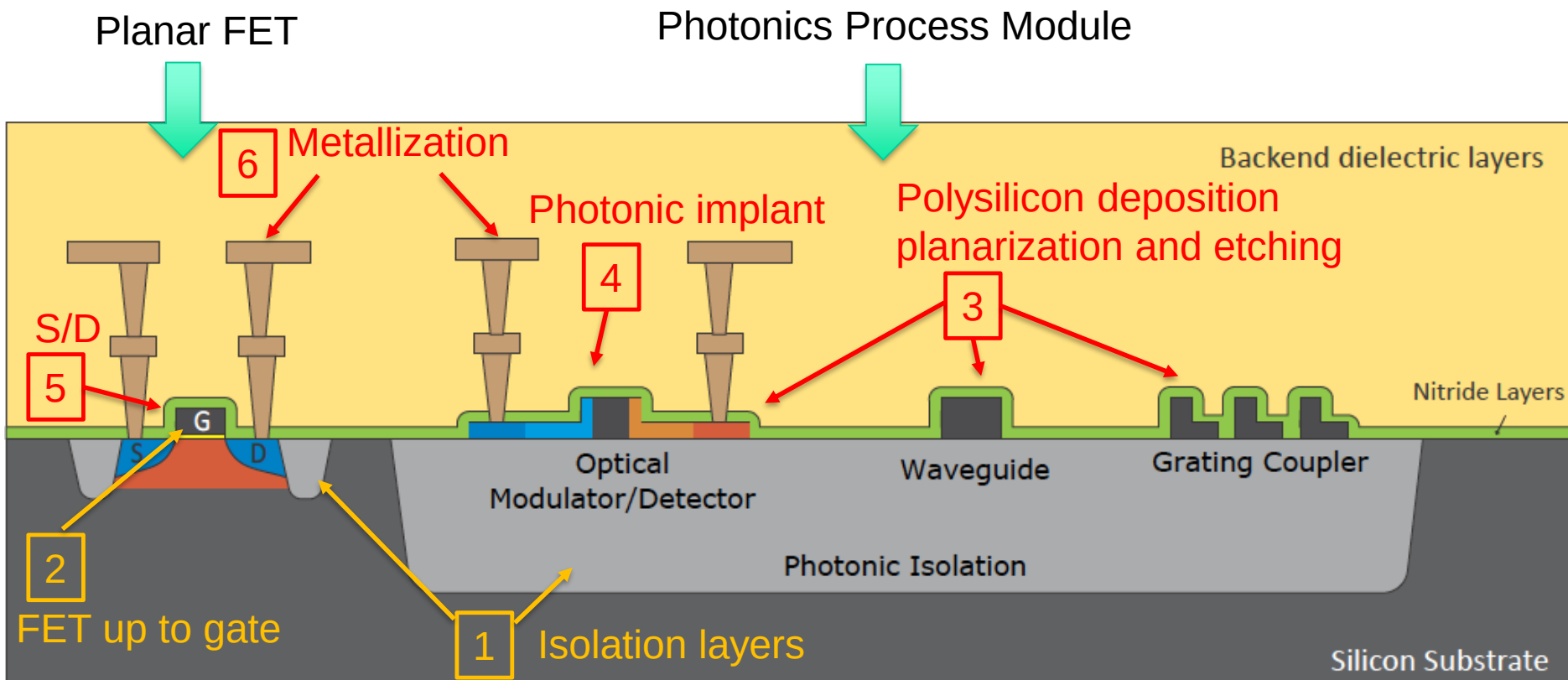


ST/Luxtera

Boeuf et al.,
OFC 2015

Combining the advantages of the two solutions
by integrating photonics on bulk CMOS

- Suitable integration in some of the most deeply scaled CMOS processes: planar bulk, finFET bulk and FD-SOI CMOS
- Can easily achieve 25 Gb/s for transmit and receive



Photonics added with only 6 lithography masks

Electronic-Photonic CMOS Platform

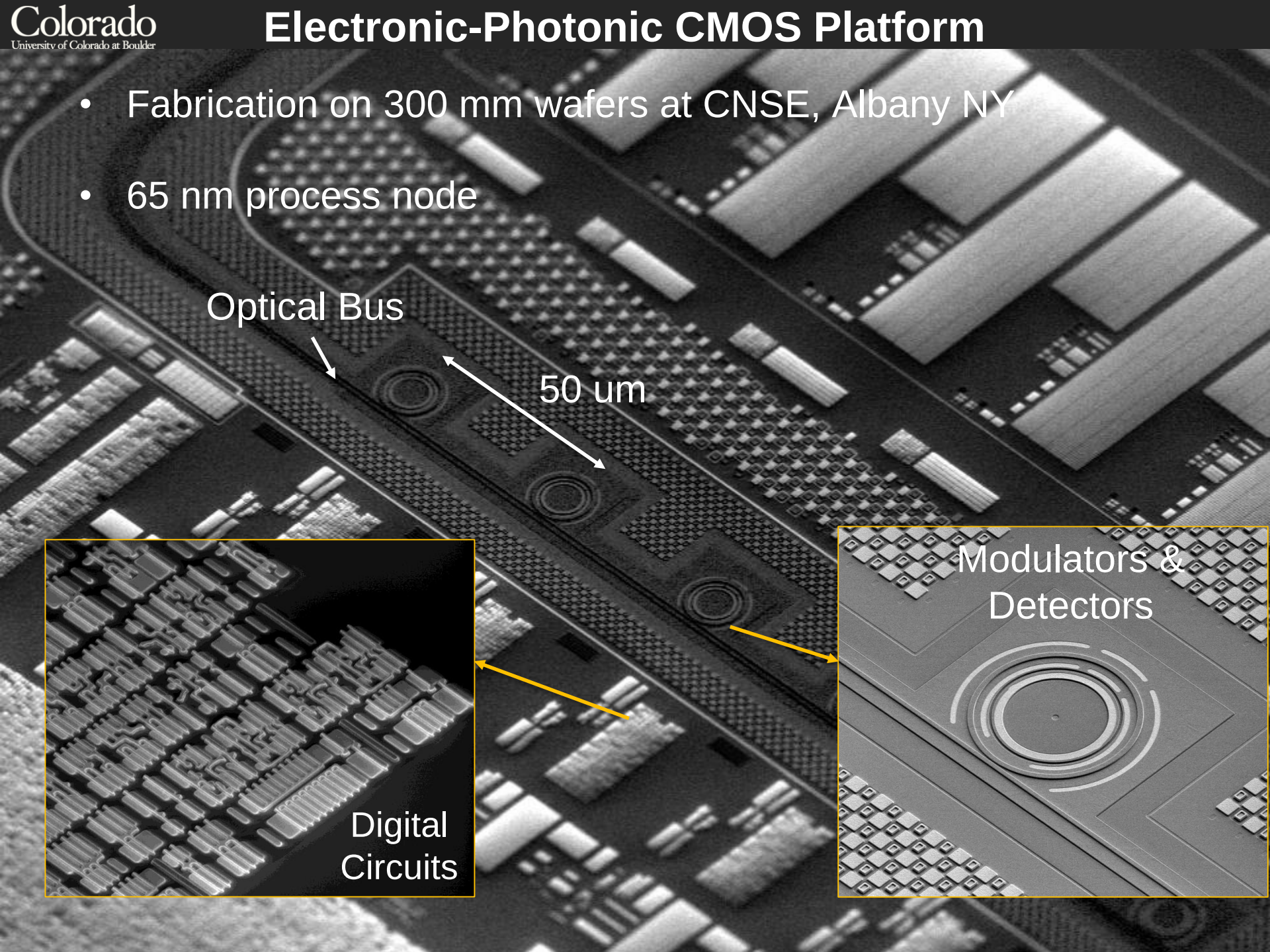
- Fabrication on 300 mm wafers at CNSE, Albany NY
- 65 nm process node

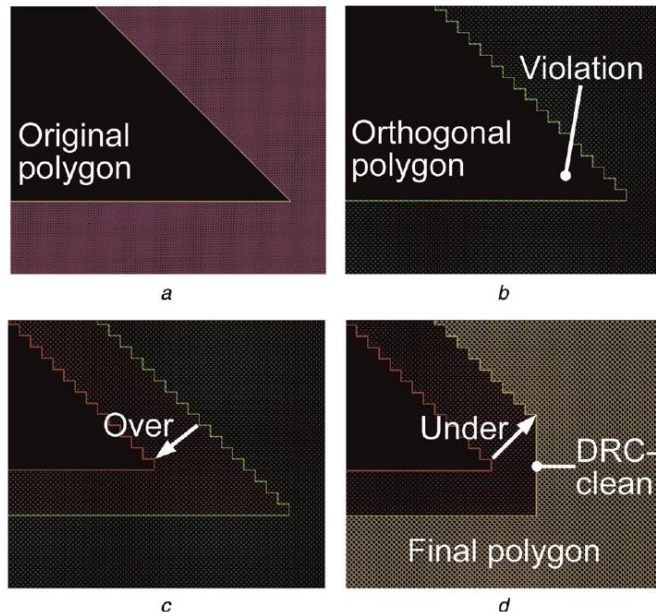
Optical Bus

50 μm

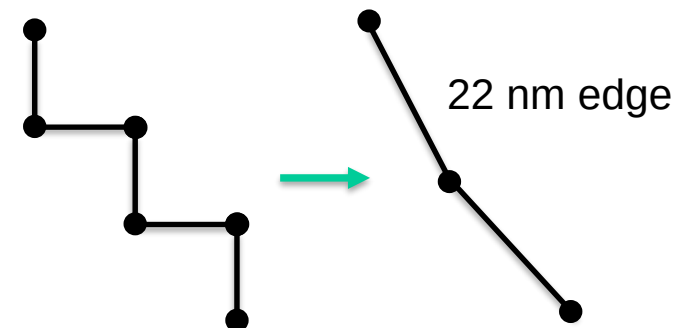
Modulators &
Detectors

Digital
Circuits



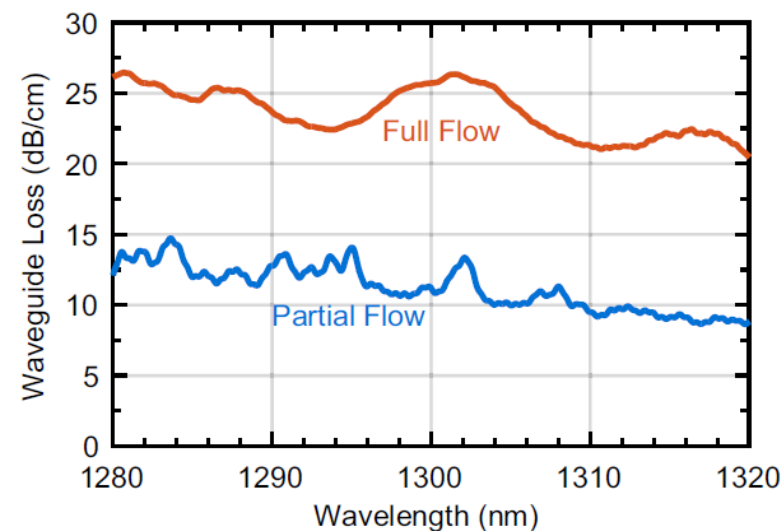


Alloatti et al., IET Optoelectronics **9(4)** (2015)

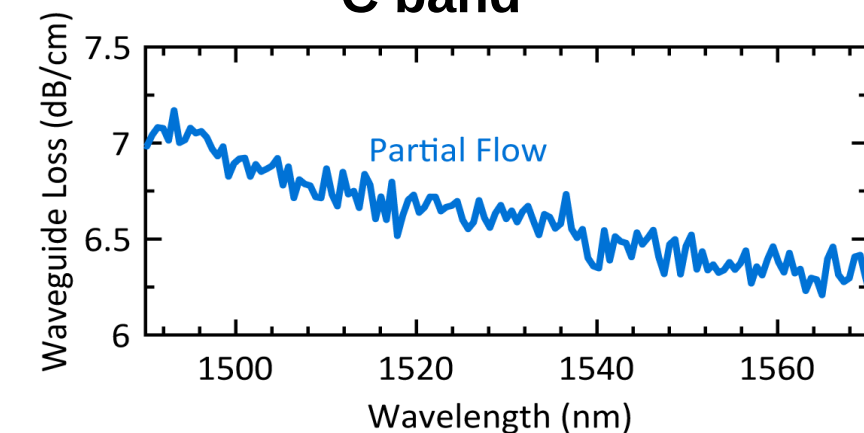


- Layout of the reticle performed in Cadence (Virtuoso Suite)
- Process design kits used: GF 10lpe + custom PDK for photonics
- In-house extension of Cadence Virtuoso to allow for solving DRC sizing issues (min feature size)
- No optical proximity correction employed
- Final layout on a non-Manhattan grid for processing file volume reasons

O band

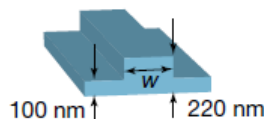


C band

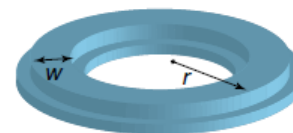


Passive components (specifications at 1,300 nm)

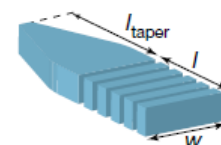
Ridge waveguide



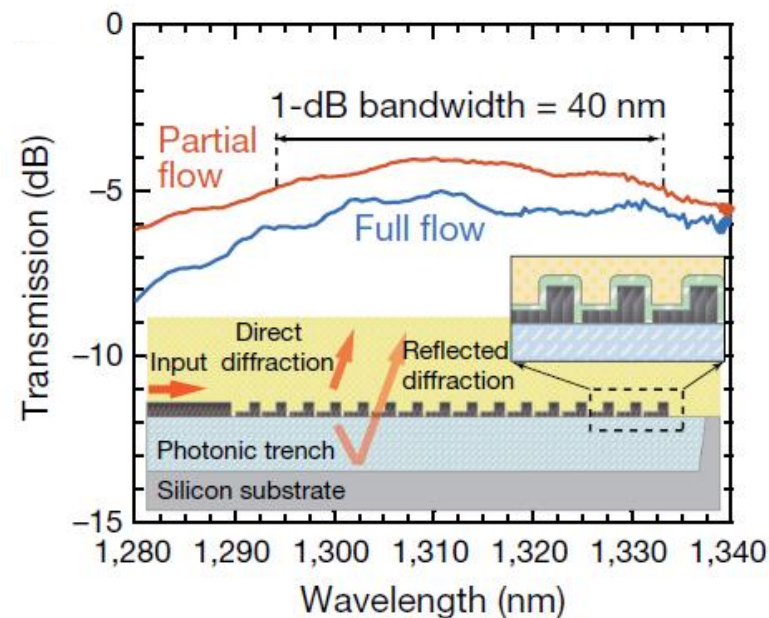
Ridge microring



Grating coupler



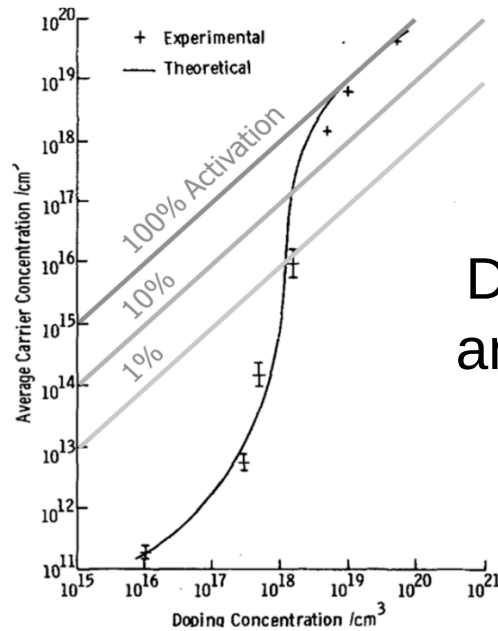
	Propagation loss	Intrinsic Q	Coupling loss
Partial flow	8–15 dB cm ⁻¹	19,000–31,000	4.2 dB
Full flow	21–27 dB cm ⁻¹	10,000–19,000	5.2 dB
Dimensions	$w = 400$ nm	$w = 400$ nm $r = 7.5$ μ m	$w = l = 8$ μ m $l_{\text{taper}} = 250$ μ m



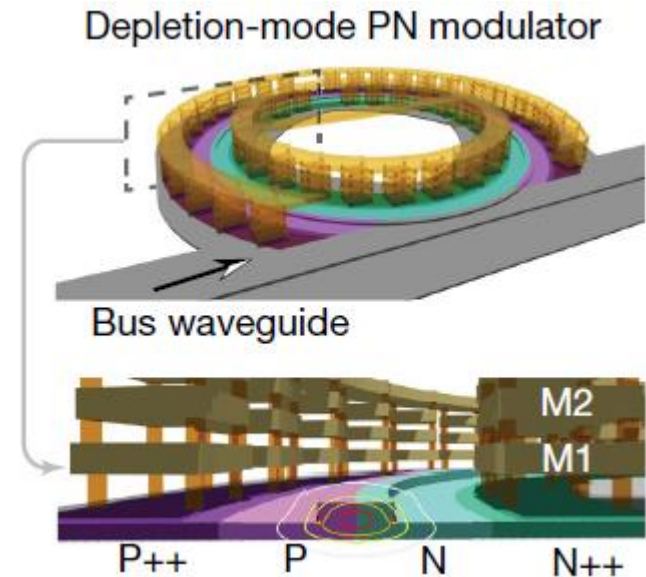
Atabaki, Moazeni, Pavanello et al., Nature 556, 2018.

CU Nanophotonic Systems Laboratory

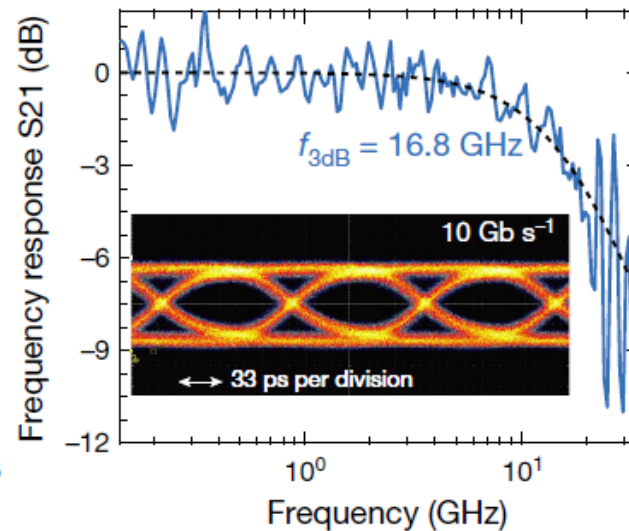
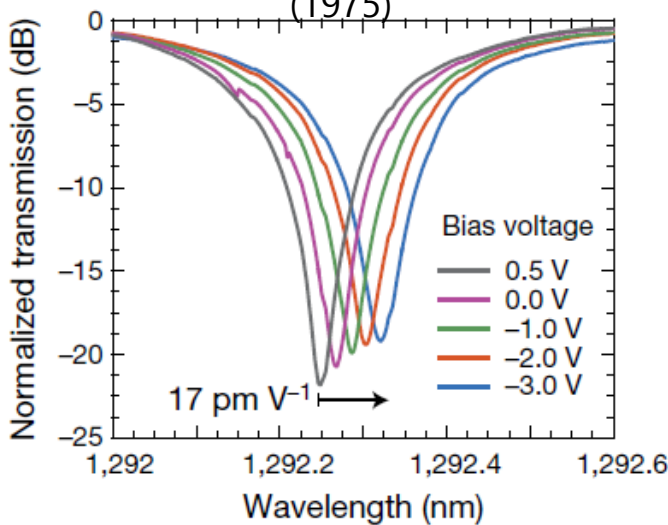
10



Deposition, annealing
and implant conditions
are critical!



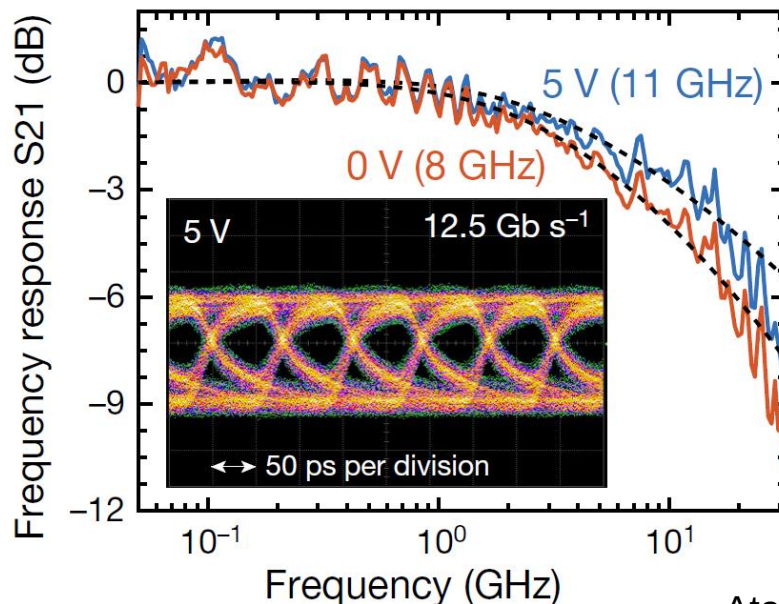
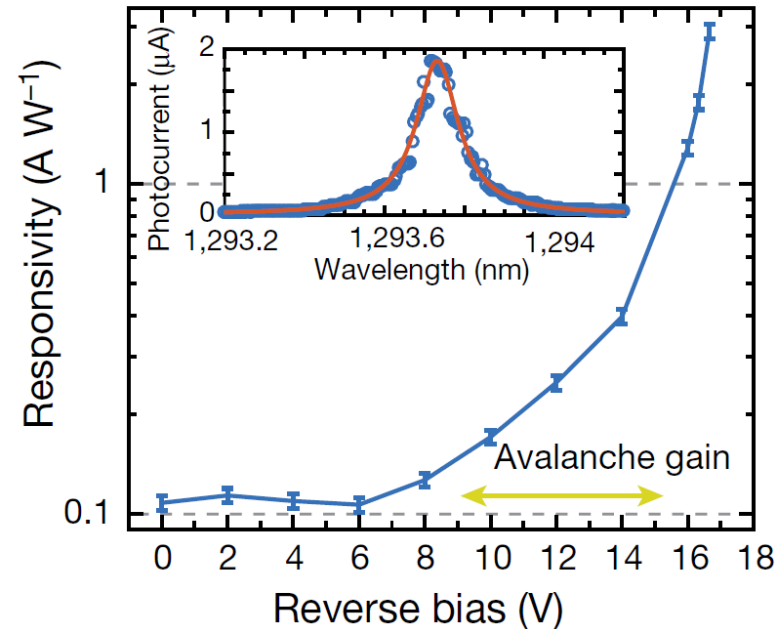
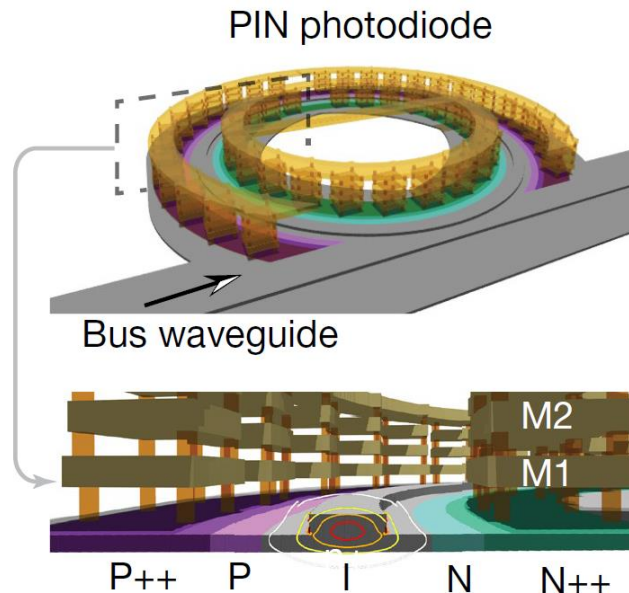
Seto et al., Appl. Phys. Lett. 46
(1975)



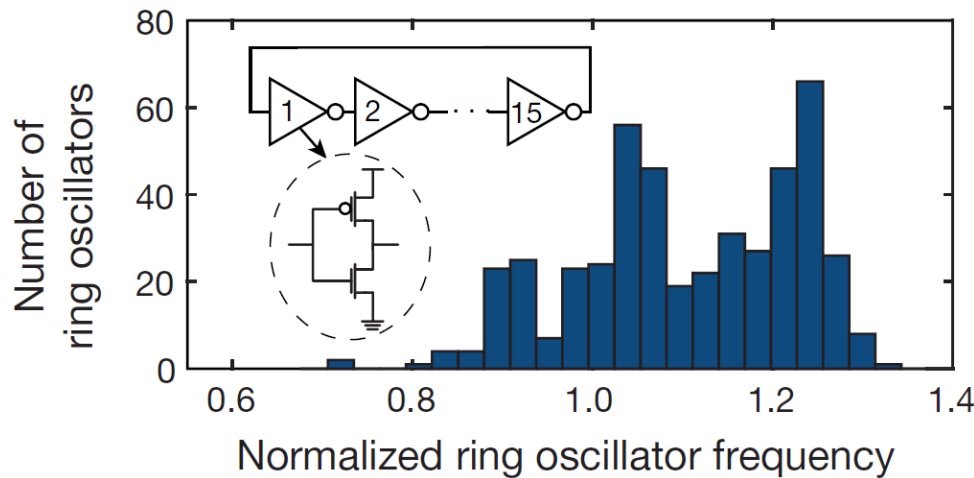
- 2 Vpp
- BW: 17 GHz
- ER: 5.7 dB
- IL: 3.8 dB

$Q_l = 4.5k$

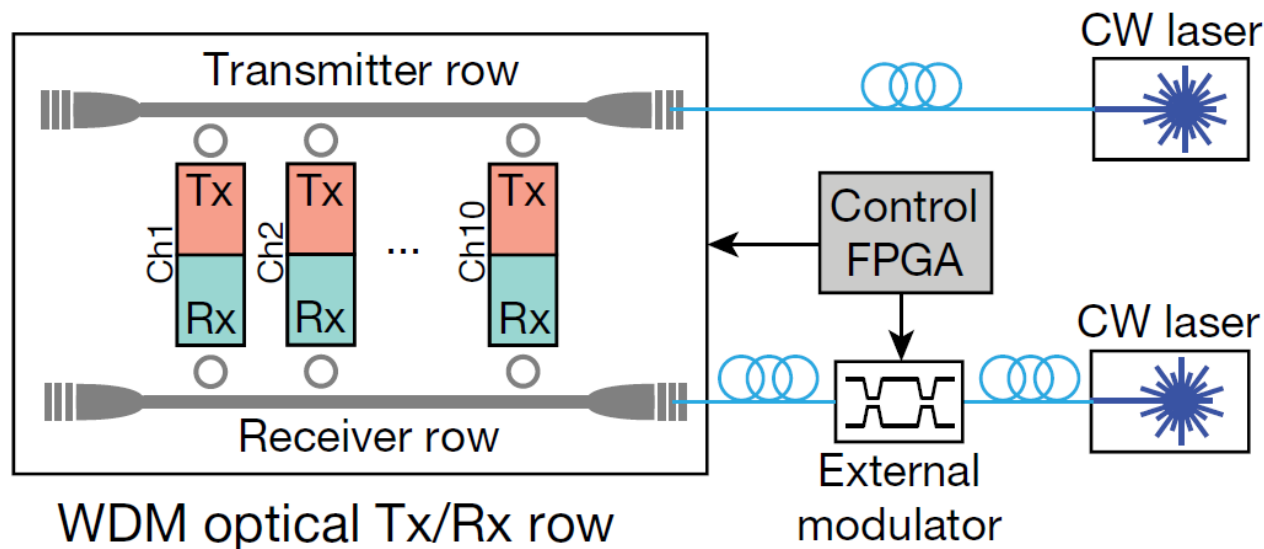
Atabaki, Moazeni, Pavanello et al., Nature 556, 2018.



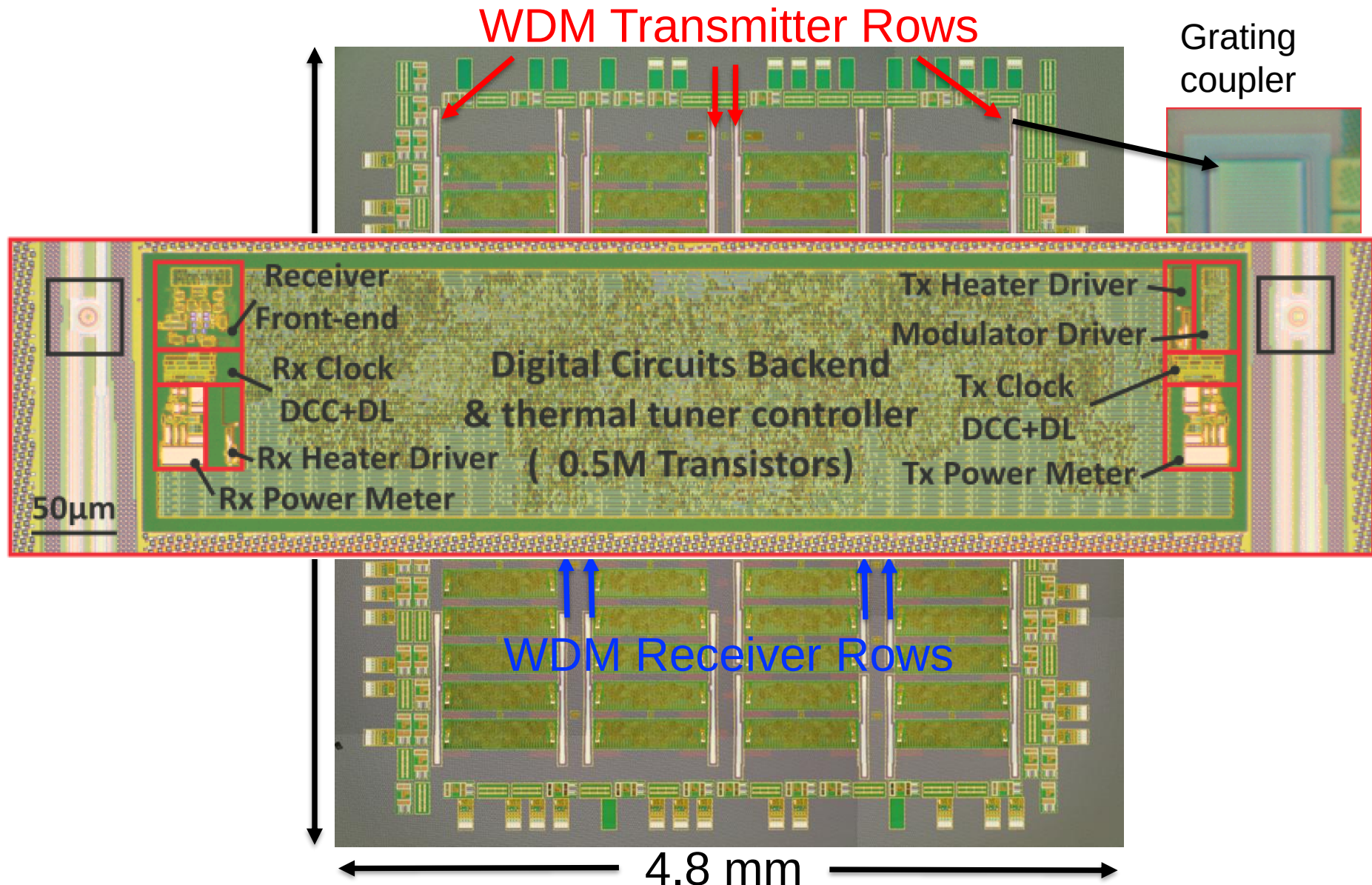
- Defect-mediated absorption
- BW: 8 (11) GHz @ 0 (5) V bias
- Avalanche gain: 13 @ 16 V bias



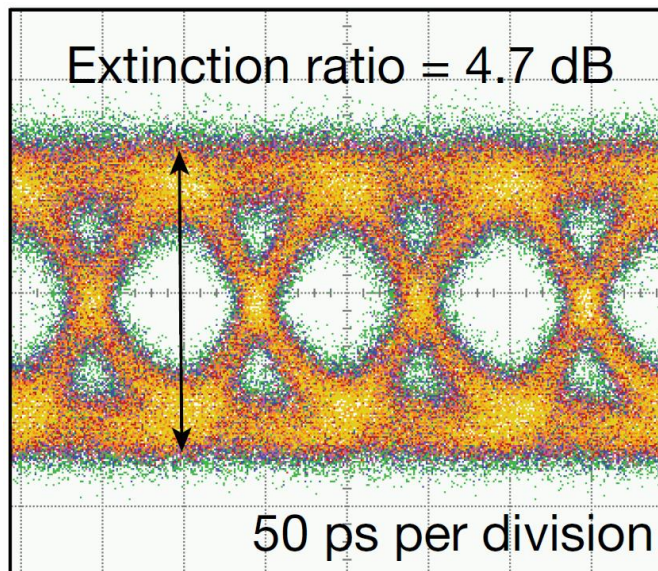
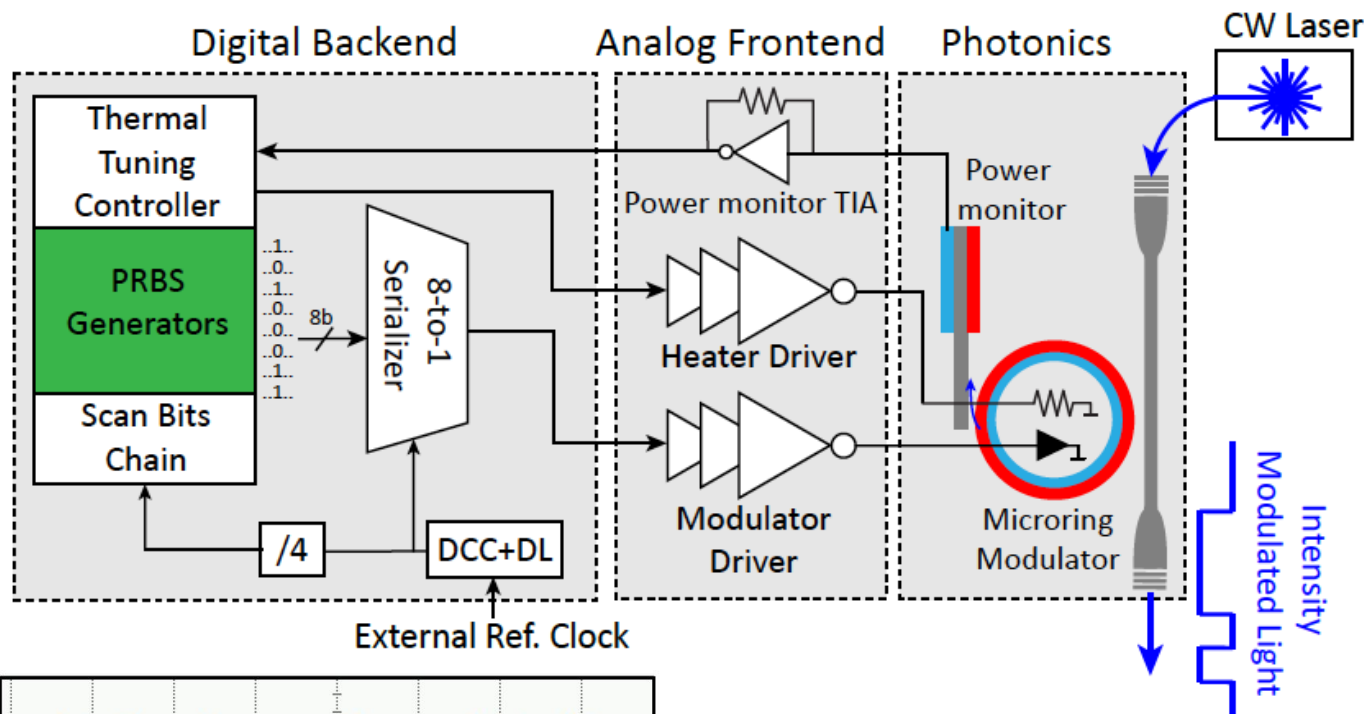
- Transistors performance are **not** compromised by the photonics module



Monolithic WDM Optical Transceivers

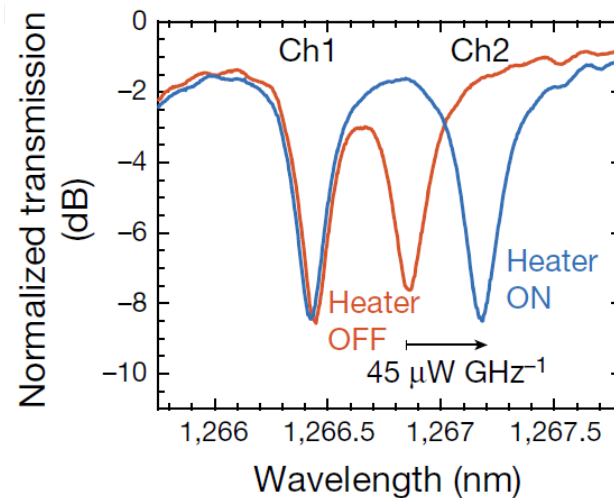
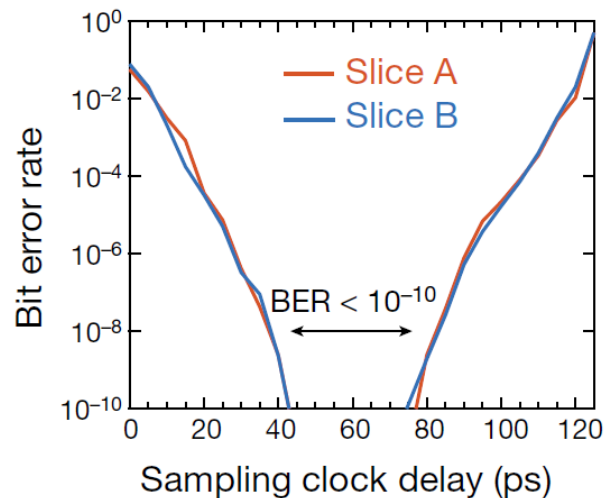
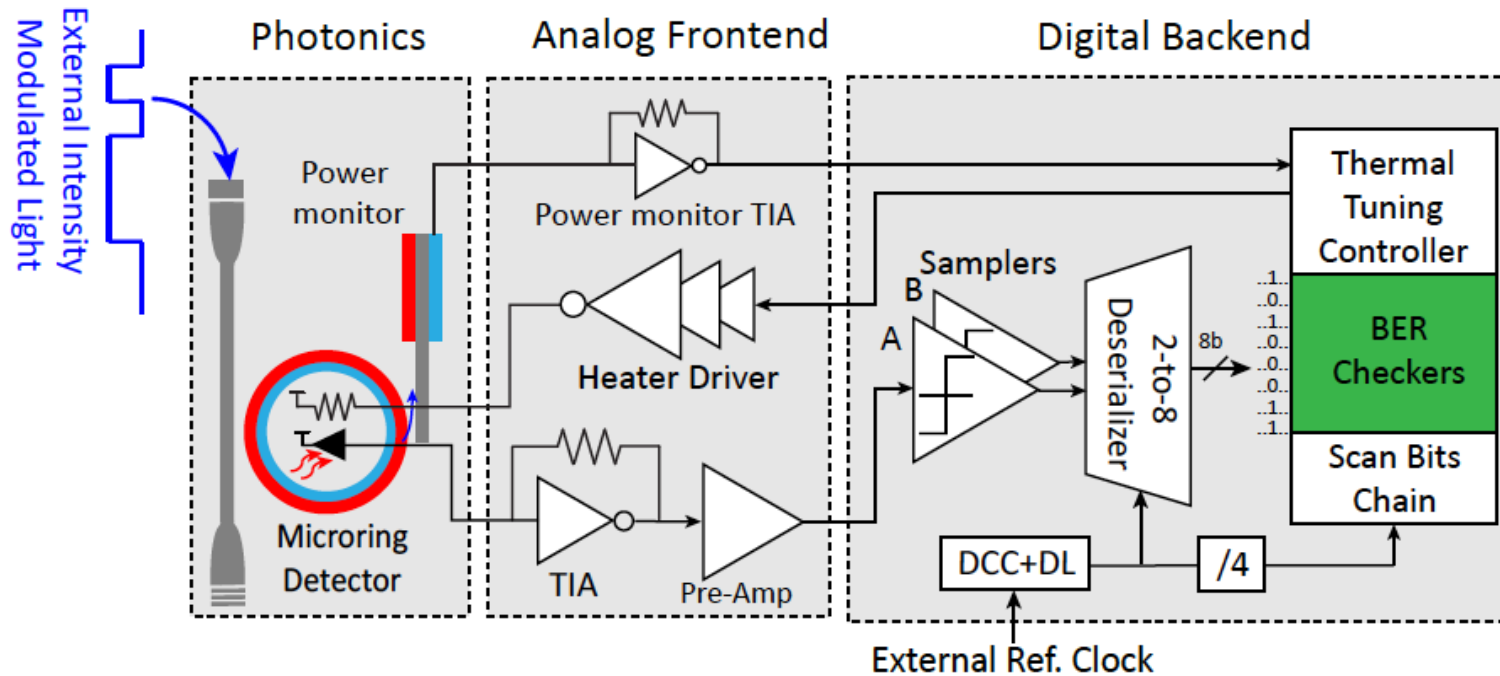


O-Band Monolithic Photonic Transmitter



- 10 Gbit/s speed (limited by the circuits)
- 100 fJ/bit energy

Atabaki, Moazeni, Pavanello et al., Nature 556, 2018.



- 7 Gbit/s speed
- 500 fJ/bit energy
- Transceiver BW density: 180 Gb/s/mm²

- Polysilicon photonics as a viable material platform
- Integration of polysilicon photonics with deeply scaled CMOS
- 10 Gb/s monolithic transceivers demonstrated, 25 Gb/s is achievable with device optimizations
- Sub pJ/bit high bandwidth density transceiver: toward multi-Tbps I/O for CMOS chips



- H. Gevorgyan
- J. Notaros
- M. Wade
- K. A. Qubaisi
- I. Wang
- B. Zhang
- A. Khilo
- **M. A. Popović**



- **A. Atabaki**
- L. Alloatti
- **R. Ram**



- S.A. Kruger
- C. Baiocco



- **S. Moazeni**
- C. Sun
- **V. Stojanović**



- Gordon Keeler