

DESIGNING LARGE-SCALE PHOTONIC INTEGRATED CIRCUITS (PICs)

Muhammad Umar Khan, Yufei Xing and Wim Bogaerts

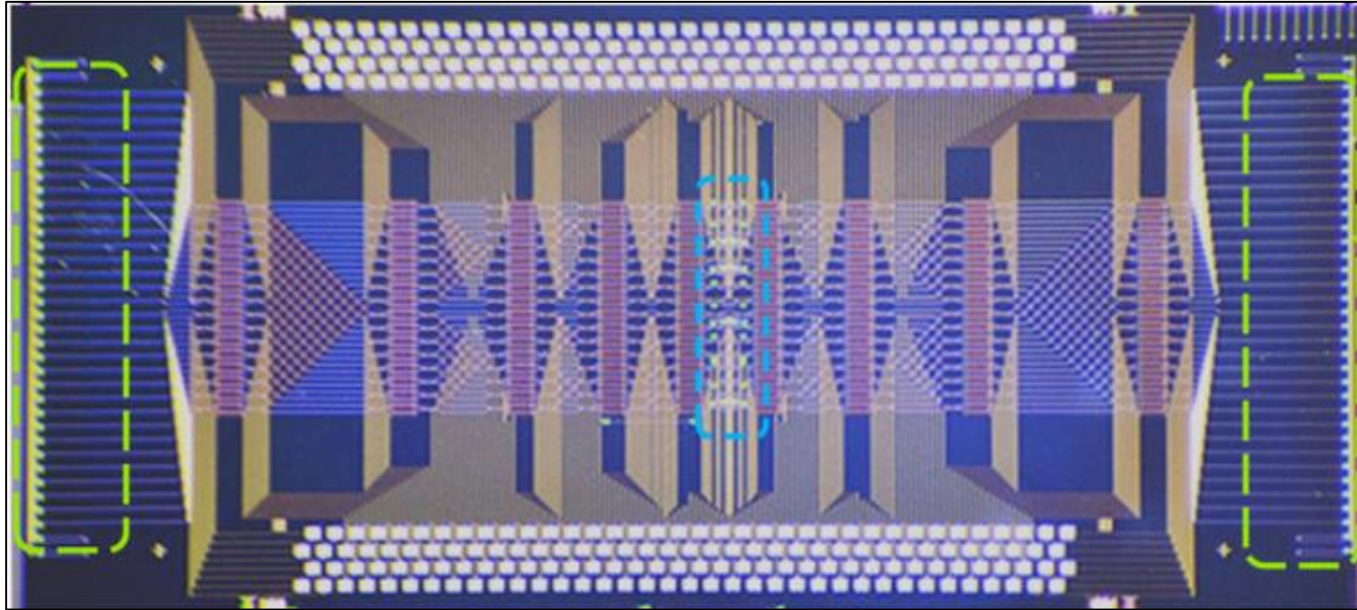
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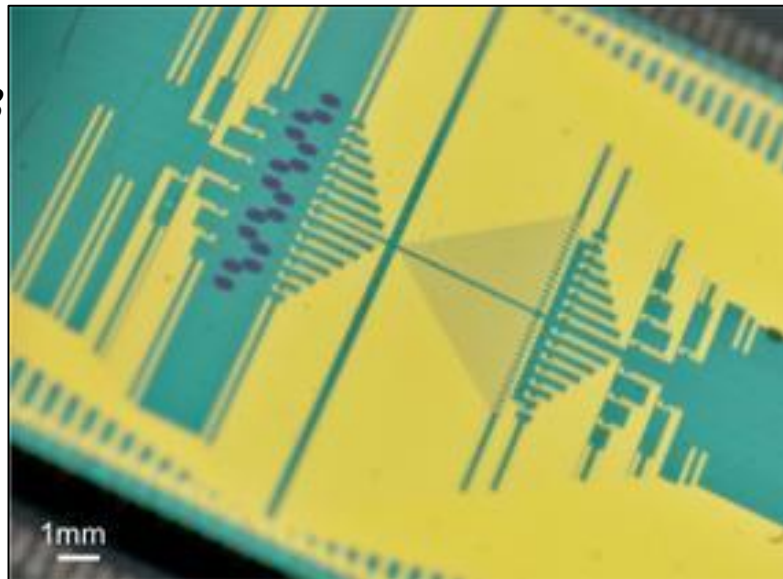
OUTLINE

- Large scale PICs
 - Fabrication imperfections/variability
 - *Silicon-on-insulator (SOI) waveguide*
- Design flow
 - Layout aware yield prediction
 - Parameter Extraction & spatial variability
- Summary

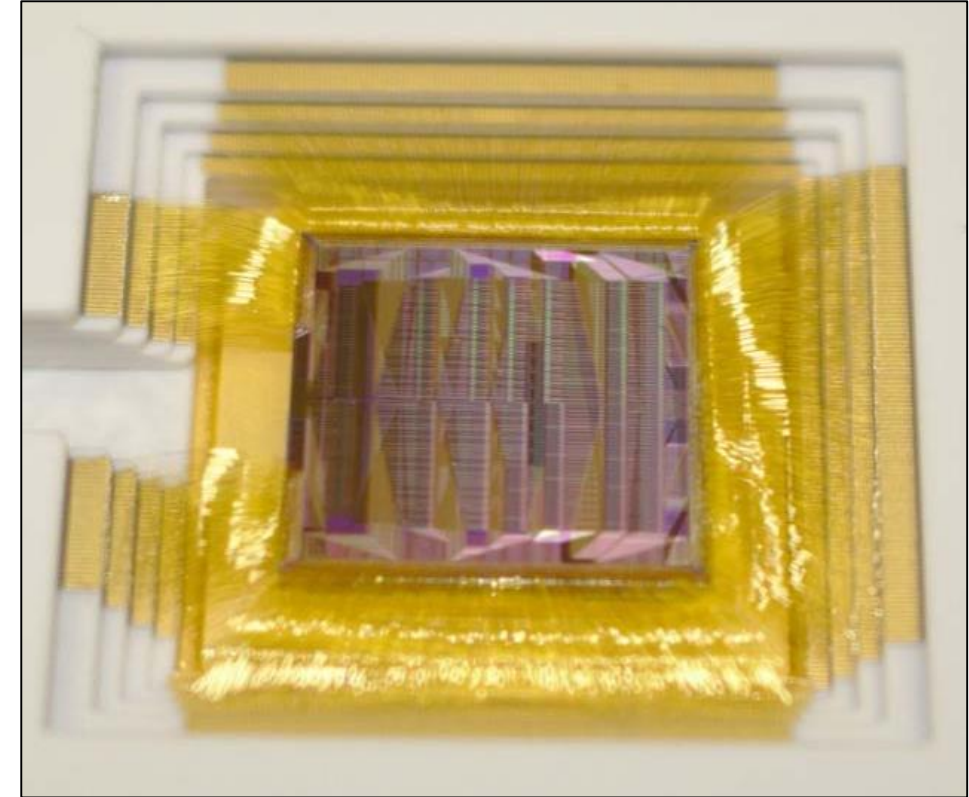
PHOTONIC LARGE-SCALE INTEGRATION IS HERE



Photonic switch
Cheng, et al., *Optics Express* 2018



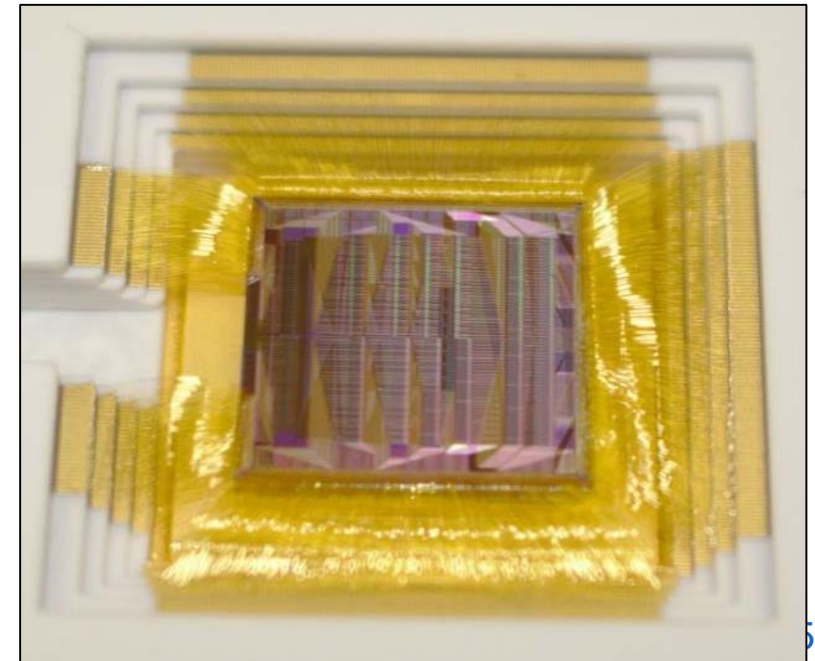
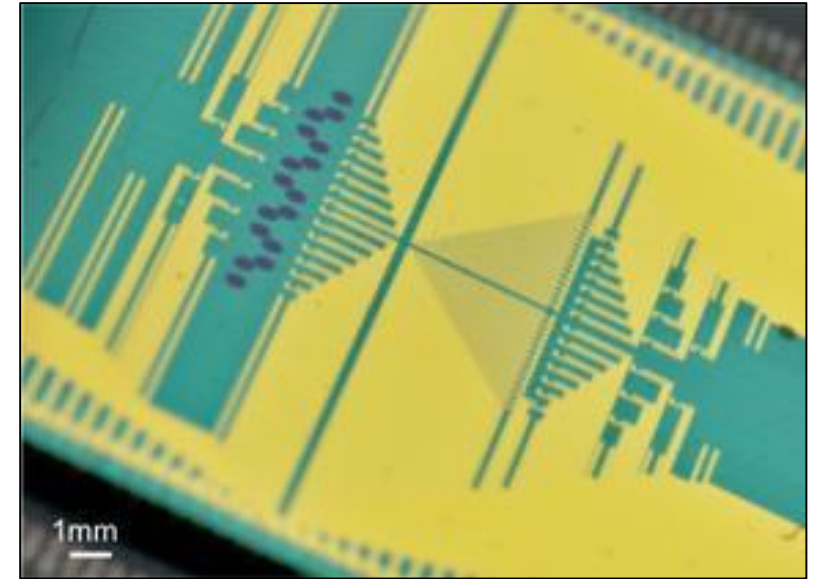
Quantum silicon chip
J. Wang, et al. *Science* 2018



32 × 32 SiPh switch matrix
D. Celo et al. 2016

PHOTONIC LARGE-SCALE INTEGRATION IS HERE

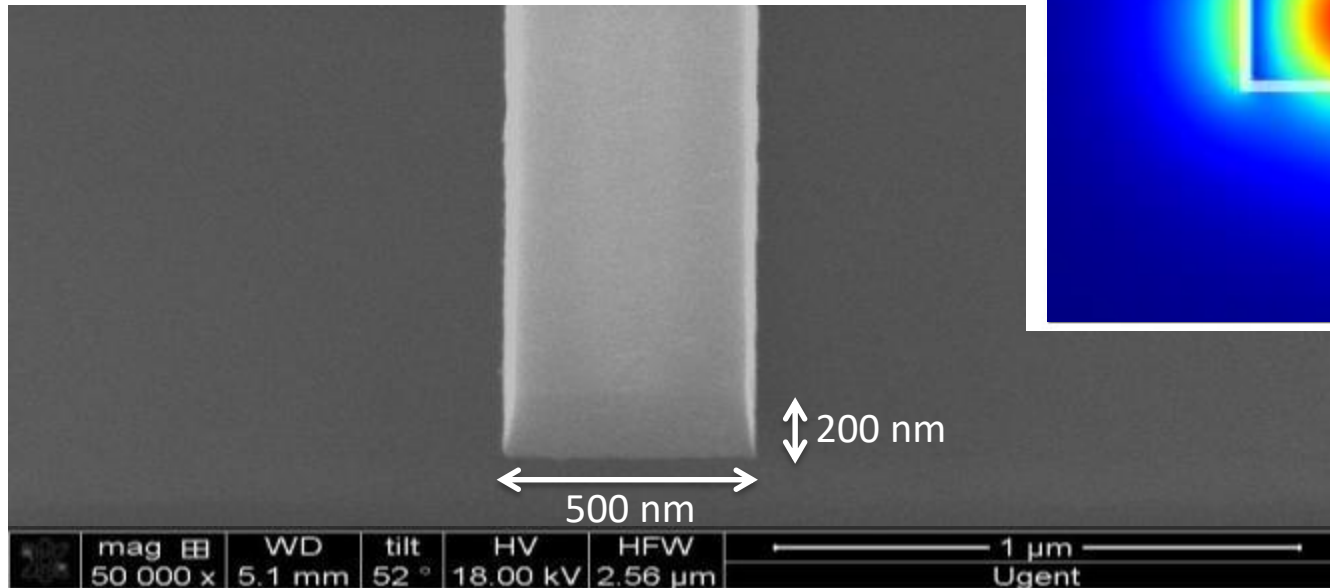
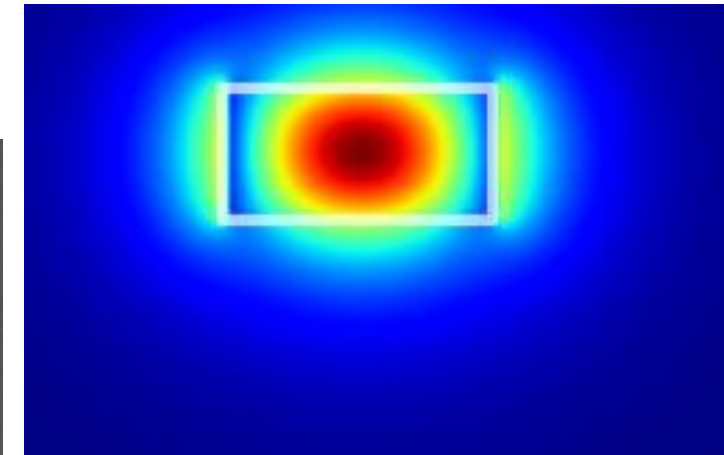
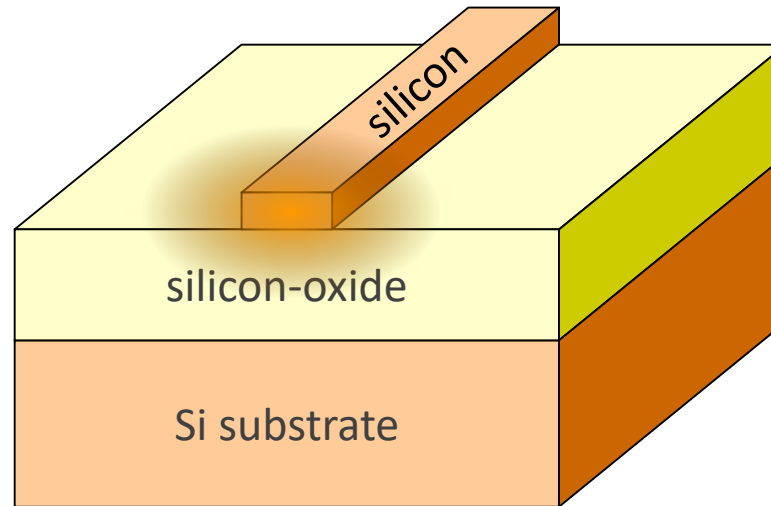
- Large scale PICs
 - Complexity
 - **Functionality** 😊
- Fabrication imperfections
 - Linewidth and thickness
 - **Not as desired** 😞
 - Fabrication variations accumulate
 - **Performance degradation** 😞
 - Lower fabrication yield
 - **Expensive** 😞



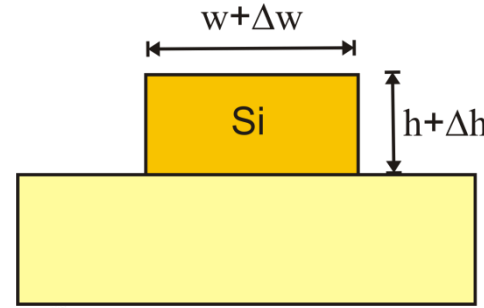
FABRICATION IMPERFECTIONS (VARIABILITY)

SILICON PHOTONIC WAVEGUIDE

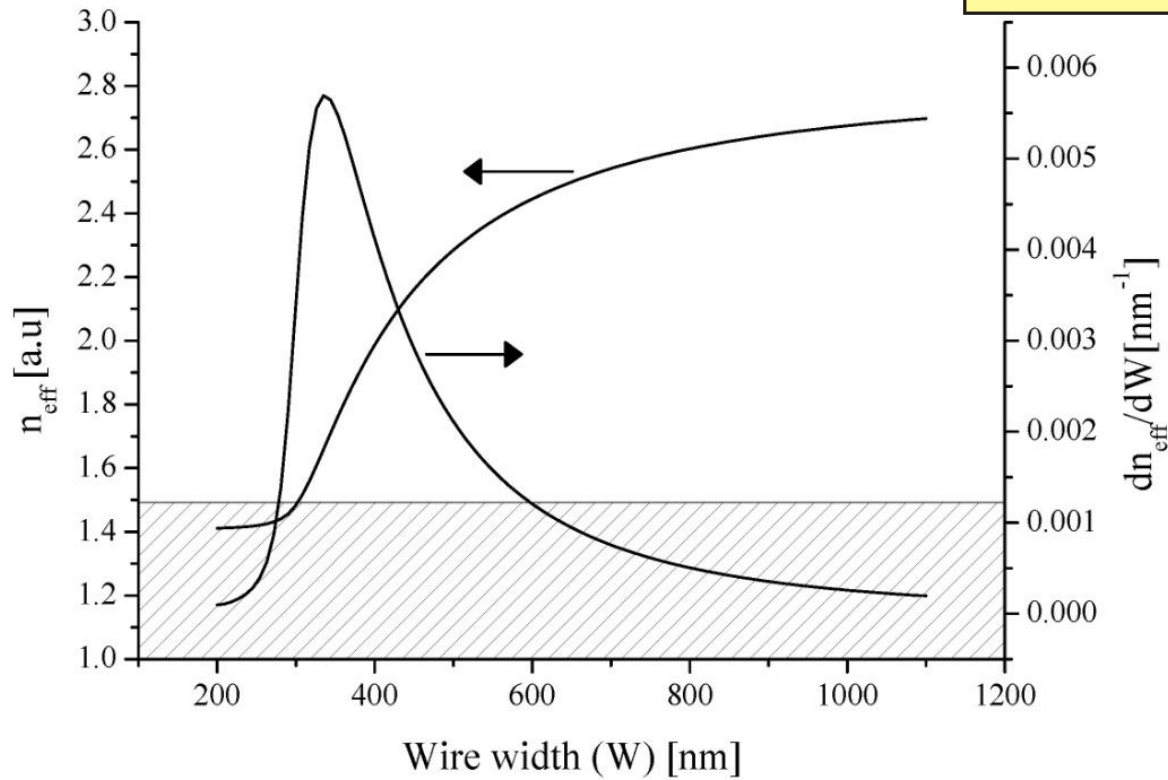
$$n_1(=3.5) > n_2(=1.45)$$



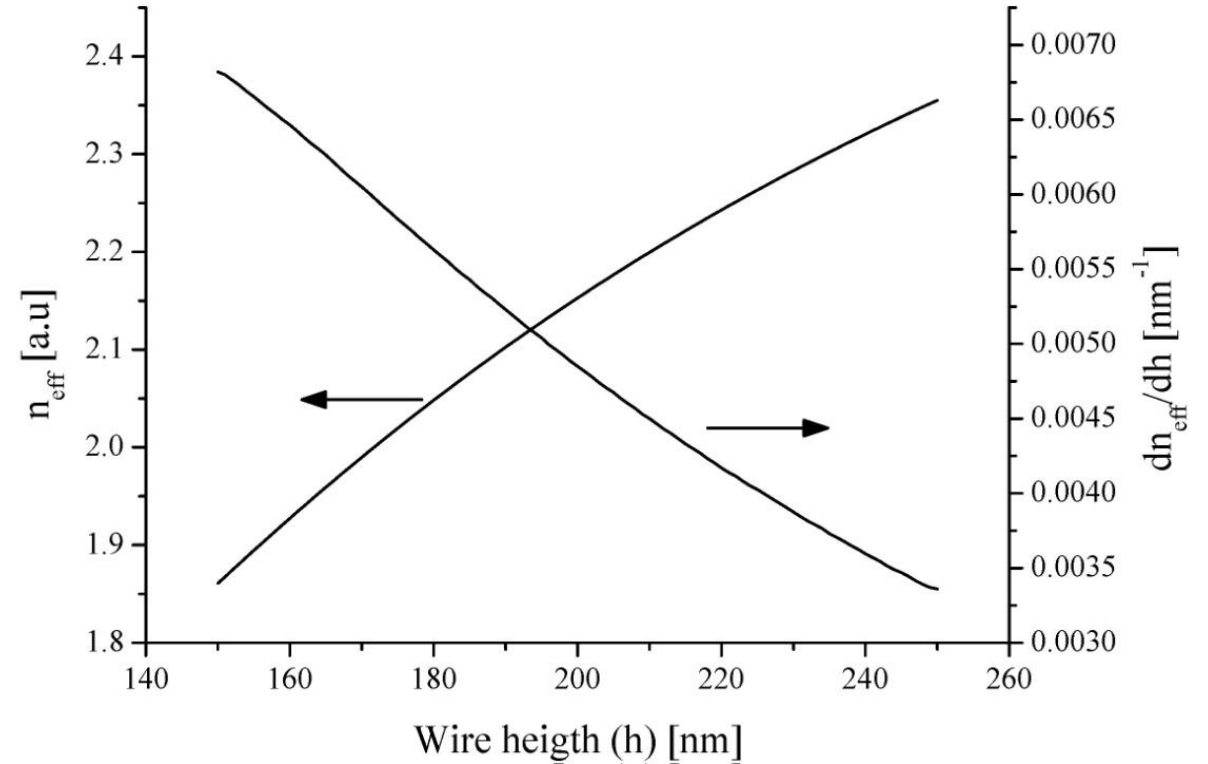
DIMENSIONAL DEPENDENCE OF A WAVEGUIDE



Effective index for different widths



Effective index for different heights



SENSITIVITY OF SILICON PHOTONICS

Silicon photonic waveguides are sensitive to

- geometry
- stress
- temperature
- ...

wire width

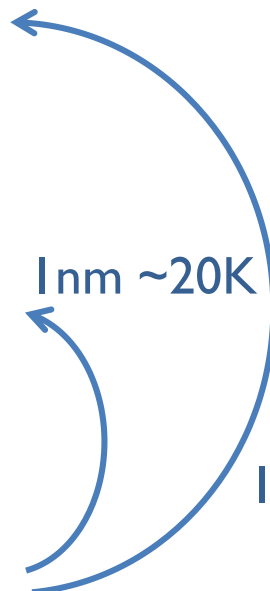
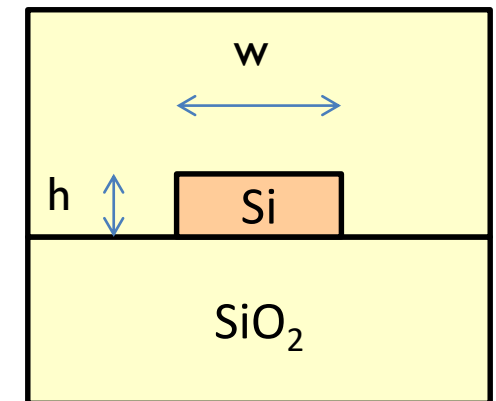
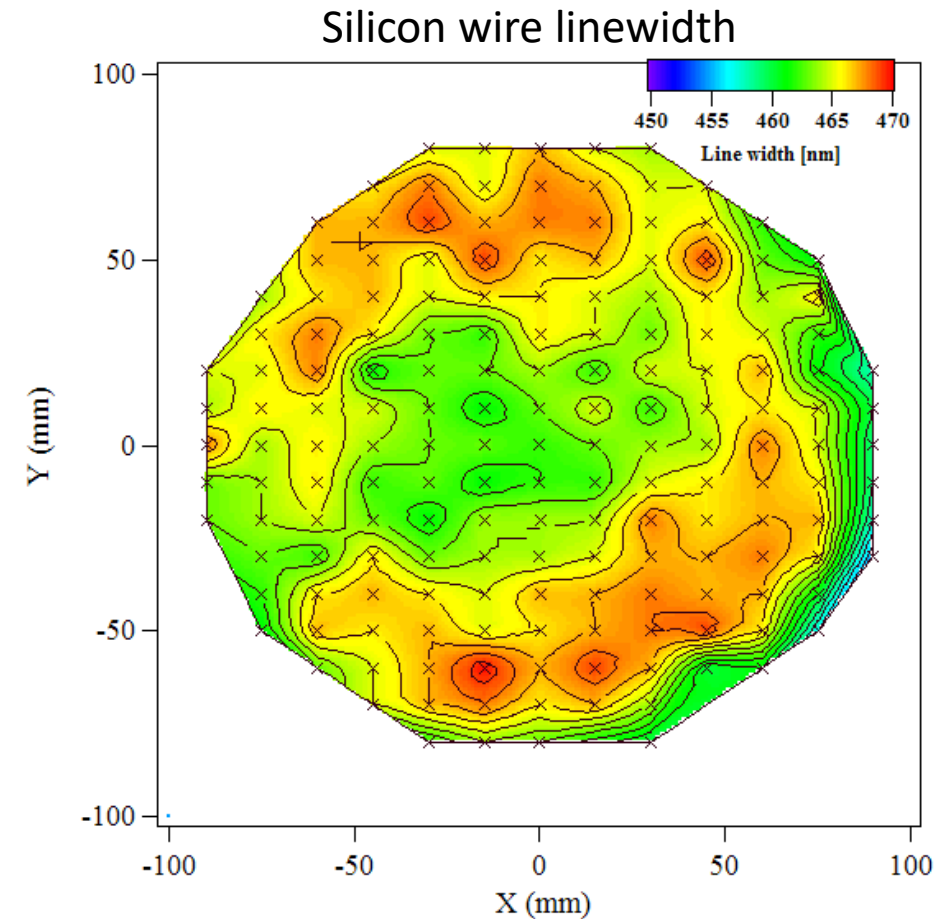
$$\frac{\partial \lambda}{\partial w} \approx 1 \text{ nm/nm}$$

wire height

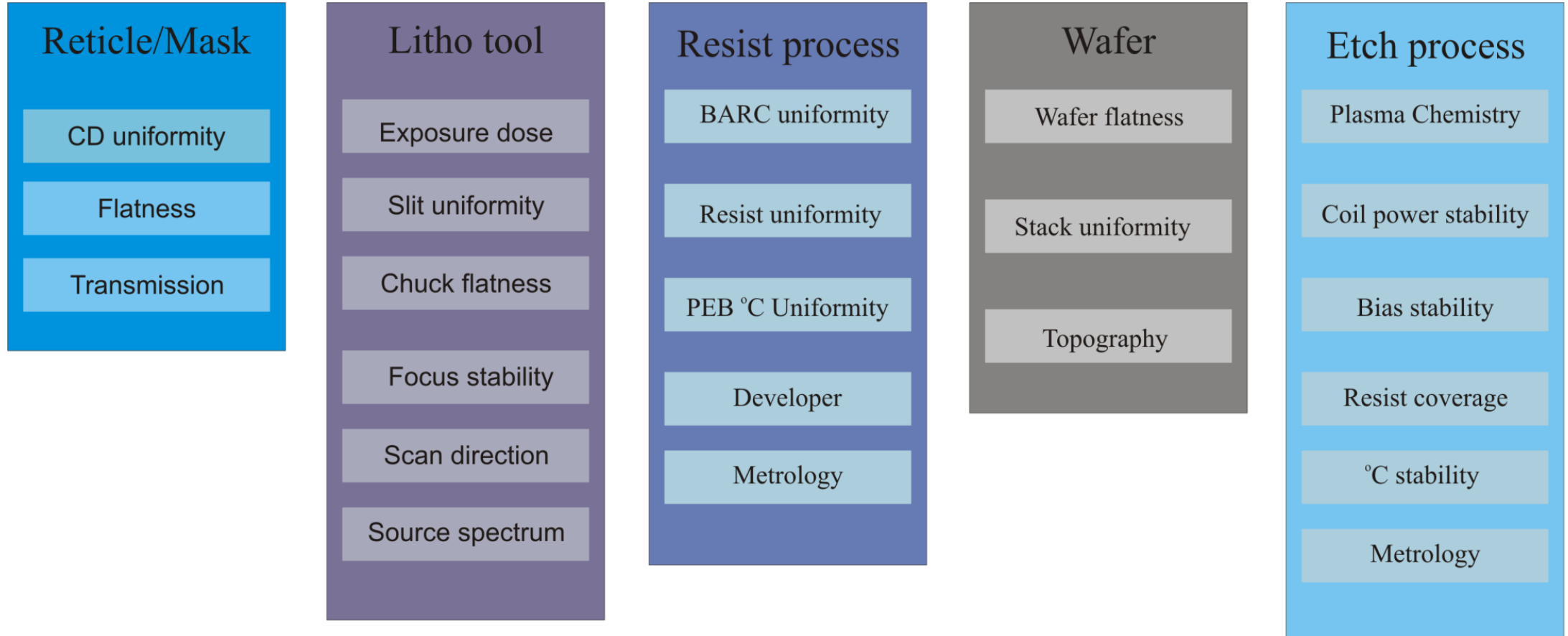
$$\frac{\partial \lambda}{\partial h} \approx 2 \text{ nm/nm}$$

temperature

$$\frac{\partial \lambda}{\partial T} \approx 0.08 \text{ nm/K}$$

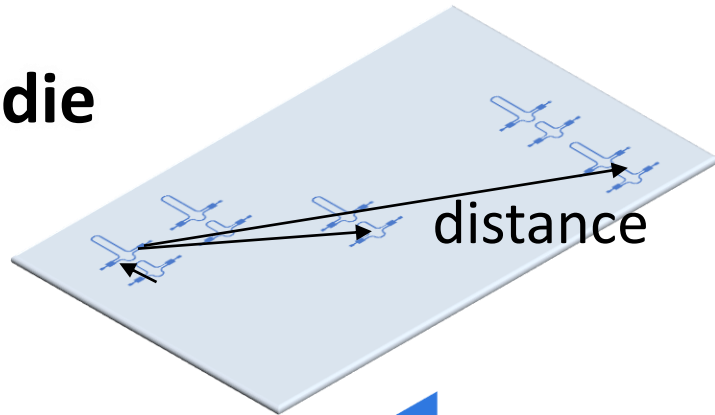


SOURCES OF NON-UNIFORMITY

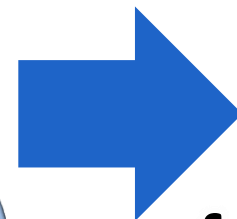
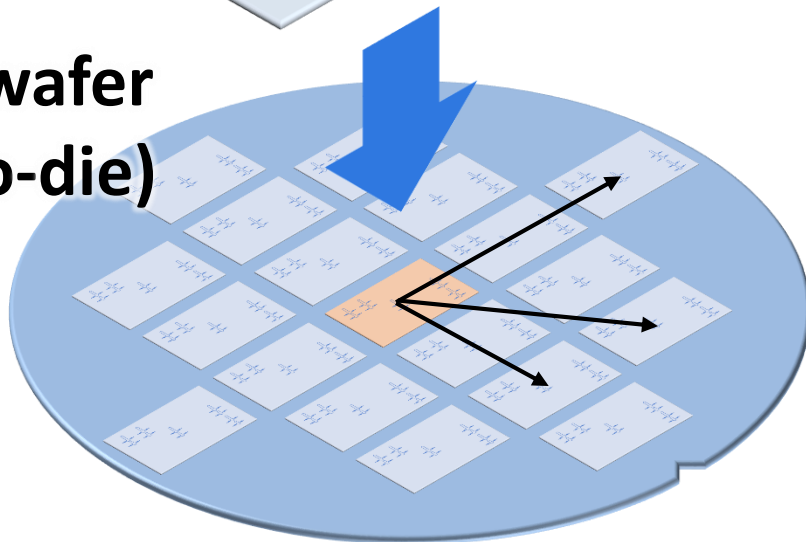


VARIABILITY EFFECTS WORK ON DIFFERENT SCALES

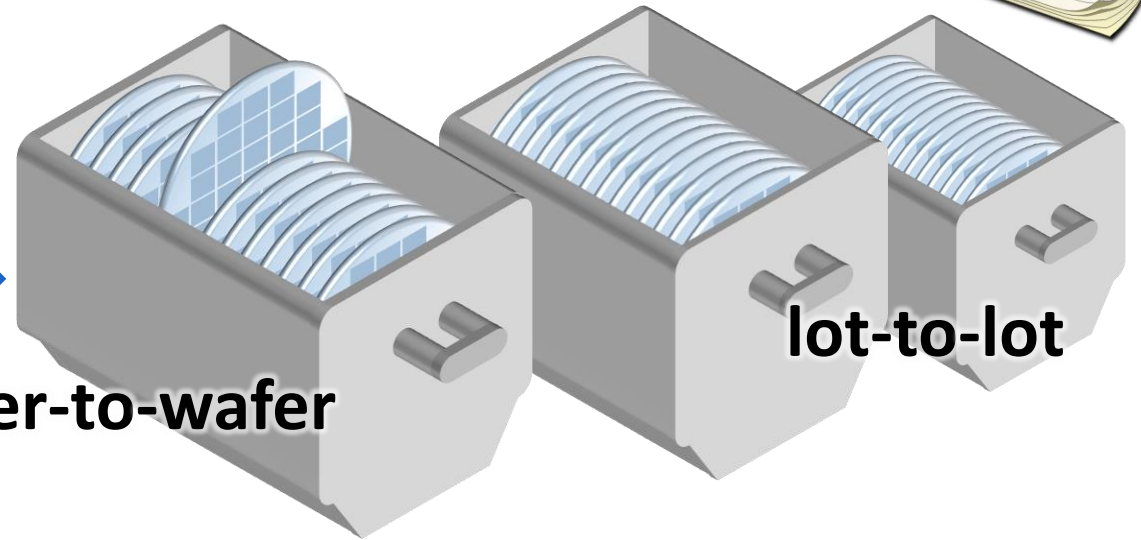
intra-die



**intra-wafer
(die-to-die)**

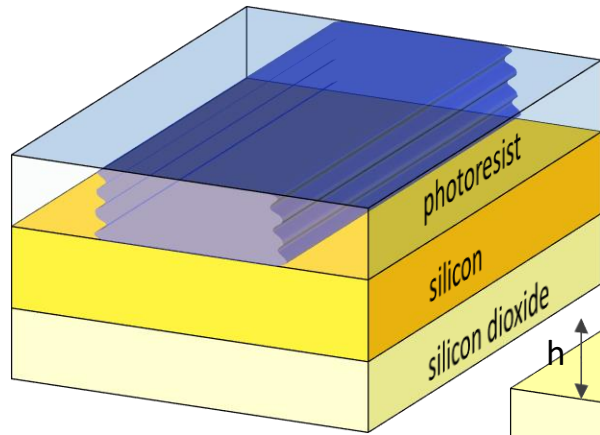


wafer-to-wafer



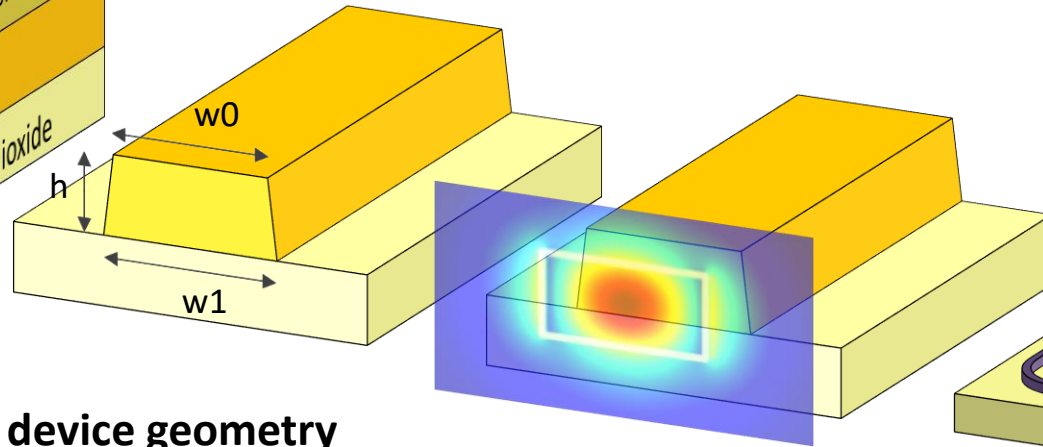
lot-to-lot

DESCRIBING VARIABILITY AT DIFFERENT LEVELS



process conditions

exposure dose
resist age
plasma density
slurry composition
...

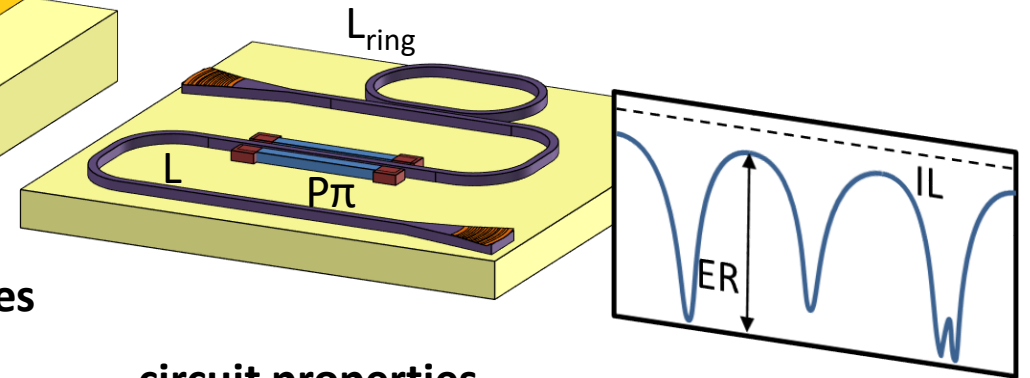


device geometry

line width
layer thickness
sidewall angle
doping profile
...

optical device properties

effective index
group index
coupling coefficients
center wavelength
...



circuit properties

optical delay
path imbalance
tuning curve
...

system performance

insertion loss
crosstalk
noise figures
power consumption
...

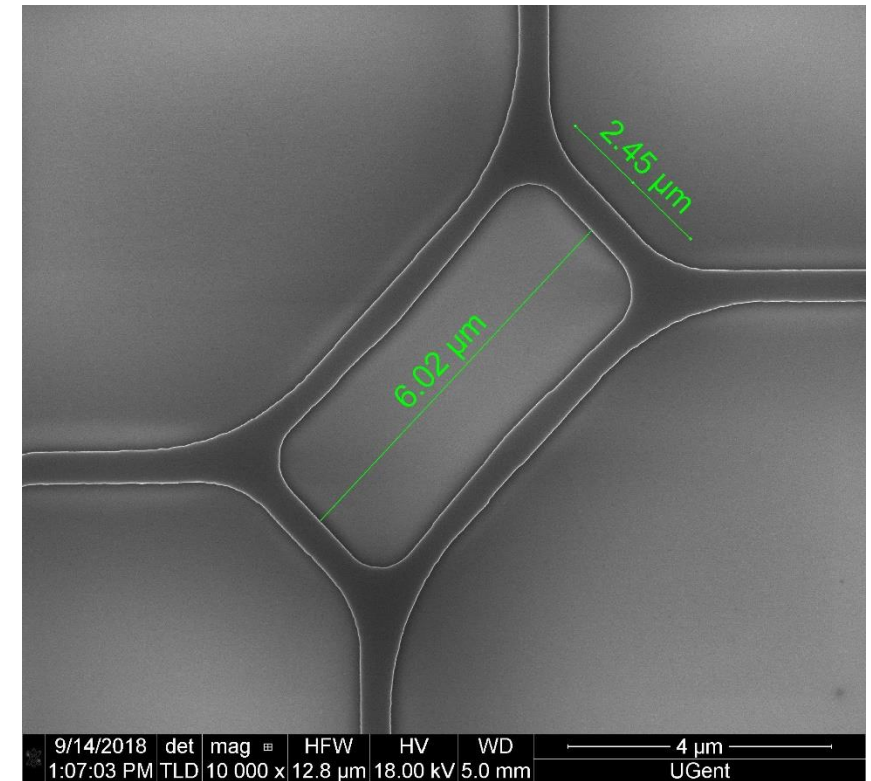
DESIGN WORKFLOW

- **Parameter Extraction & Spatial Variability**
 - Geometrical parameters
 - Waveguide width
 - Waveguide thickness
 - Optical parameters
 - Mapping of optical parameters to geometrical parameters
- **Layout-Aware Yield Prediction**

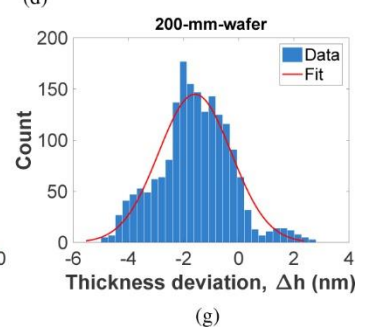
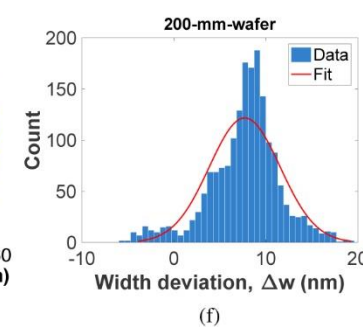
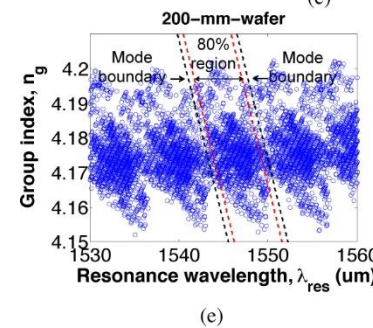
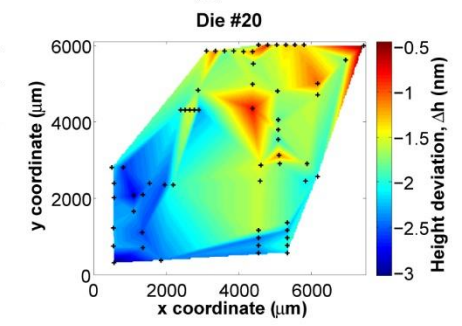
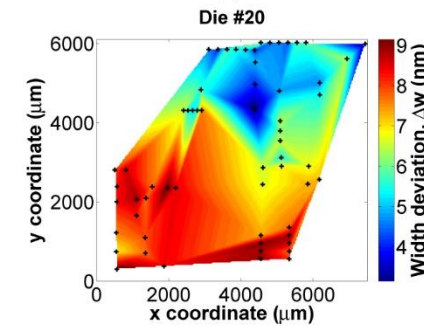
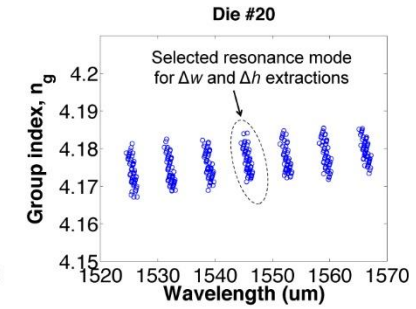
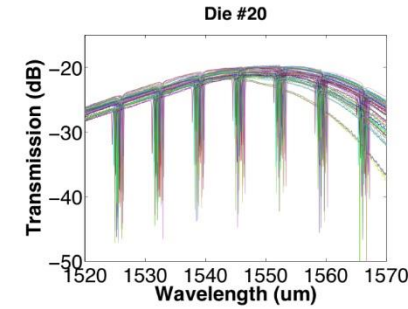
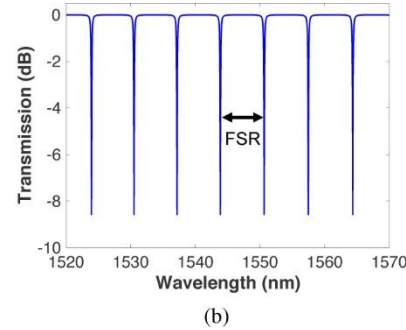
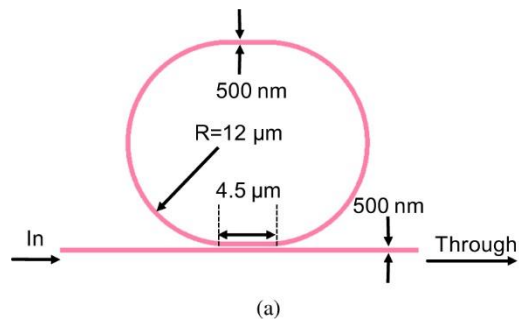
PARAMETER EXTRACTION & SPATIAL VARIABILITY

PARAMETER EXTRACTION

- Metrology measurements
 - Scanning electron microscope (SEM)
 - Atomic force microscope (AFM)
 - Time consuming ☹️
 - Expensive ☹️
 - Destructive ☹️
 - Extraction error (~nm) ☹️
 - Few places on the wafer/die ☹️
- Optical Measurements
 - Fitting of measurements to simulations
 - Mapping of optical parameters to geometric parameters
 - Smaller extraction errors (sub-nanometer) 😊
 - Non-destructive 😊
 - Many places over the wafer/die 😊

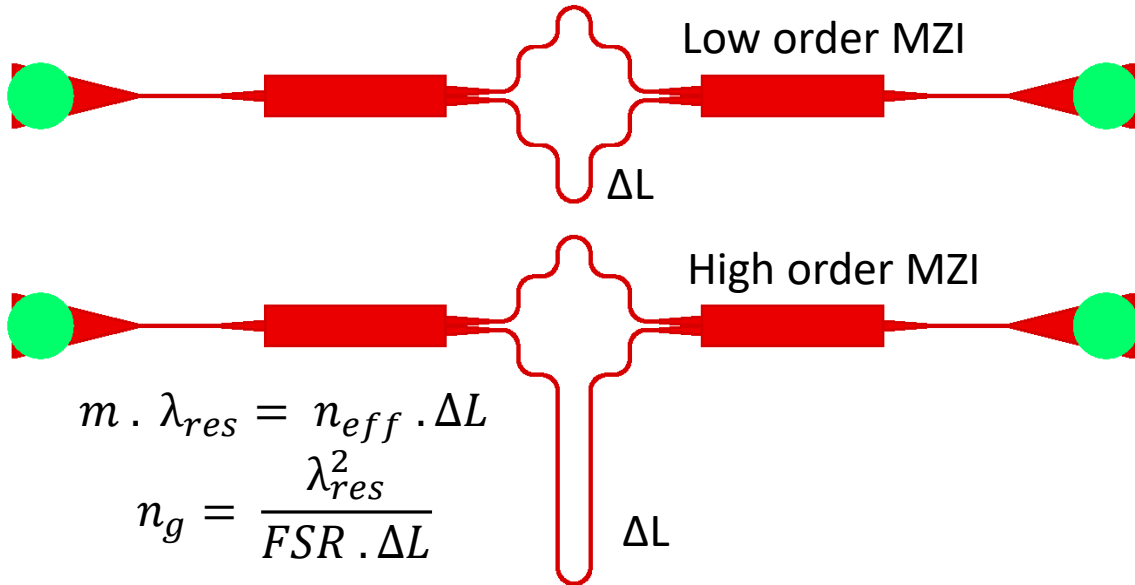


EXTRACTION - OPTICAL MEASUREMENTS OF RINGS



- Extract parameters (n_{eff}, n_g) using wafer scale measurements
- Link n_{eff}, n_g to width and thickness
- Cannot separate straight and bend waveguide

EXTRACTION - OPTICAL MEASUREMENTS OF TWO MZIs



Spectrum

- n_{eff}, n_g : Straight waveguide
- Length difference between two arms

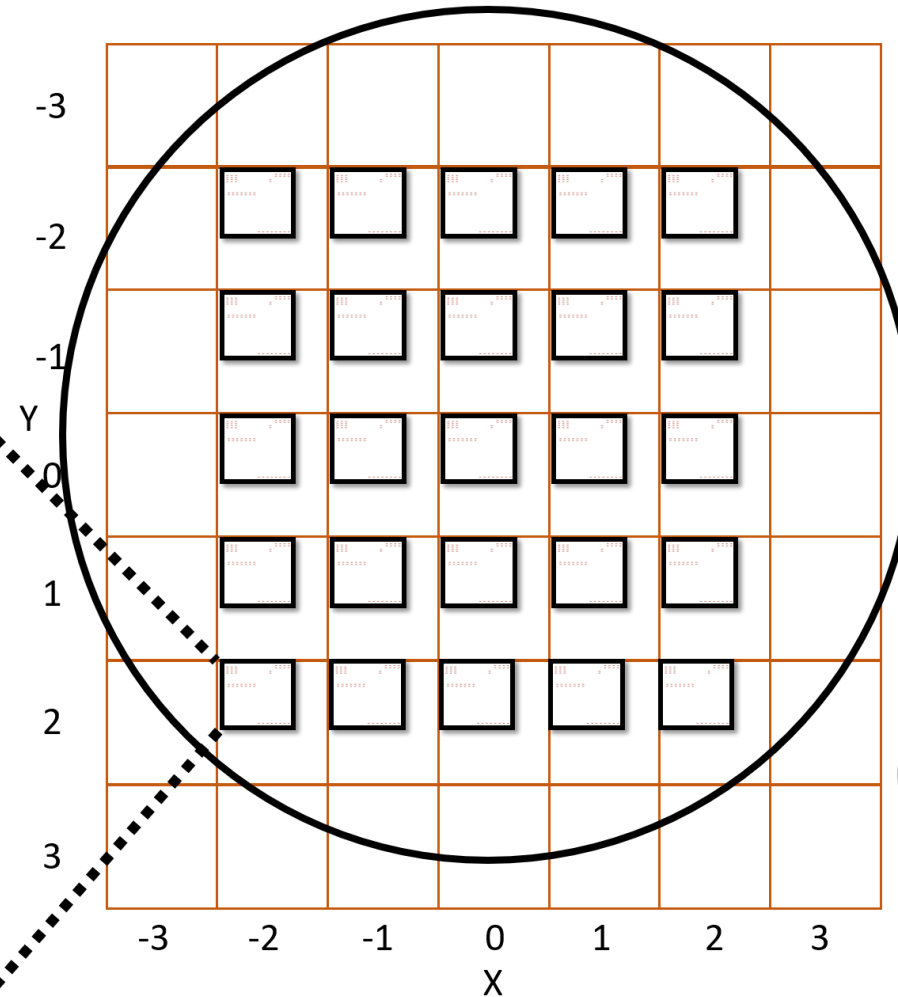
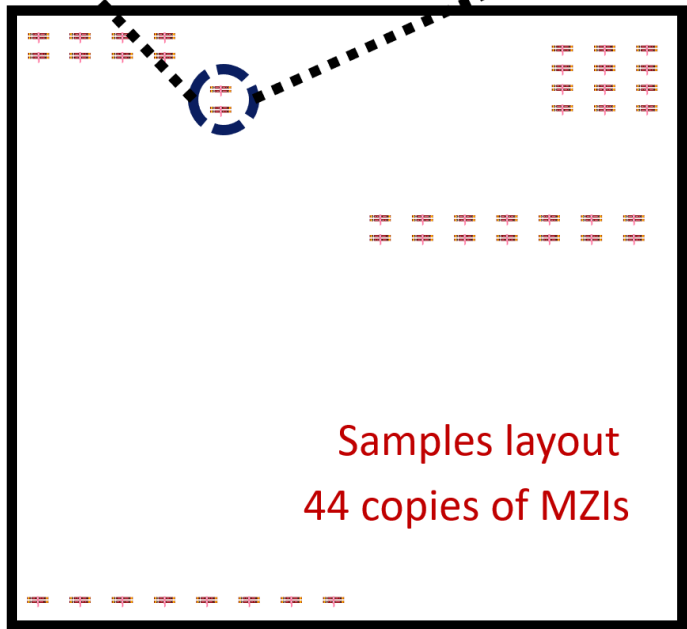
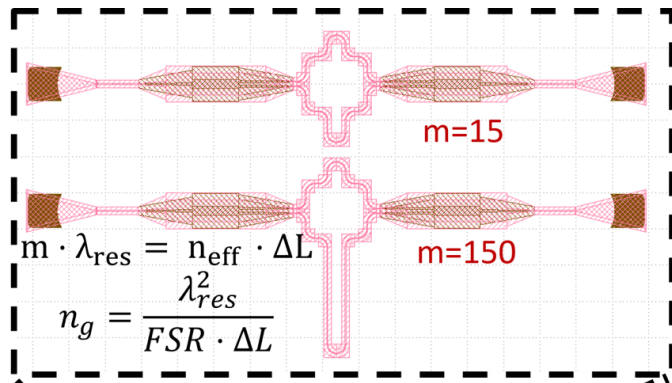
Low order

- Inaccurate extraction
- Tolerant to overall variation
- Set reference effective index

High order

- Accurate extraction of group index and effective index

MEASUREMENT SITES



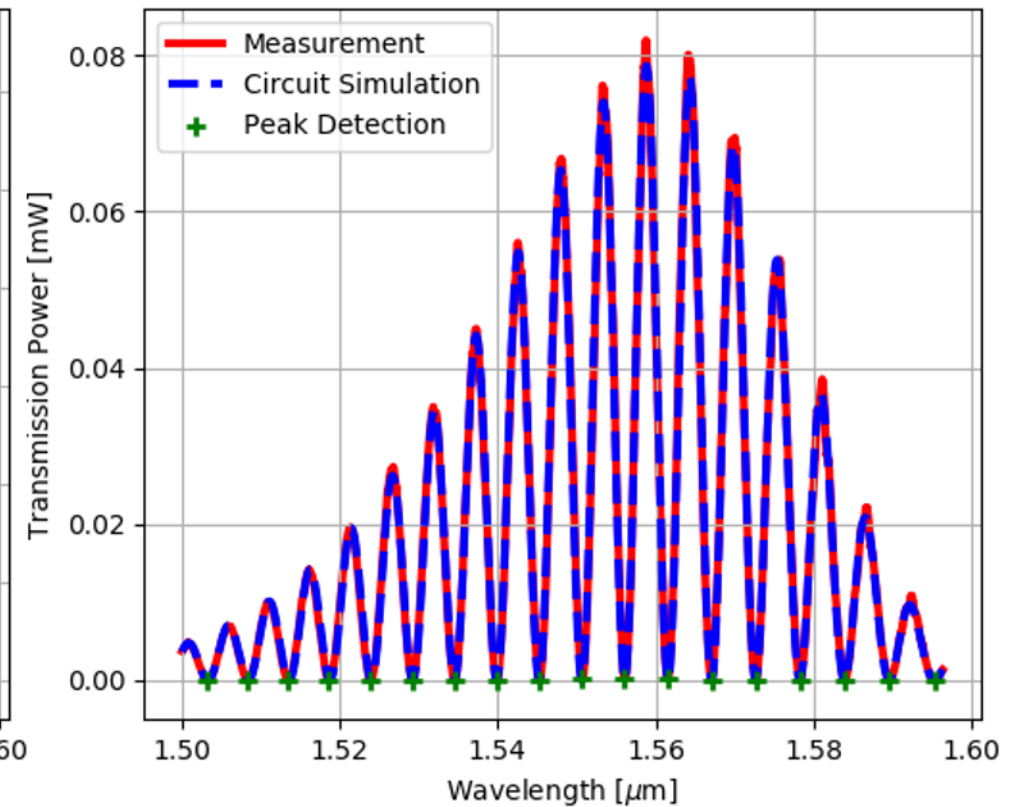
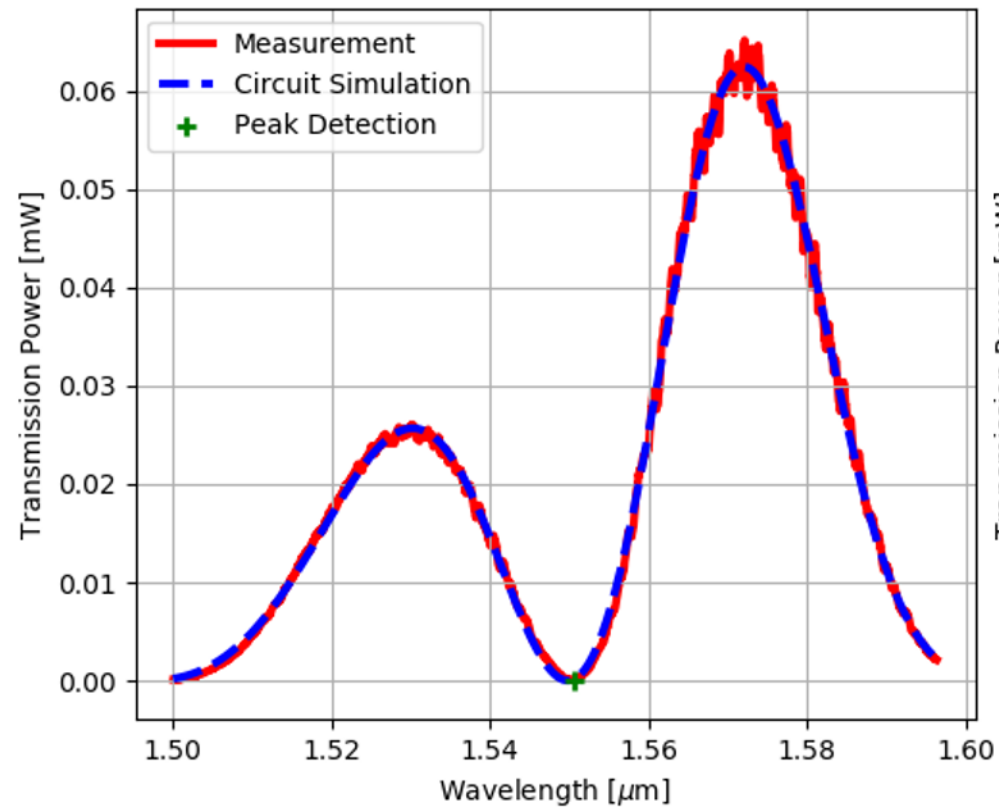
25 dies

44 copies of MZI
pairs per die

Obtain geometry parameters

$$(n_{eff}(\lambda_0), n_g(\lambda_0)) \xrightarrow{(w,t)=f(n_{eff}(\lambda_0), n_g(\lambda_0))} (w, t)$$

CURVE FITTING



$$\Rightarrow n_{eff}, n_g$$

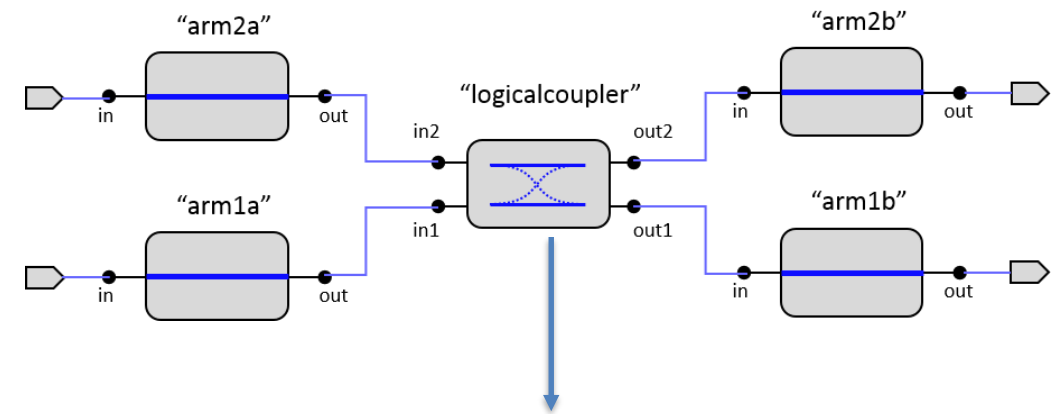
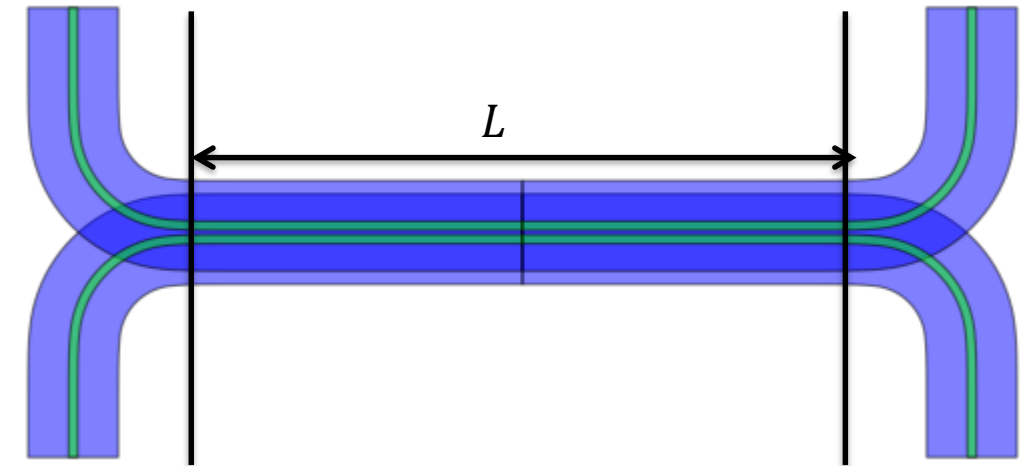
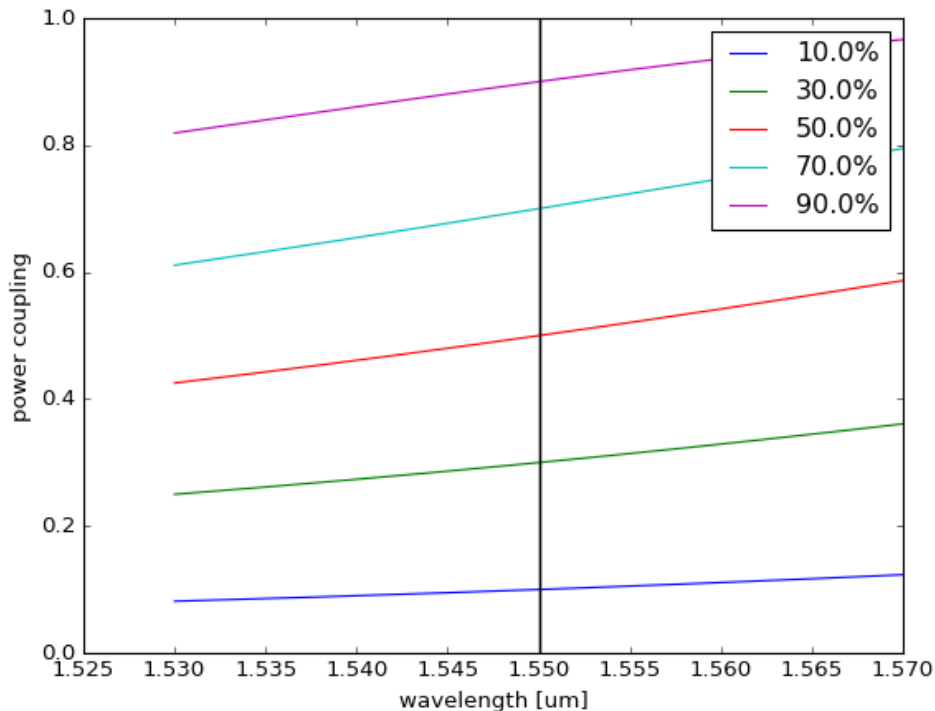
DIRECTIONAL COUPLERS

Treat coupler as circuit:

- 4 waveguides with their sensitivity to w, t
- 1 logical coupler with sensitivity to w, t

Coupling model = dispersive: straight + bends

Sensitivity calculated using mode solver + FDTD

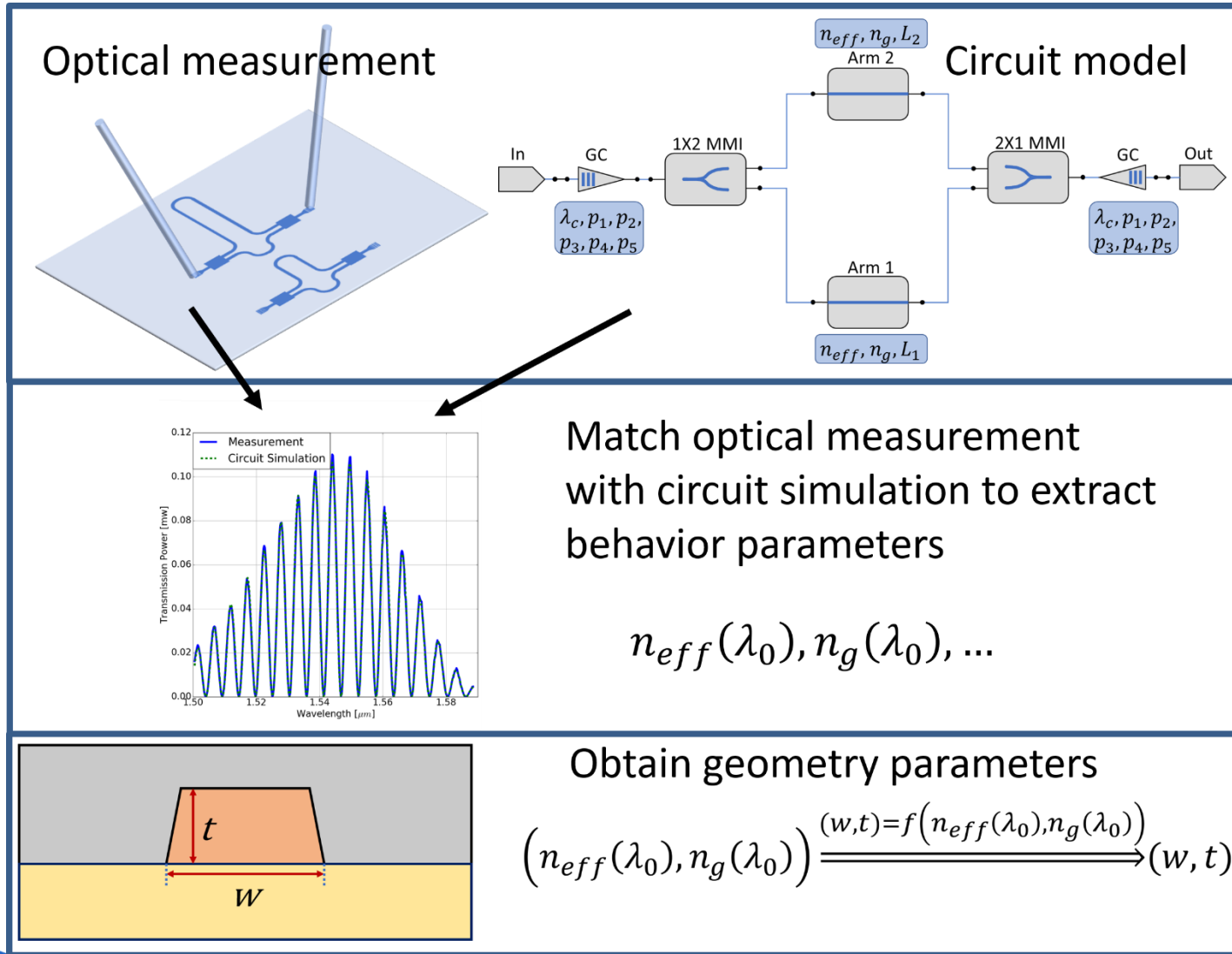


$$K = \cos^2(\kappa_0 + \kappa' L)$$

$$\kappa_0(\lambda) = \kappa_0(\lambda_0) + \frac{\partial \kappa_0}{\partial \lambda} (\lambda - \lambda_0) + \frac{1}{2} \frac{\partial^2 \kappa_0}{\partial \lambda^2} (\lambda - \lambda_0)^2$$

$$\kappa'(\lambda) = \kappa'(\lambda_0) + \frac{\partial \kappa'}{\partial \lambda} (\lambda - \lambda_0) + \frac{1}{2} \frac{\partial^2 \kappa'}{\partial \lambda^2} (\lambda - \lambda_0)^2$$

WORKFLOW TO EXTRACT GEOMETRY PARAMETERS



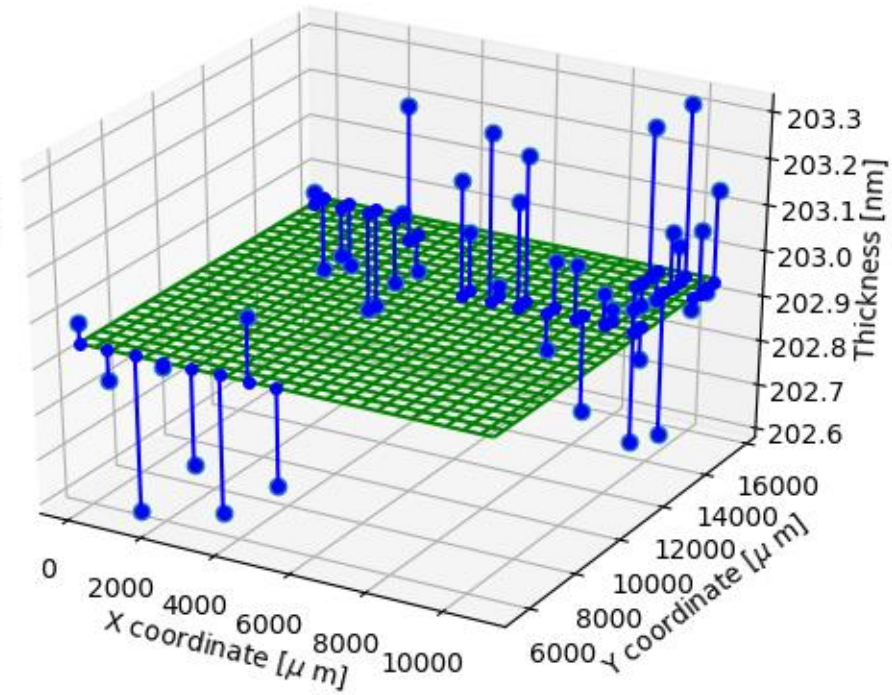
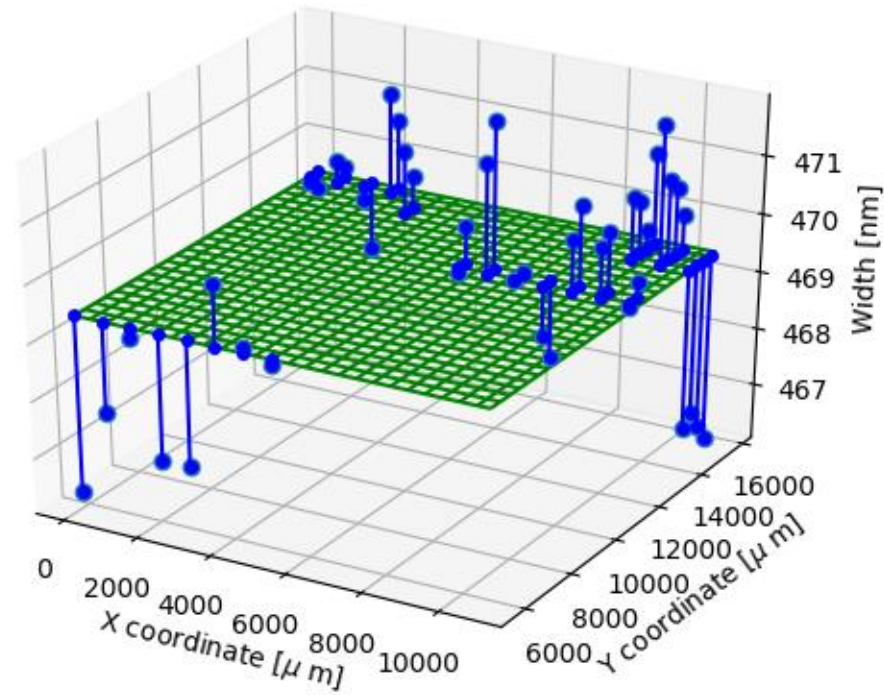
Extraction error of this experiment

Width: 0.37 nm

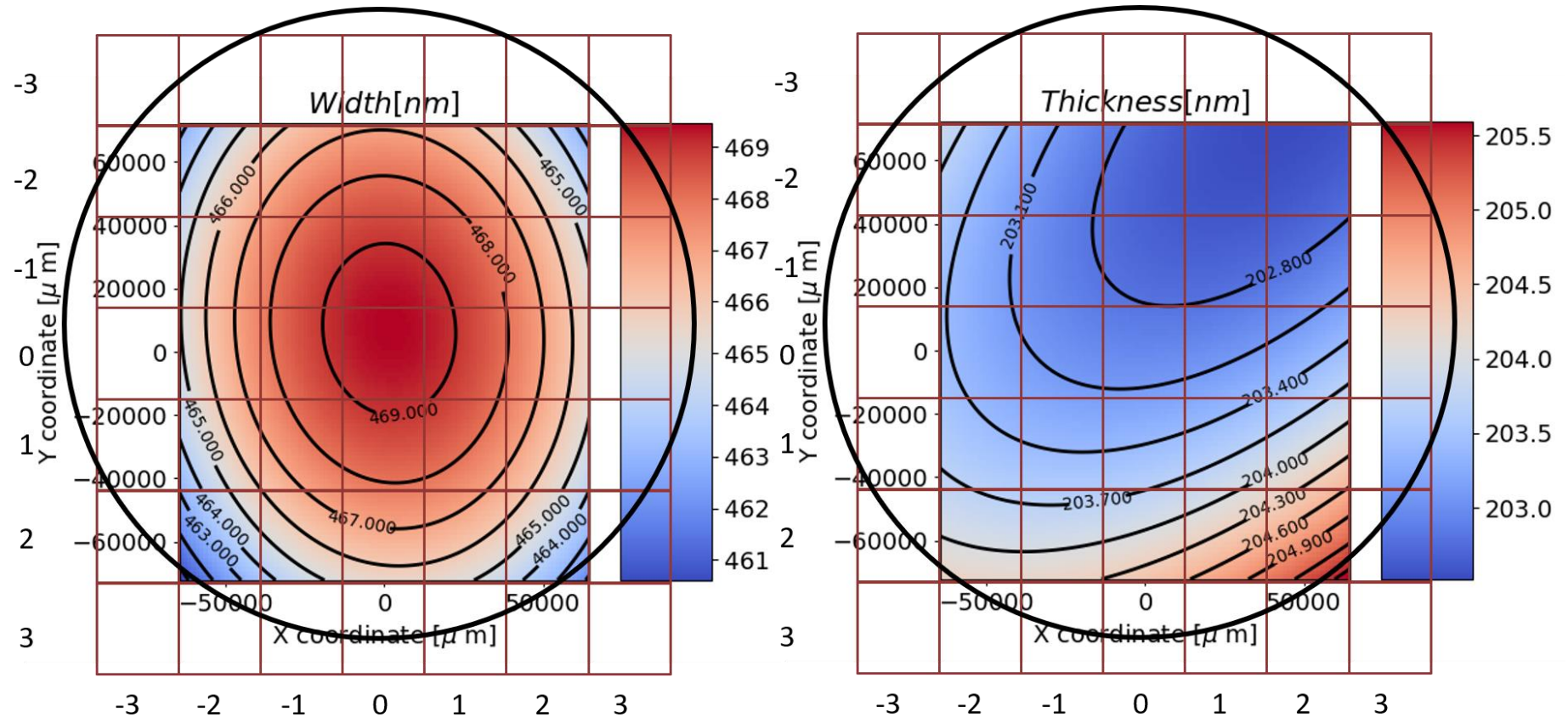
Thickness: 0.26 nm

Xing et al., Photonics Research 2018

SYSTEMATIC INTRA-DIE VARIATION

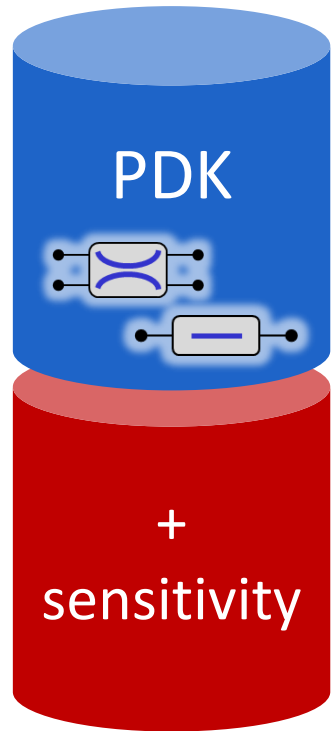


SYSTEMATIC INTRA-WAFER VARIATION

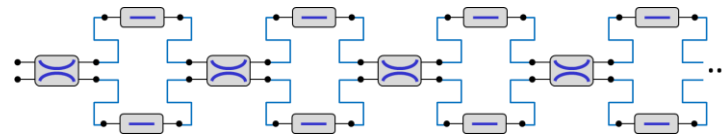


LAYOUT-AWARE YIELD PREDICTION

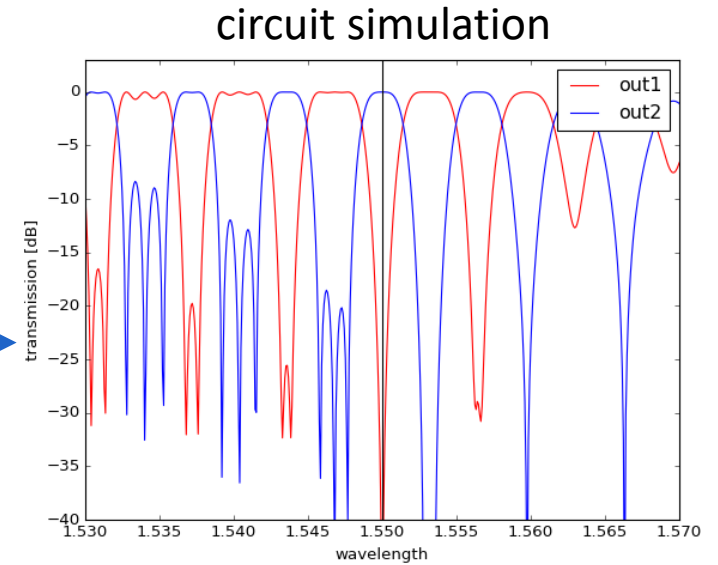
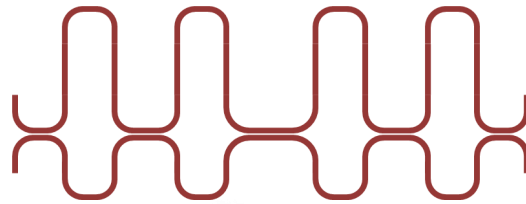
YIELD PREDICTION SCHEME



building blocks
+ models

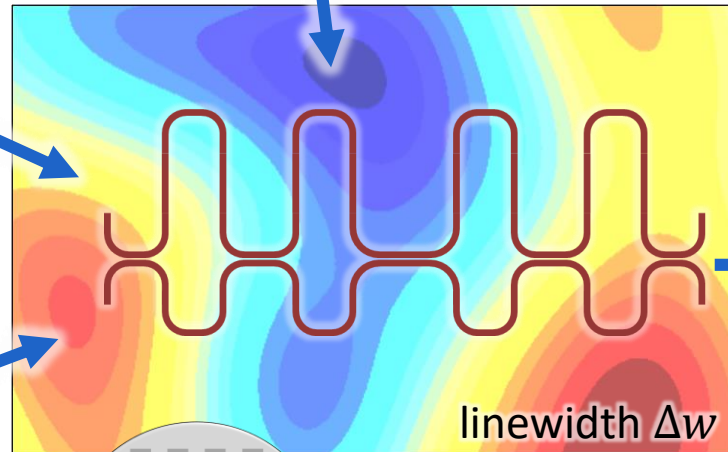


circuit netlist + layout

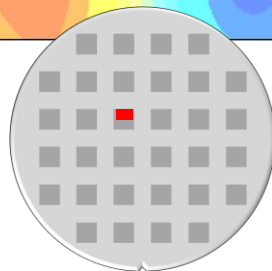


sensitivity of model
parameters
to fabrication
parameters

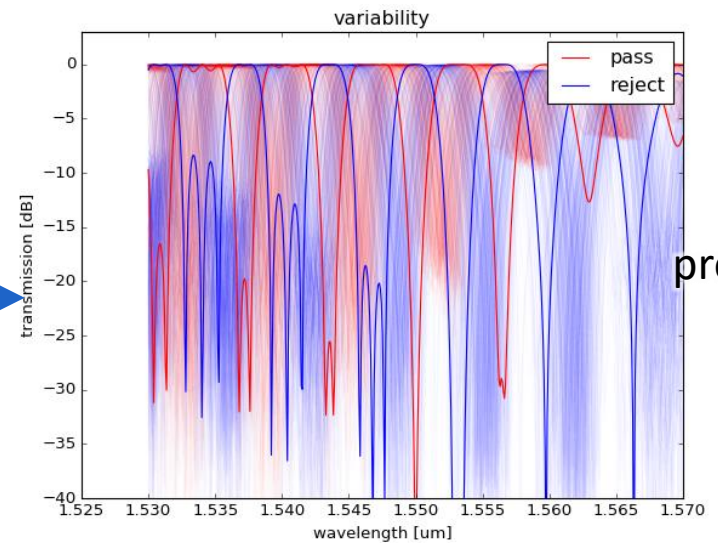
$$\frac{\partial n_{eff}}{\partial w}, \dots$$



wafer maps
(or model)
for fabrication
parameters

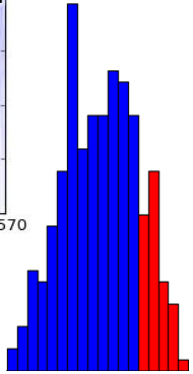


place circuit on wafer
and adjust model
parameters



Monte-Carlo on
dies and wafers

Yield
prediction



EXAMPLE: MZI LATTICE FILTER

Simple (but sensitive) building blocks

- directional couplers
- waveguide delay lines

FSR = 800GHz (~6.4nm)

Pass-band = 80GHz

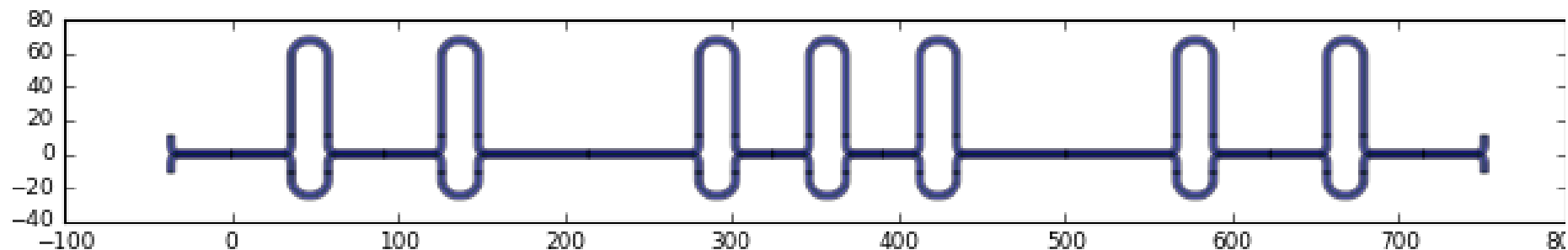
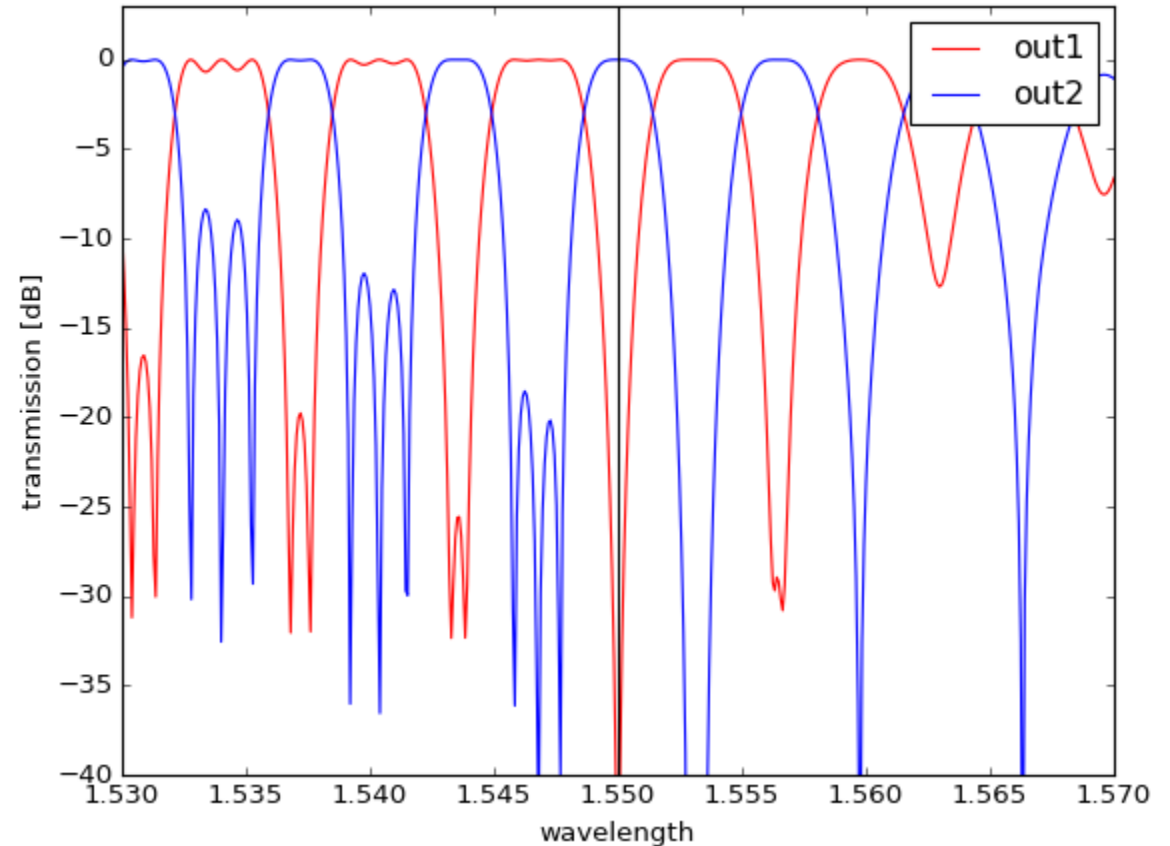
Guard band = 80GHz

Crosstalk (rejection) = -15dB

Center wavelength = 1.55 μ m

Long directional couplers

- dispersive
- very sensitive



WAFER MAPS: WIDTH AND THICKNESS

Most straightforward parameters

linewidth map

Simplex noise model

- $radius = 200\mu m$
- $amplitude = 1nm$

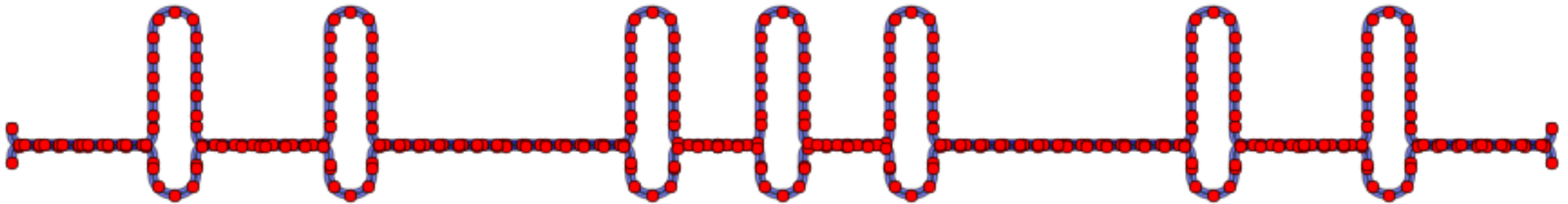
Thickness map (measured)

- $range = 213 - 219nm$

SAMPLING POINTS IN THE LAYOUT

All building blocks with a model will sample all variables (w, t)

- waveguides: n_{eff}, n_g
- logical couplers: $\kappa', \frac{\partial \kappa'}{\partial \lambda}, \frac{\partial^2 \kappa'}{\partial \lambda^2}, \kappa_0, \frac{\partial \kappa_0}{\partial \lambda}, \frac{\partial^2 \kappa_0}{\partial \lambda^2}$



- Sampling points are aggregated over the component: results in averaging, same as in fabricated devices

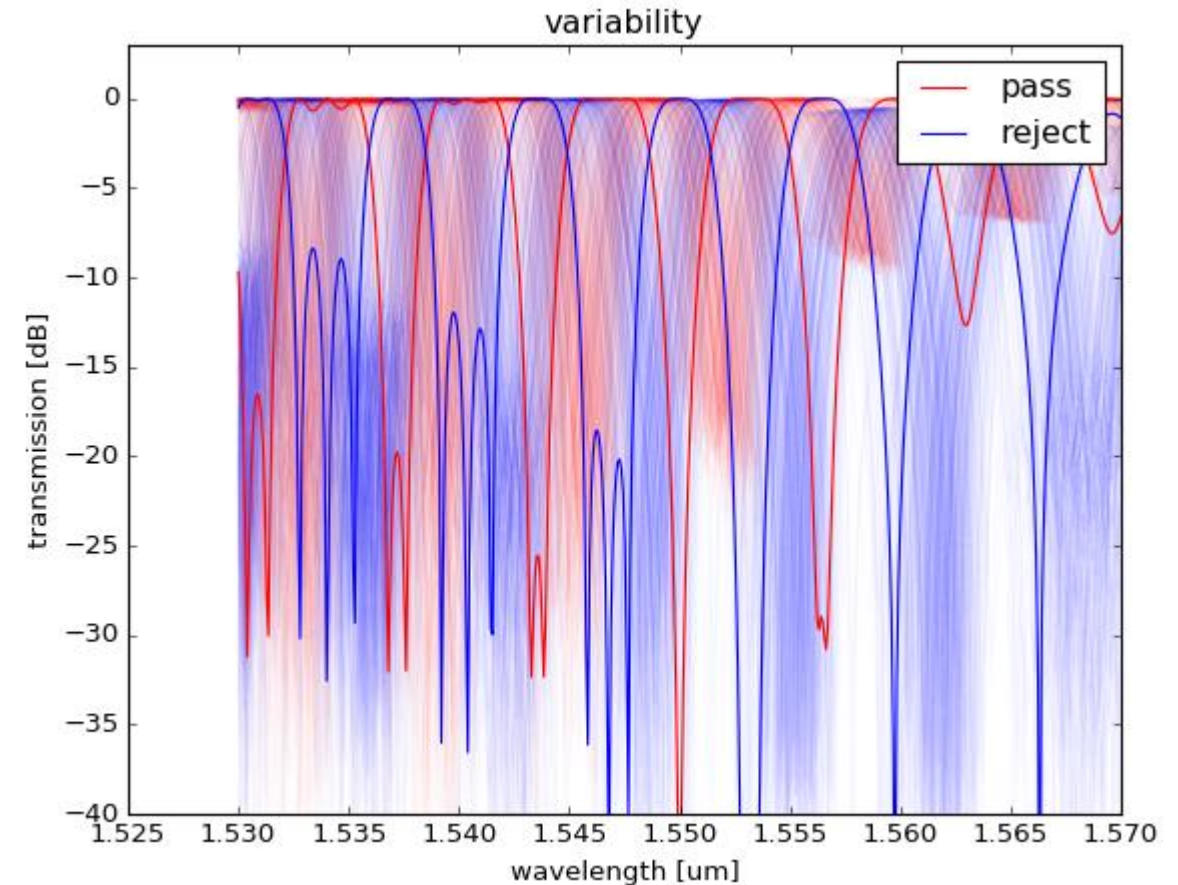
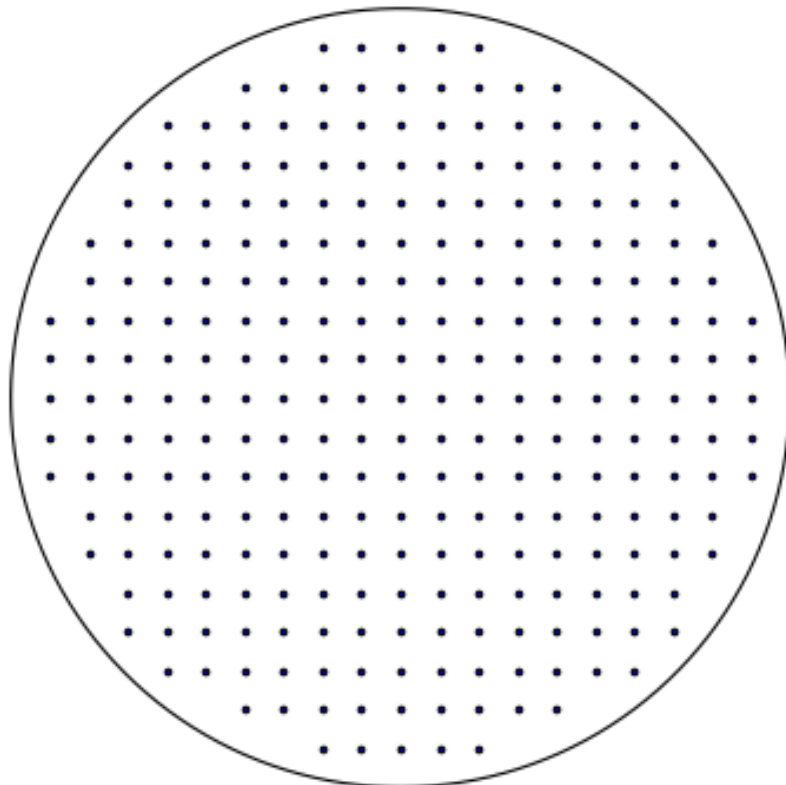
MONTE-CARLO SIMULATIONS OVER A WAFER

10mm spacing

277 dies on a wafer

Using CAPHE circuit simulator (Luceda)

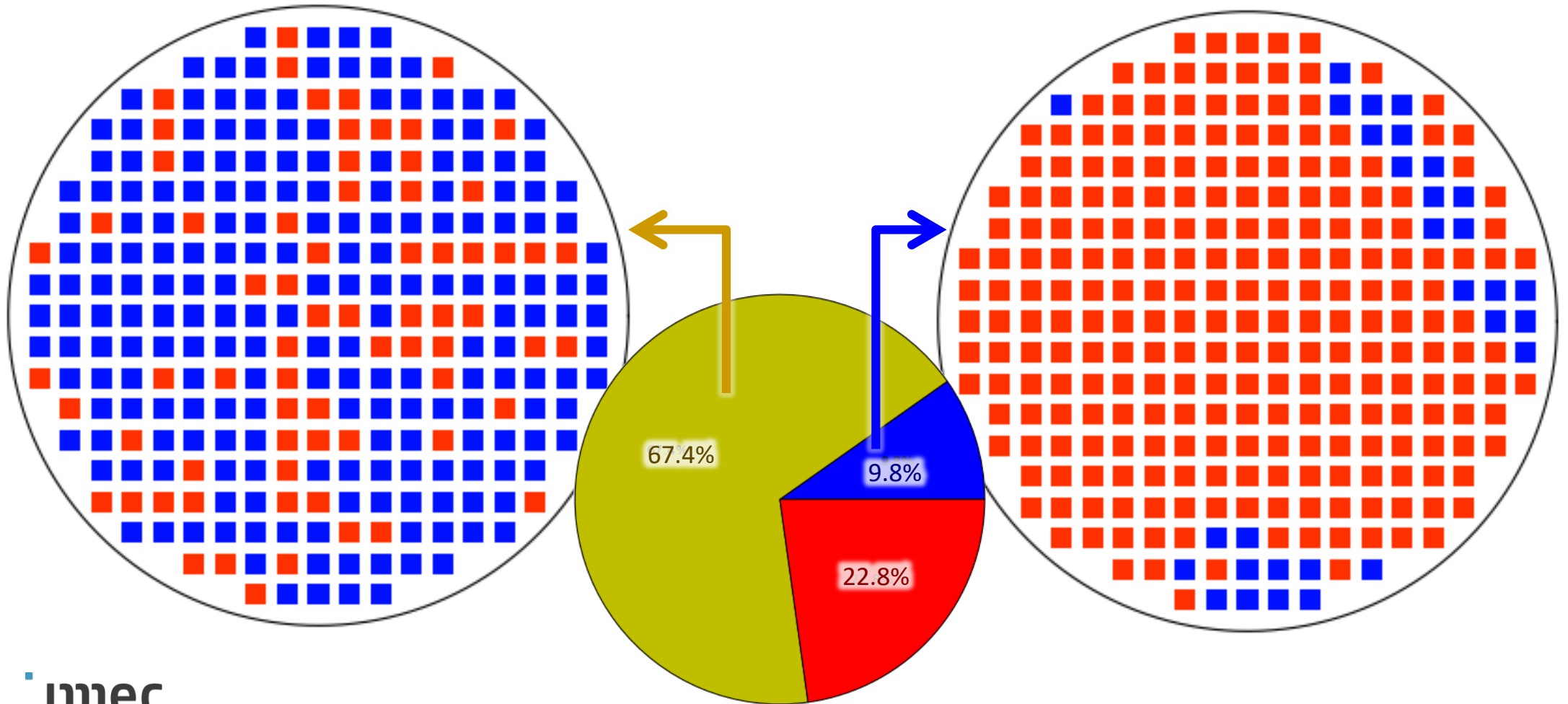
1000 wavelength points



YIELD MAPS

Without absolute wavelength spec

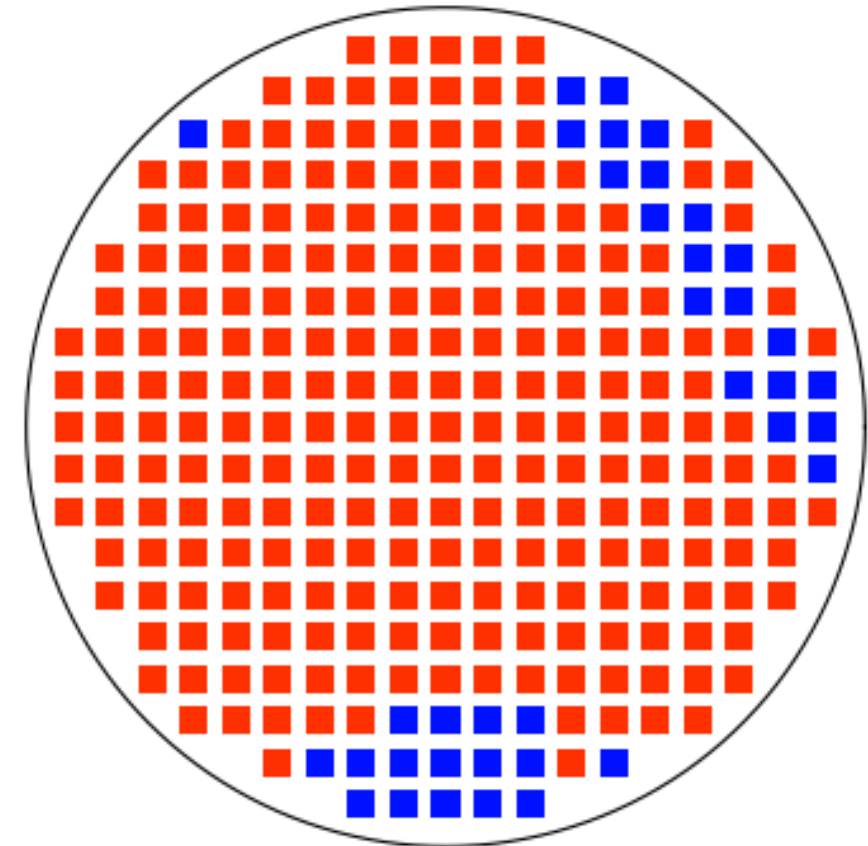
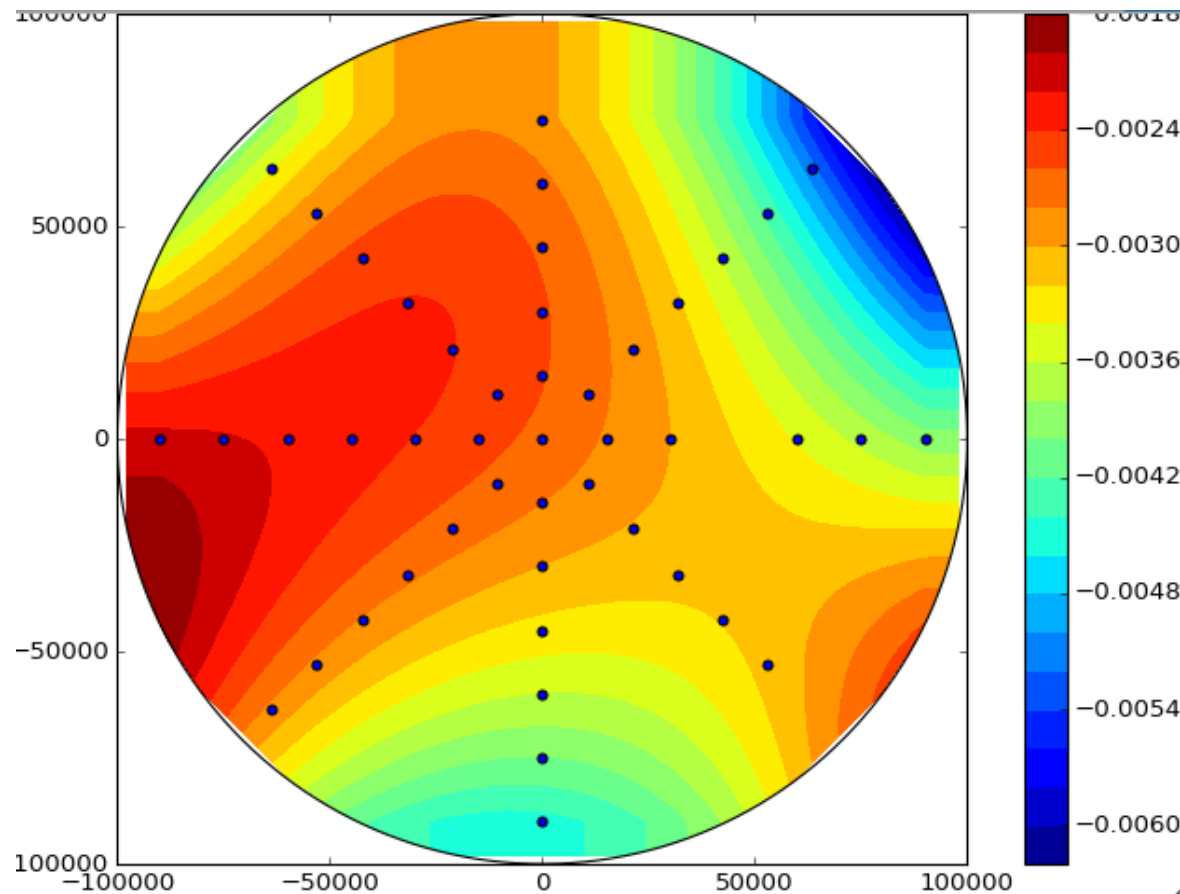
With absolute wavelength spec:
peak = $1.55\mu\text{m} \pm 80 \text{ GHz}$



PEAK WAVELENGTH: LARGELY AFFECTED BY THICKNESS

Wafer thickness map

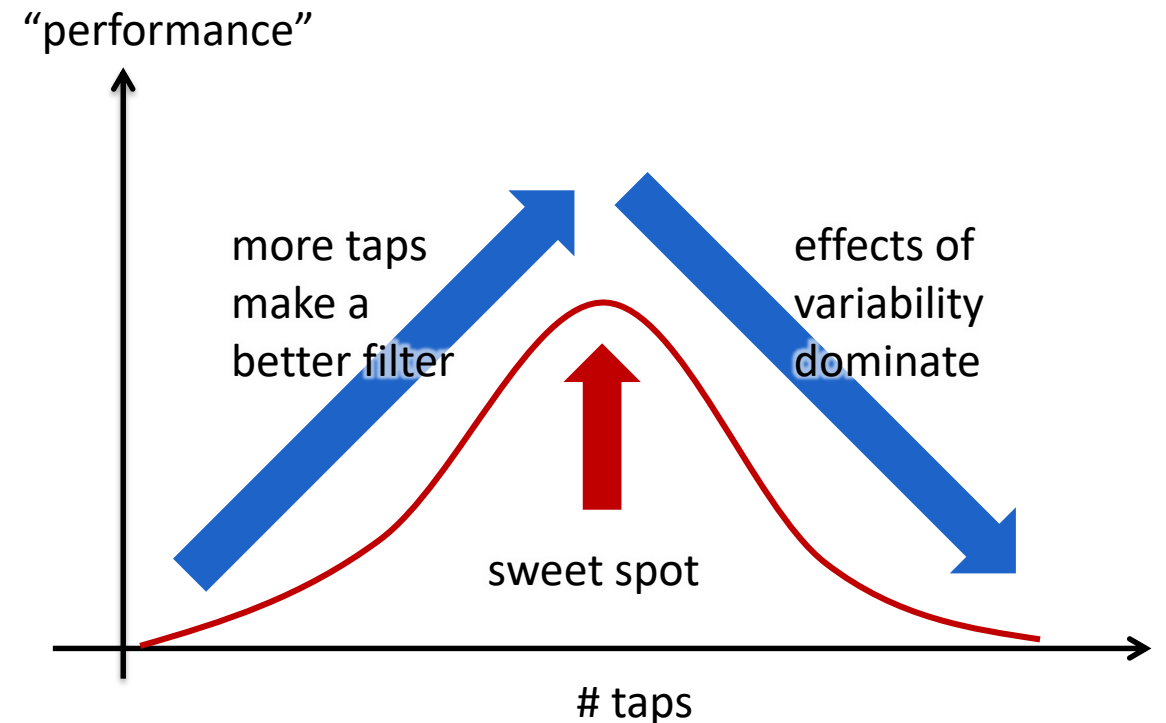
yield on wavelength spec



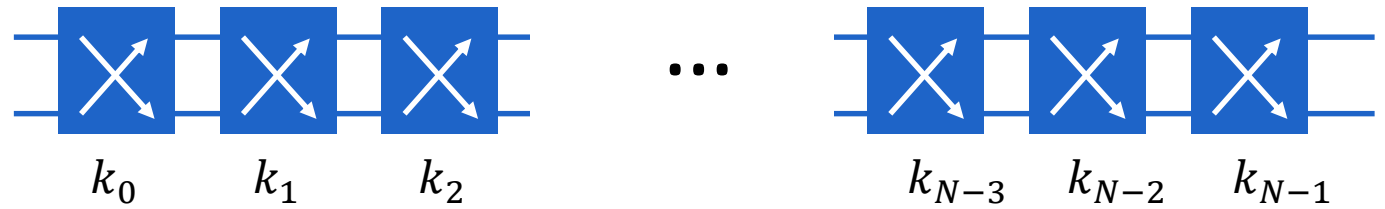
IMPROVE FILTER ?

Sweep number of taps

- More taps: better (box-like) filter
 - higher rejection ratio
 - sharper edges
- With variability
 - phase errors add up
 - coupler errors add up



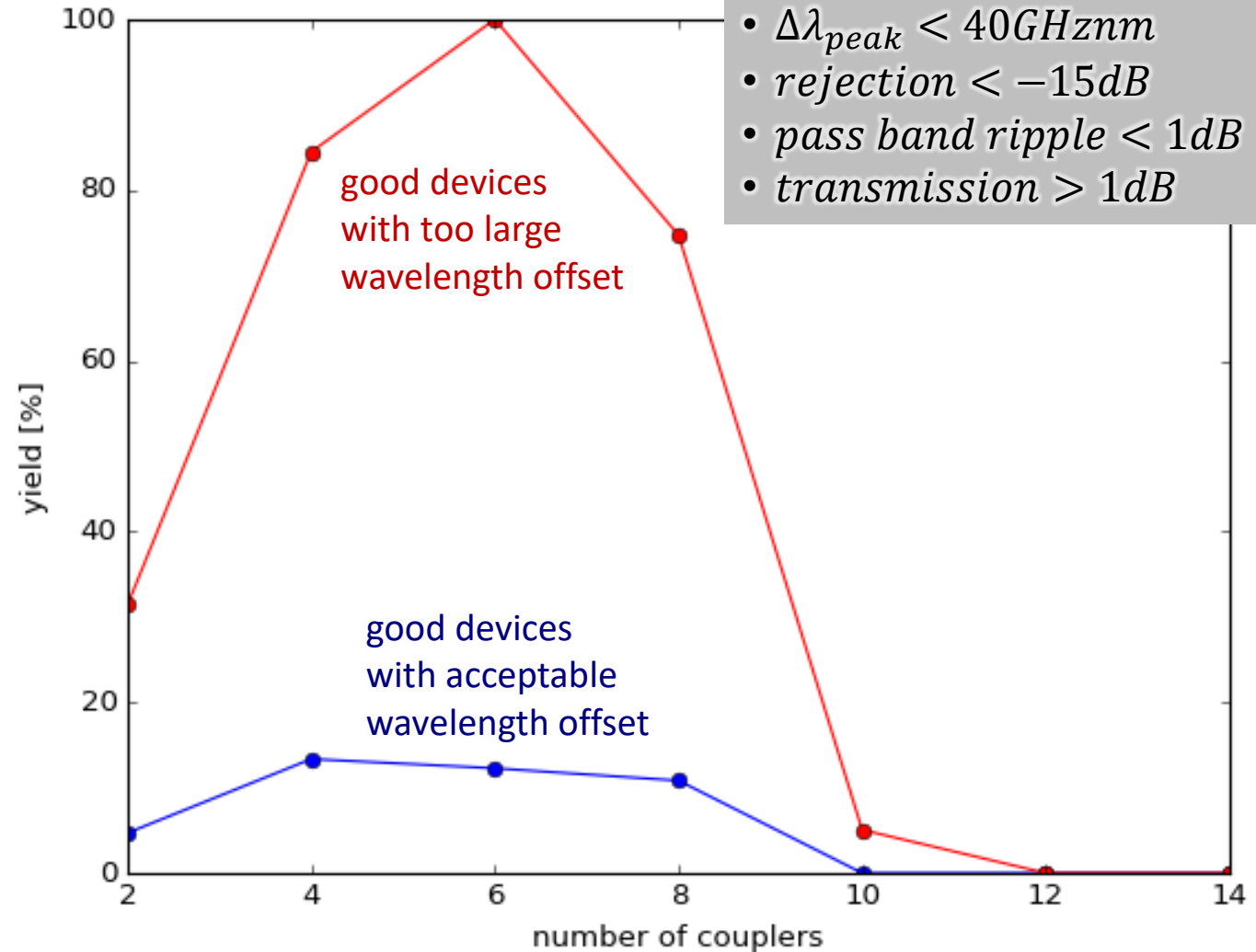
YIELD ANALYSIS



Increase number of taps:

- 2: not enough taps to reach rejection ratio
- 4-8: good quality
- 10-14: variability kills performance

Best: 6 taps



SUMMARY

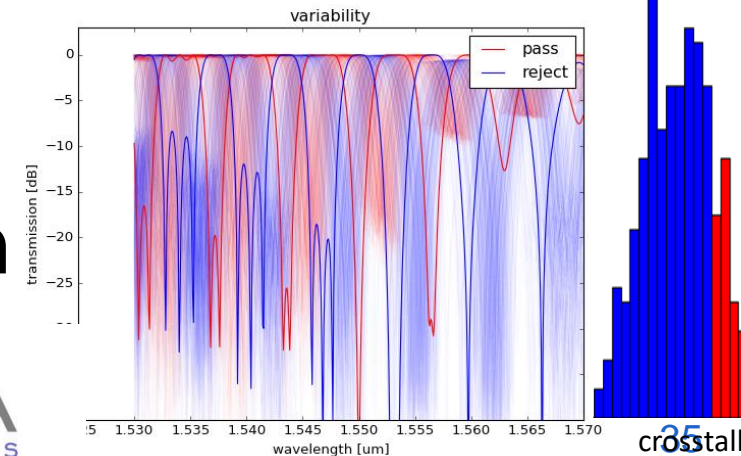
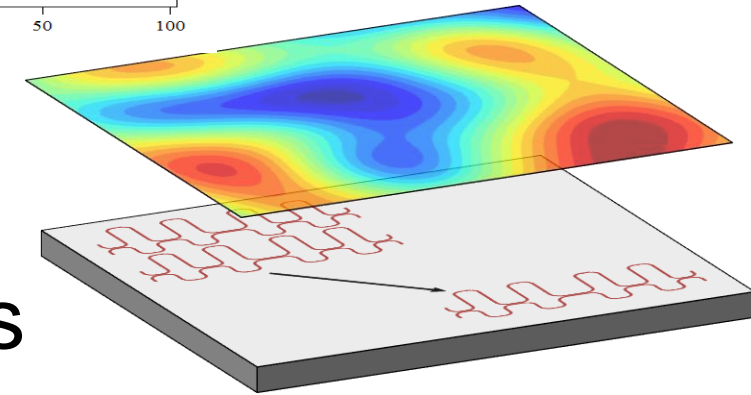
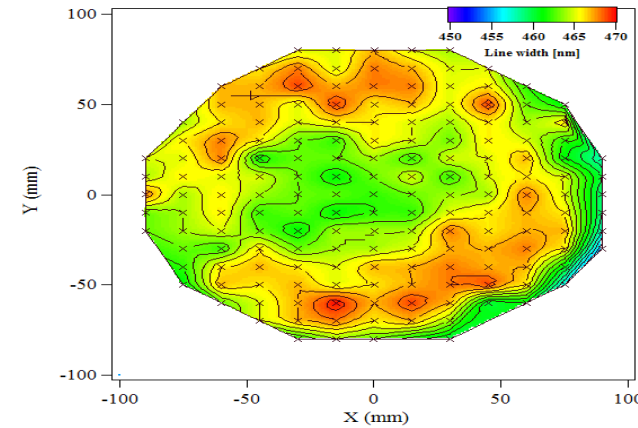
- Fabrication Imperfections

- Variability

- Variability determines yield in large circuits

- Variability should be considered at design stage

- Need layout awareness for yield prediction



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3RD SILICON PHOTONICS DESIGN COURSE

17-21 June 2019 – Ghent (Belgium)

- Gain fundamental understanding of silicon photonics design
- Circuits, components, simulation, layout, tape-outs, ...
- 5 days hands-on design labs
- Get a design fabricated and measured

<http://epixfab.eu/trainings/upcoming-trainings/spdc19/>

