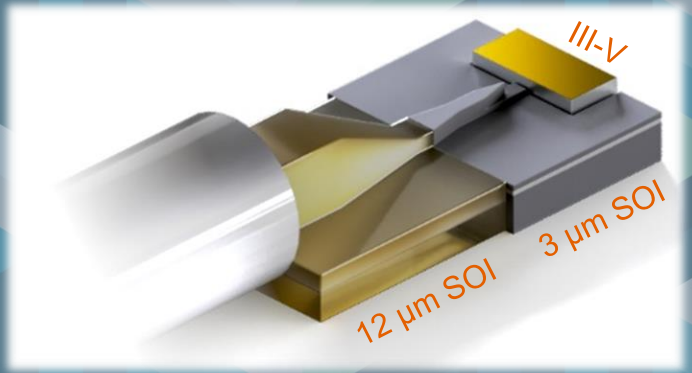


3 µm and 12 µm SOI platforms for optical interconnects and I/O coupling

Timo Aalto
Research Team Leader
VTT Technical Research Centre of Finland

The 5th International Workshop on Optical/Photonic Interconnects for Computing Systems

Florence, Italy, 29th March 2019

Other contributors and projects

- VTT: Matteo Cherchi, Mikko Harjanne, Fei Sun, Tapani Vehmas, Srivathsa Bhat, Markku Kapulainen, Giovanni Delrosso, Ari Hokkanen, Tomi Hassinen, Lauri Lehtimäki, Mikko Karppinen, Jyrki Ollila, Noora Heinilehto, Pentti Karioja

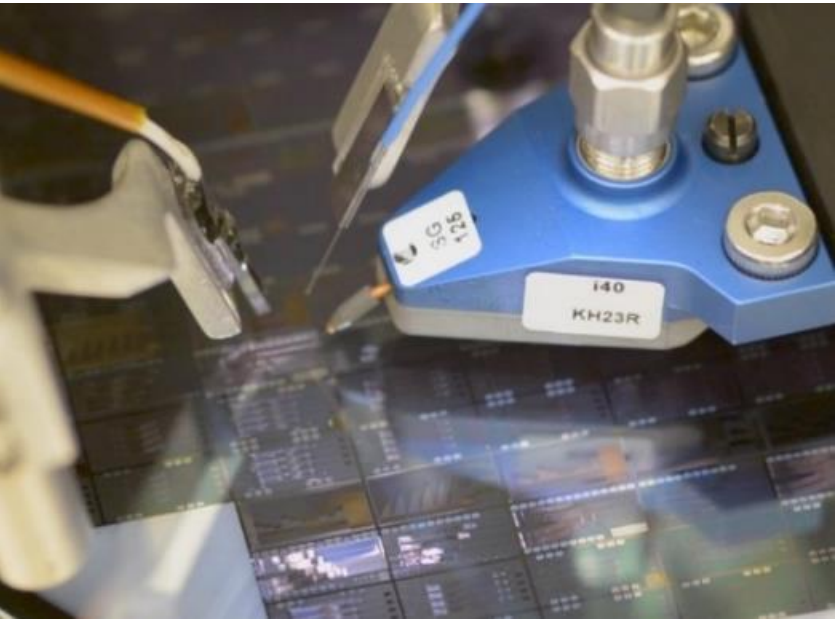
- Tampere University: Mircea Guina, Jukka Viheriälä
- Hamburg University of Technology:
  - Dirk Jalas, Nabeel Hakemi, Alexander Petrov, Manfred Eich
- Vertilas Gmbh: Christian Neumeyr
- Tyndall National Institute: Frank Peters, Robert Sheehan
- Scuola Superiore Sant'Anna: Antonio Malacarne

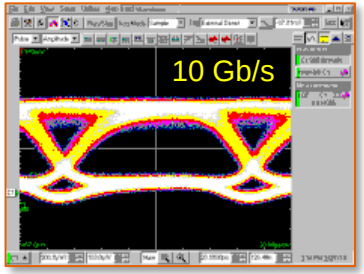
What is silicon photonics?

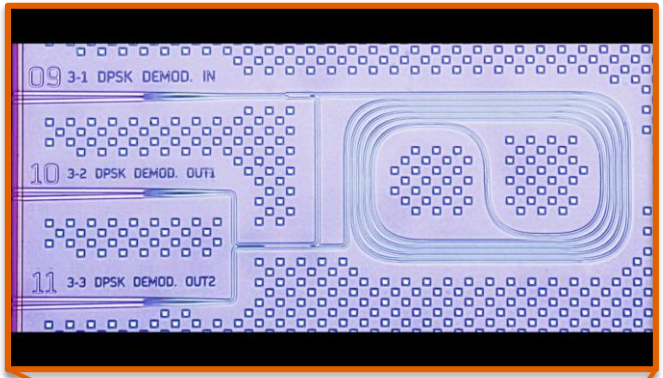
Generating, manipulating, guiding and using light

In Photonic Integrated Circuits (PICs)

processed on silicon-on-insulator (SOI) wafers

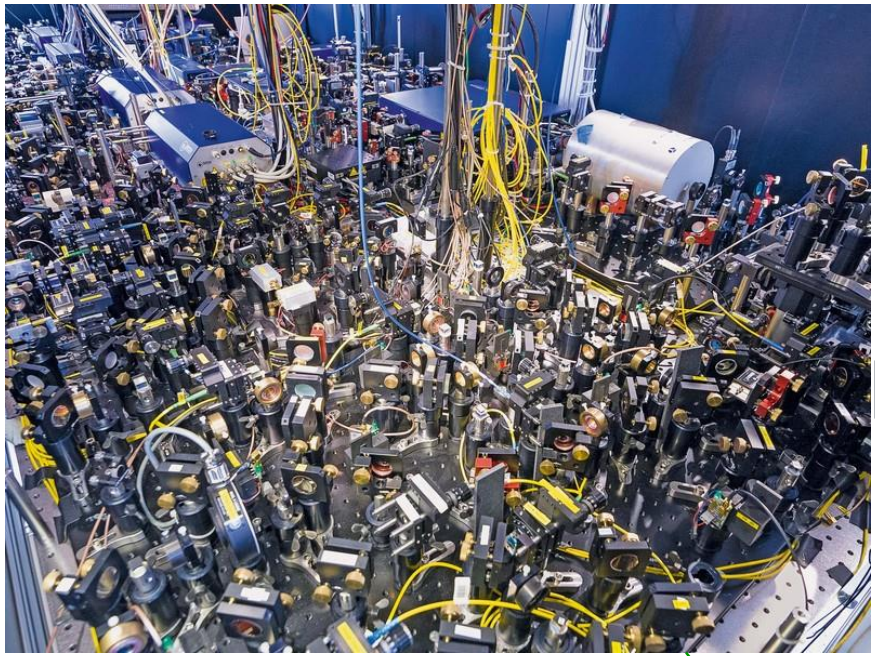






Photonics integration – Why?

- Discrete components don’t scale up well into complicated systems

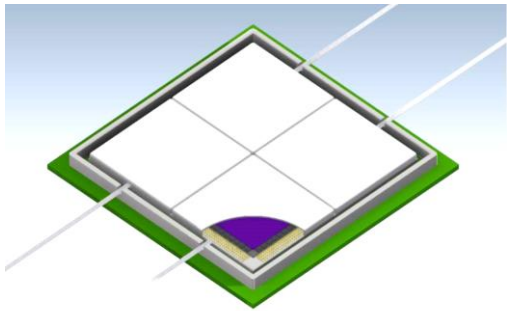


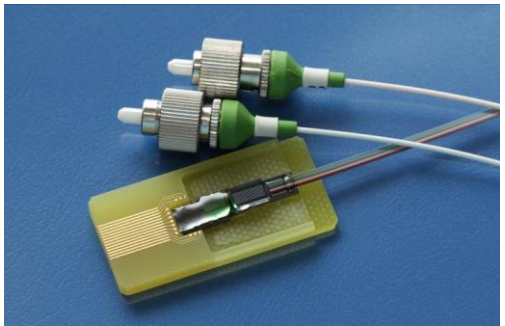
```
# endregion I/O ports

nline = n_vcsel_in.offset(0,0,-90).trim_to(nw).flip()
straight(dev, "WG_RIBS_ADD", nline, nline.trim_to(ne), 25.0)

# region mode-strippers
n_fiber_ins = [taper_wg(dev, INPUT_WG, node, RWG_2000) for node in n_fiber_ins]
n_fiber_ins = [straight_wg(dev, node.wg_def, node, node.trim_to(nw).offset(-850.0)) for no
n_fiber_ins = [taper_wg(dev, node.wg_def, node, RWG_2500) for node in n_fiber_ins]
n_fiber_ins = [rib_strip_wg(dev, node.wg_def, WG_2500, node) for node in n_fiber_ins]
# endregion mode-strippers

# region alignment waveguides
nar = n_fiber_ins[0]
nal = n_fiber_ins[3]

nar = line_wg(dev, nar.wg_def, nar, 200.0)
nal = line_wg(dev, nal.wg_def, nal, 200.0)
[nar, nal] = [taper_wg(dev, node.wg_def, node, WG_1875) for node in [nar, nal]]

nal = euler_wg(dev, nal.wg_def, nal, R_EULER_1310_L, 90)
nar = euler_wg(dev, nar.wg_def, nar, R_EULER_1310_L, -90)

namid = nal.offset(abs(nal - nal.trim_to(nar)) / 2.0

nodes = mmi_2x2_wg(dev, WG_3000, config.strip

node = taper_wg(dev, WG_3000, nodes[0], WG_18
straight_wg(dev, WG_1875, nal, node.flip())

node = taper_wg(dev, WG_3000, nodes[2], WG_1875)
straight_wg(dev, WG_1875, nar, node.flip())

nal = taper_wg(dev, WG_3000, nodes[1], WG_1875)
nar = taper_wg(dev, WG_3000, nodes[3], WG_1875)

nal = euler_wg(dev, nar.wg_def, nal, R_EULER_1310_L, 90)
nar = euler_wg(dev, nal.wg_def, nar, R_EULER_1310_L, -90)
[nar, nal] = [taper_wg(dev, node.wg_def, node, WG_2500) fo
[nar, nal] = [strip_rib_wg(dev, node.wg_def, RWG_2500, node)
                                                    nar, nal]]
```

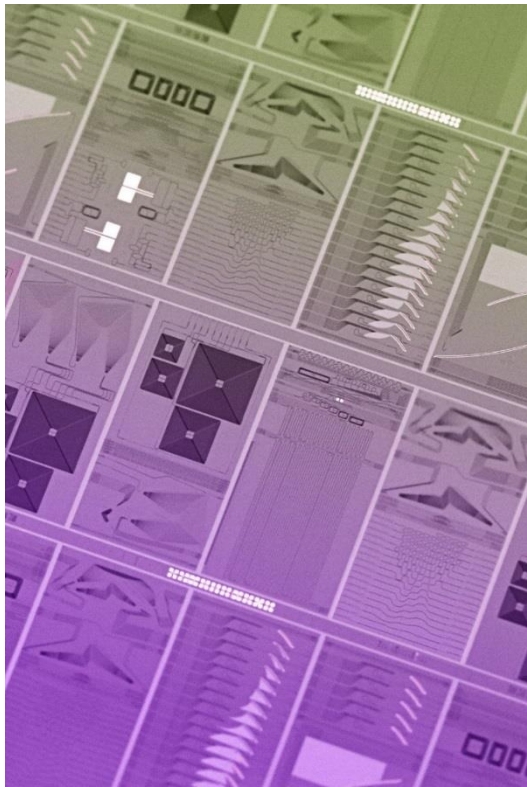
Ludwig-Maximilians-University – Munich
https://www.quantum-munich.de/media/nice-photos

Benefits of photonic integrated circuits

- Smaller **size**
- Smaller **weight**
- Smaller **power consumption**
- Smaller **cost** (in volume manufacturing)
- Better optical **performance**
  - Lower coupling losses
  - Higher bandwidth



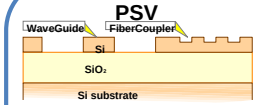




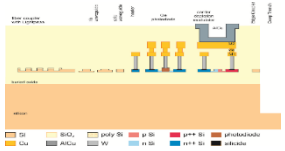
Many open access Si photonics platforms

imec

PSV



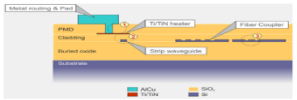
ISIPP50G



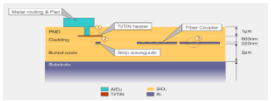
220 nm SOI

leti

Passive + heaters

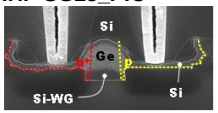


Si310-PH

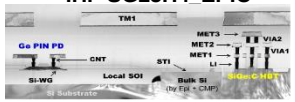


310 nm SOI

IHP SG25_PIC



IHP SG25H4_EPIC



Photonic BiCMOS

220 nm SOI

VTT

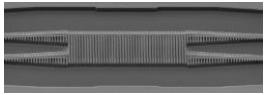
Passives
+ Heaters
+ Implanted PIN
+ Flip-chip

3 µm SOI

University of Southampton

CORNERSTONE

Passive + heaters

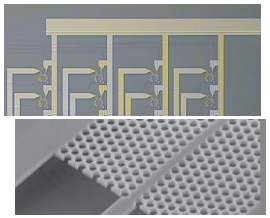


Actives

220-500 nm SOI

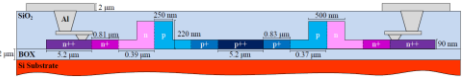
AMO

Customized actives &
Passives with EBL

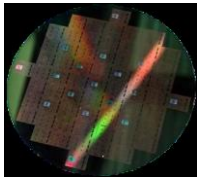


220/340 nm SOI

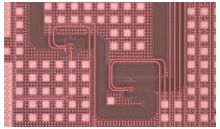
Institute of Microelectronics
A*STAR



220 nm SOI

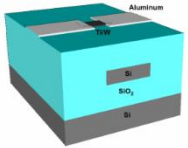


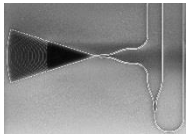
AIM photonics



220 nm SOI

ANT APPLIED NANOTOOLS INC.





220/300 nm SOI

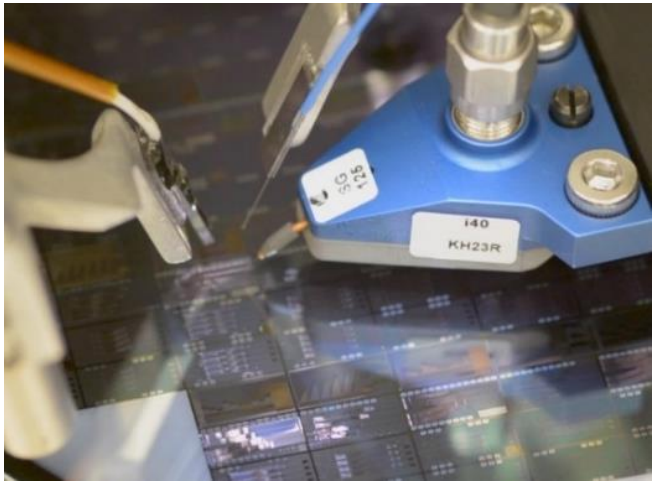
TOWERJAZZ
The Global Specialty Foundry Leader

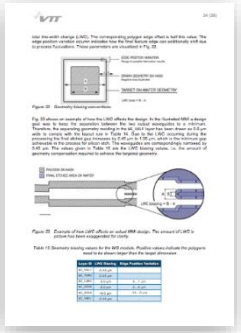
220 nm SOI

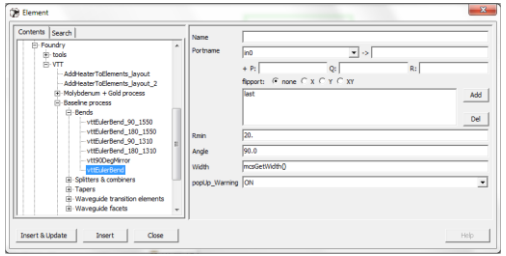
Specialty of VTT: 3 µm thick silicon waveguides

Micronova clean room facility: From R&D to production

- Clean room 2 600 m^2, class 10-100-1000
- 150 → 200 mm wafer size upgrade by 2021
- Stepper lithography (i-line) & e-beam lithography
- Automated wafer-level O/E testing
- Multi-project wafer (MPW) runs and dedicated runs
- Process design kits (PDKs)
- Small/medium volume contract manufacturing via VTT Memsfab for 1–1000 SOI wafers/year







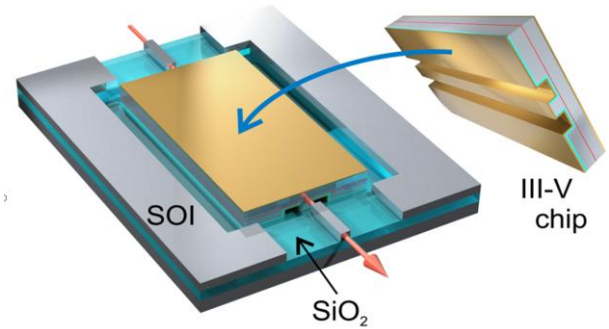
SYNOPSYS®

LUCEDA PHOTONICS

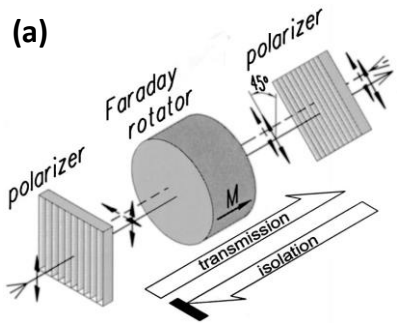
VTT MEMSFAB LTD

Remaining barriers for using Si photonics

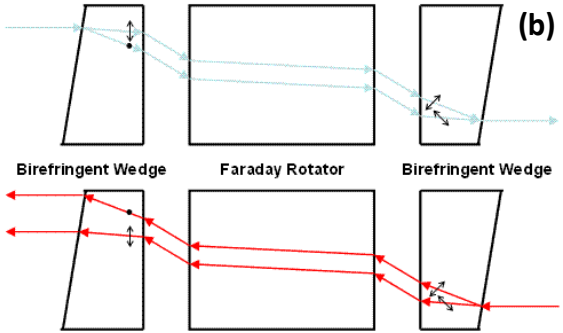
- High **scattering losses**, strong **polarization dependency** and limited **optical power** in <1 µm thick waveguides
- Low **bandwidth** in >1 µm thick waveguides
- Lack of monolithic **light sources** on silicon
- Lack of monolithic **isolators and circulators**



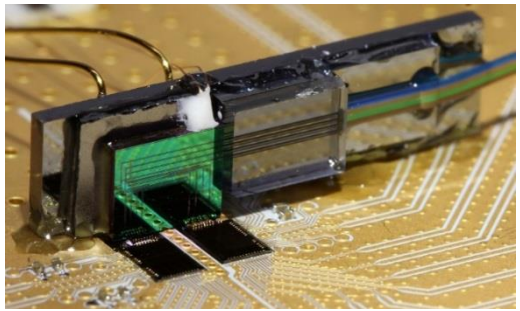
H. Tuorila et al., Appl. Phys. Lett. 113, 041104 (2018)



Single polarization isolator



Polarization independent isolator

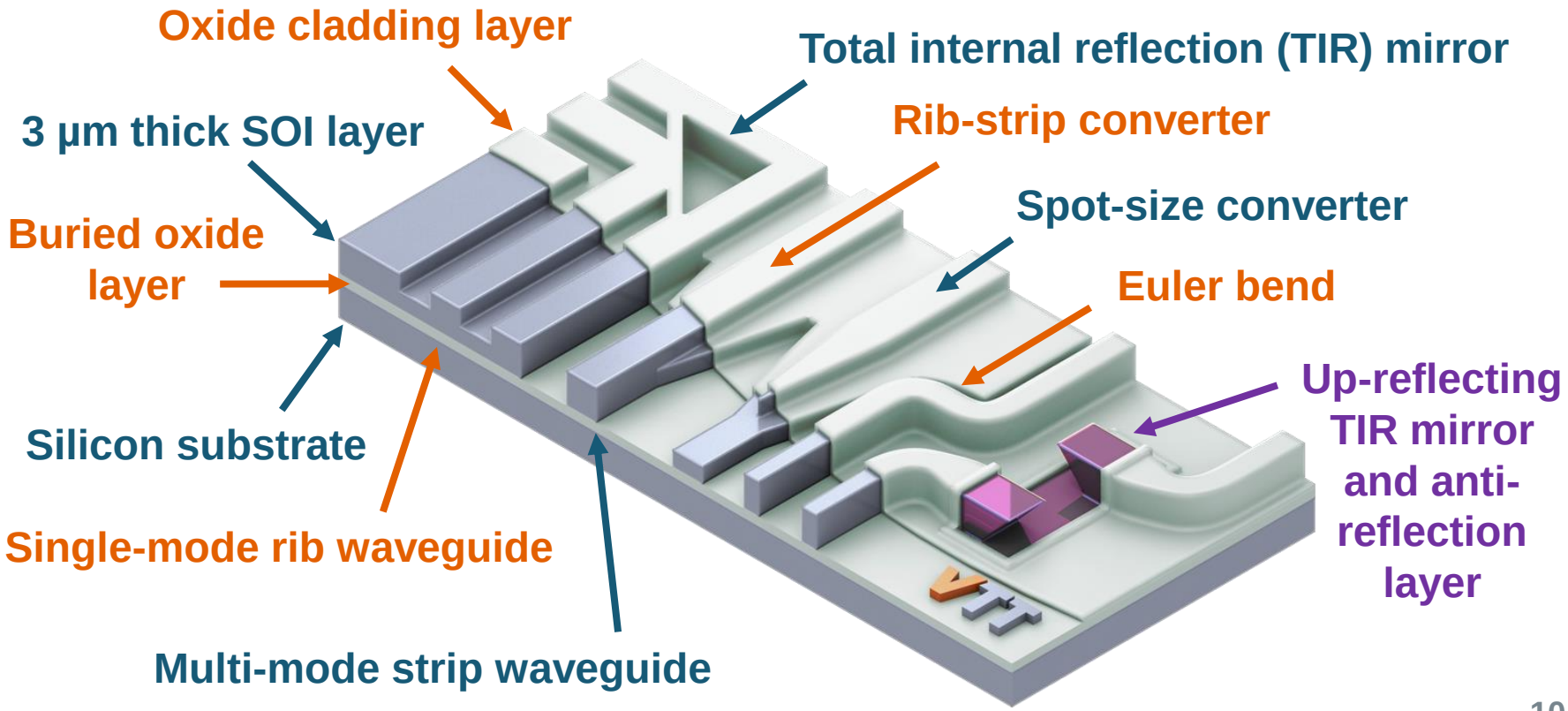


Hybrid laser assembly

Unique aspects of micron-size SOI waveguides:

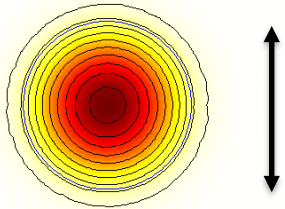
- Dense integration
- Low scattering losses
- Polarization independency
- Wavelength independency

Illustration of the 3 µm SOI platform



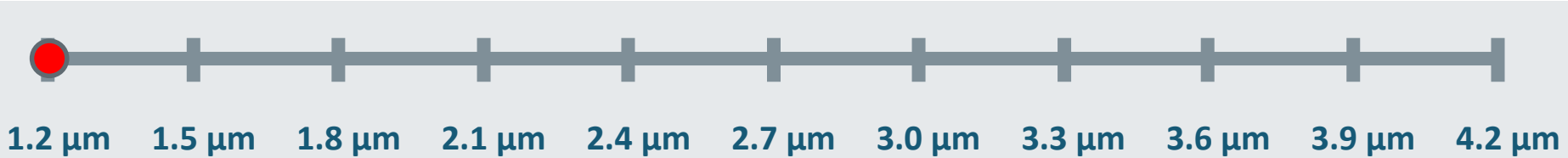
Wavelength dependency of a SMF-28 fiber

Norm of the E field plotted as a function of wavelength



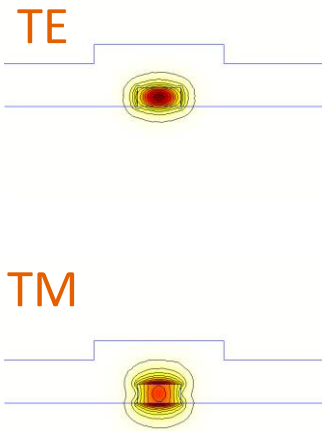
Waveguide core

Standard
single-mode fiber

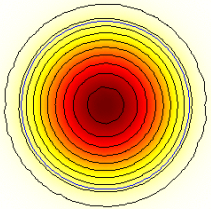


220 nm SOI waveguides have even more narrow wavelength range and high polarization dependency

Norm of the E field plotted as a function of wavelength

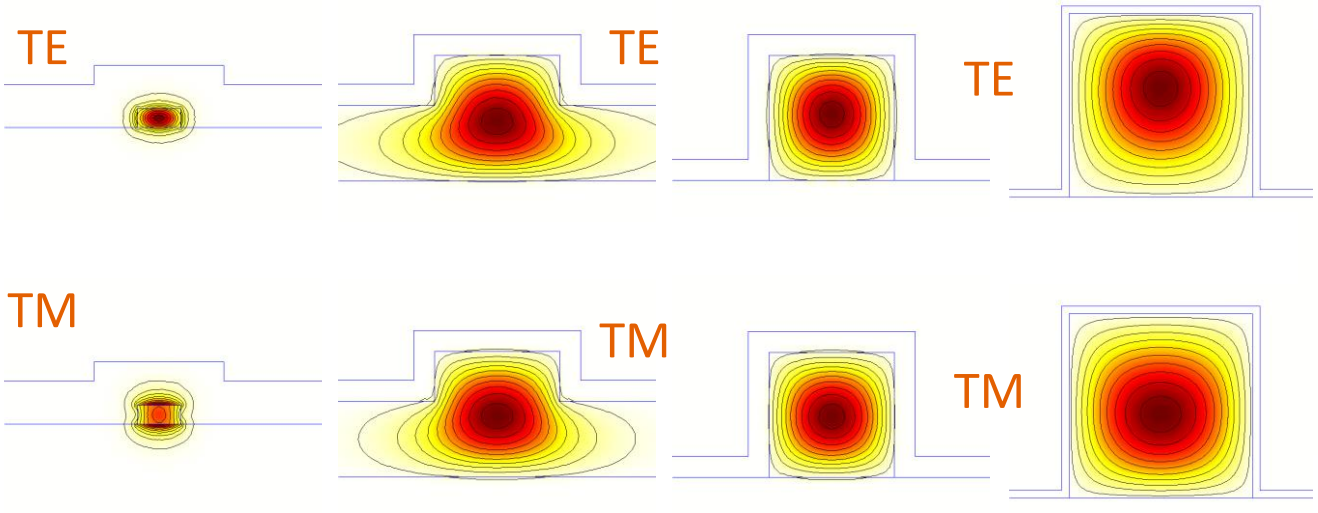


220 nm SOI (strip)



Standard single-mode fiber

Micron-size SOI waveguides have ultra-wide wavelength range for both TE & TM

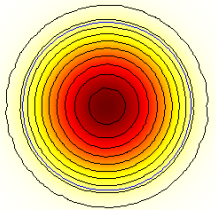


220 nm SOI (strip)

3 µm SOI (SM rib)

3 µm SOI (strip)

12 µm SOI (strip)

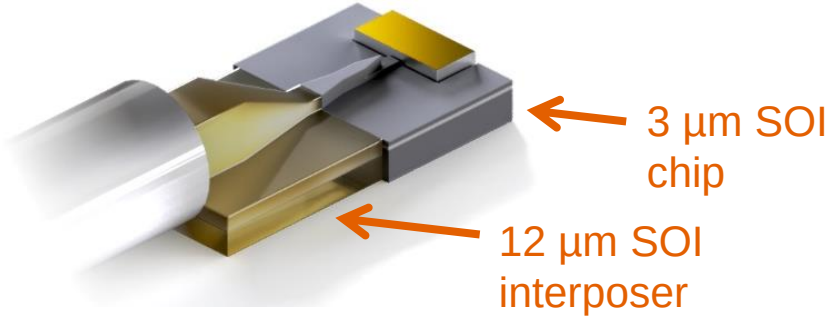


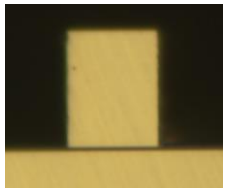
Standard single-mode fiber

1.2 µm 1.5 µm 1.8 µm 2.1 µm 2.4 µm 2.7 µm 3.0 µm 3.3 µm 3.6 µm 3.9 µm 4.2 µm

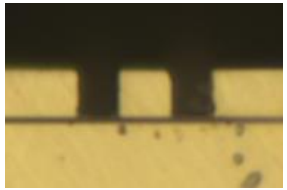
Broadband 3D tapers

- Polished 3D tapers from 12 µm to 3 µm

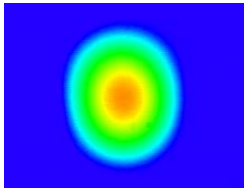




12 x 9.5 µm

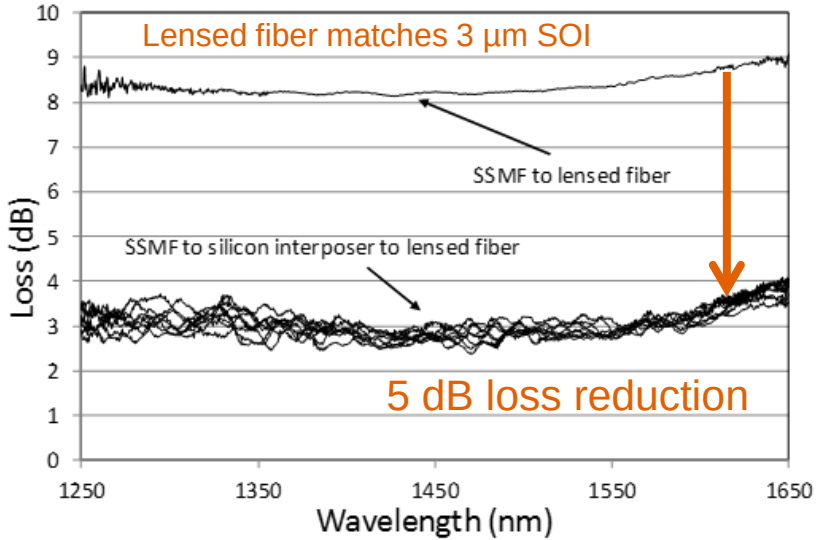


3 x 3 µm



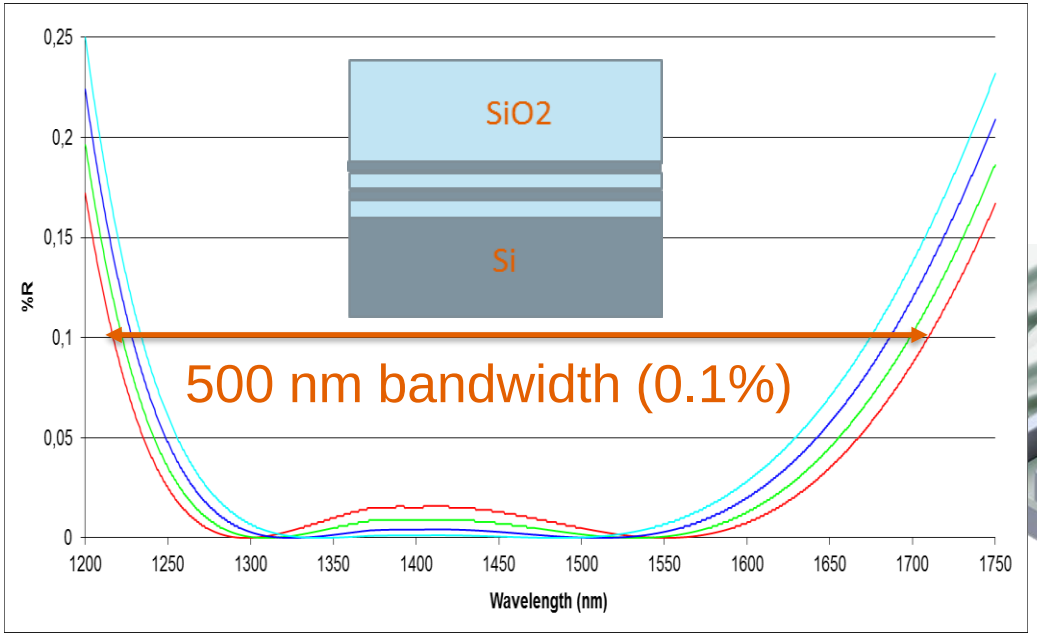
IR output (3 x 3 µm)

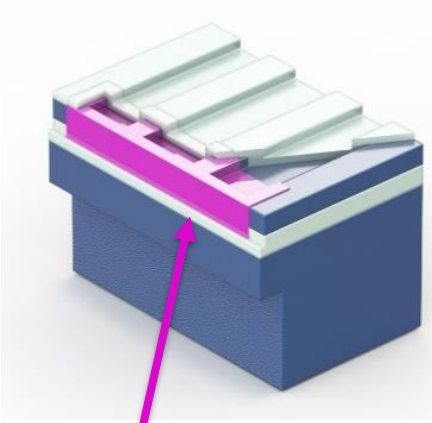
Flat transmission spectra of all 8 waveguides confirm adiabatic spot-size conversion

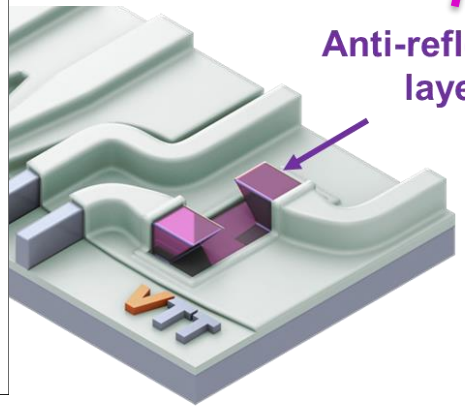


Broadband AR coating designs

- Anti-reflection coating minimizes reflections in material interfaces
- Baseline: Single SiN layer (75 nm bandwidth for 0.1%)
- Multilayer: $Si–SiO_2–Si–SiO_2–Si–SiO_2$







Highlights from silicon photonics in 3 µm SOI

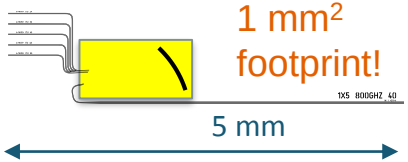
Improvements in filters & multiplexers

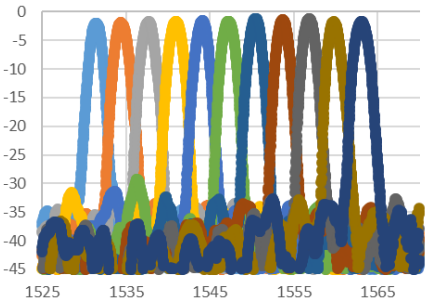
AWG multiplexers in 2013 (ESA OTUS):

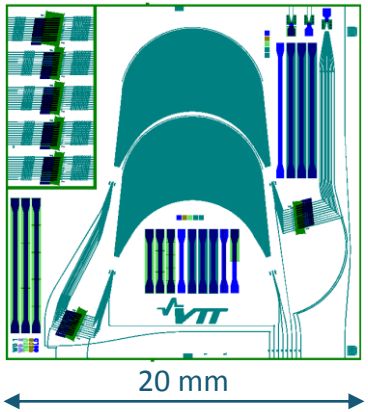
- Down to 5.5 dB loss and -25 dB cross talk
- AWG footprint ~100 mm^2

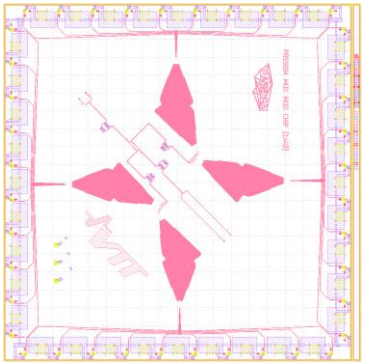
Multiplexers in 2019 (EU PASSION):

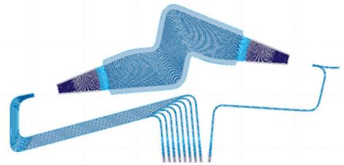
- AWGs with down to 1.6 dB loss and **-35 dB cross-talk** (footprint ~25 mm^2)
- Echelle gratings with down to **0.7 dB loss** and -25 dB cross-talk

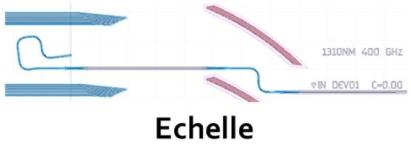


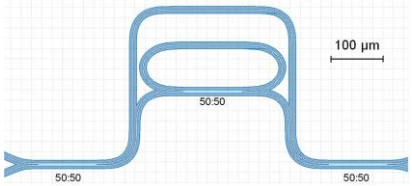








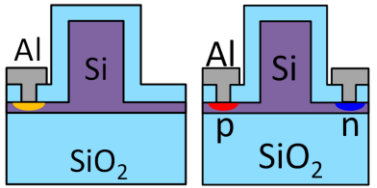


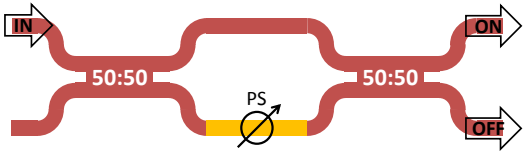


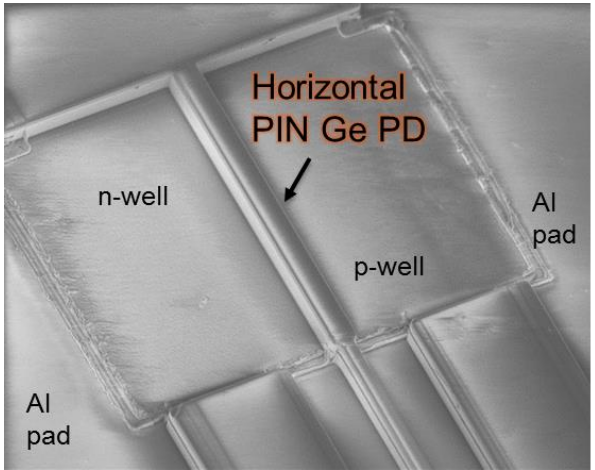
Ring-loaded AMZI

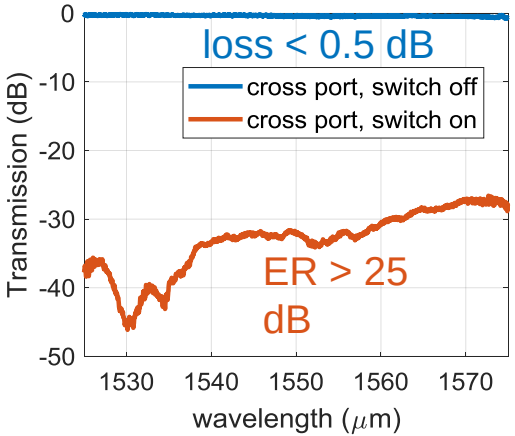
Monolithic integration of modulators, switches and photodetectors

- Implanted heaters for thermo-optic modulation/switching
  - >10 kHZ operation, 24 mW power
- Si p-i-n diodes for phase/amplitude modulation
  - > 2 MHz operation, <5 mW power
- Epitaxially grown Ge photodiodes
  - Responsivity ~1 A/W
  - 3 dB bandwidth up to 40 GHz





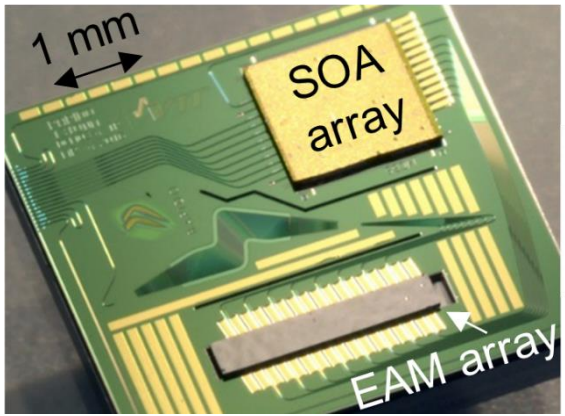




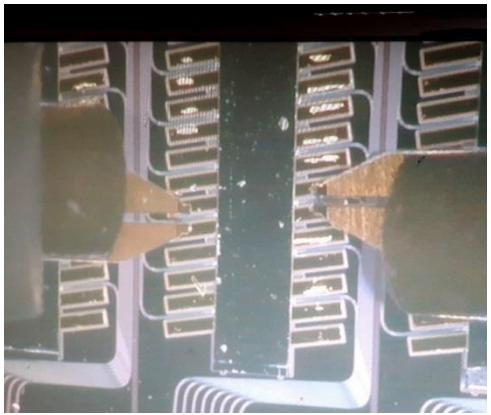
Hybrid integration of active components

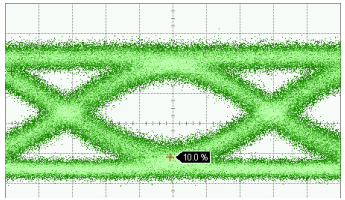
- Lasers, amplifiers, modulators and photodetectors have been hybrid integrated with 3 µm SOI

5x5 mm SOI chip with 8-ch SOA and EAM arrays

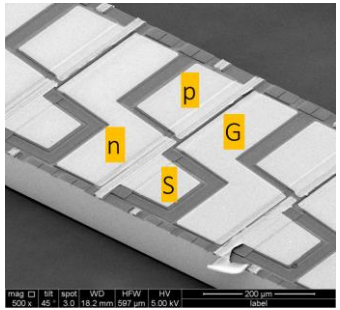


EAM array being tested on SOI





Measured 12.5 Gbps eye diagram

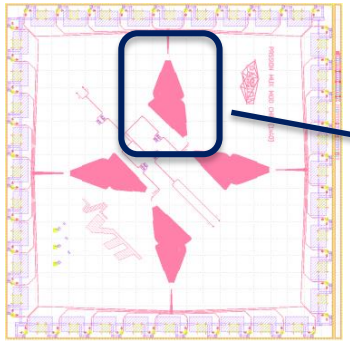


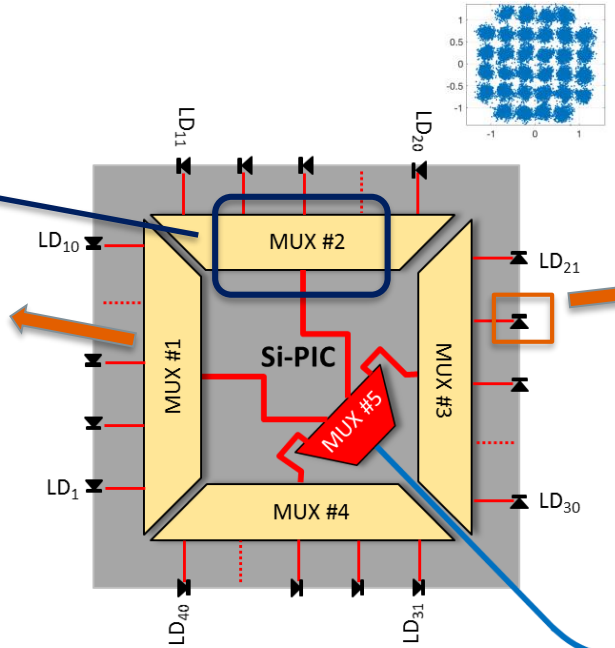
EAM array on GaAs chip

Hybrid VCSEL integration on 3 µm SOI

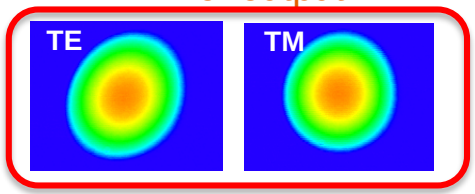
- VCSEL-SOI coupling with up-reflecting mirrors
- 40 VCSELs and 40x1 MUX in 20x20 mm

PIC layout (2x2 cm)

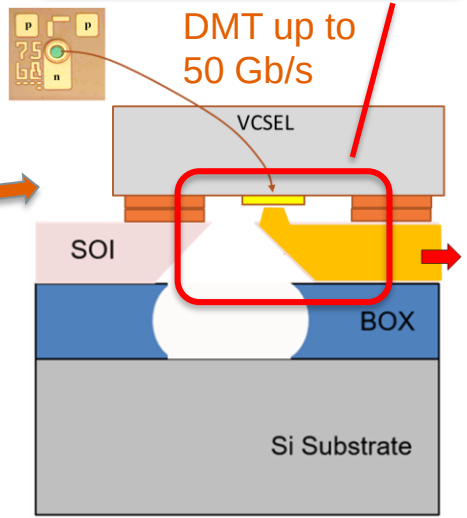




Mirror output



DMT up to 50 Gb/s

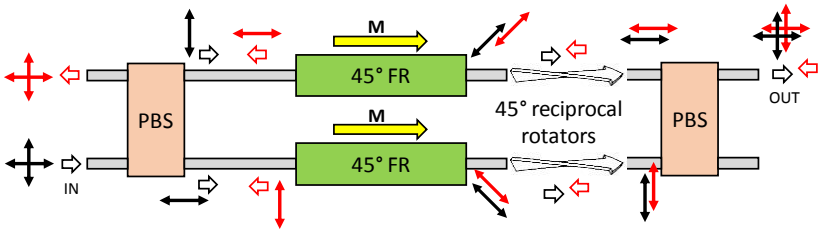


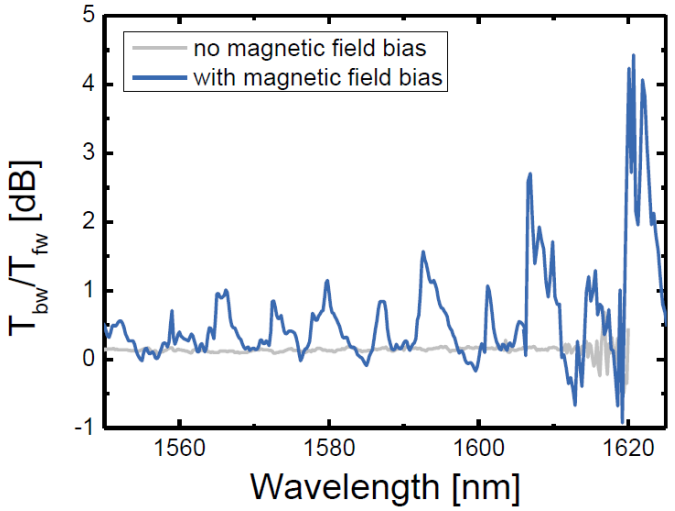
2 Tb/s transmitter

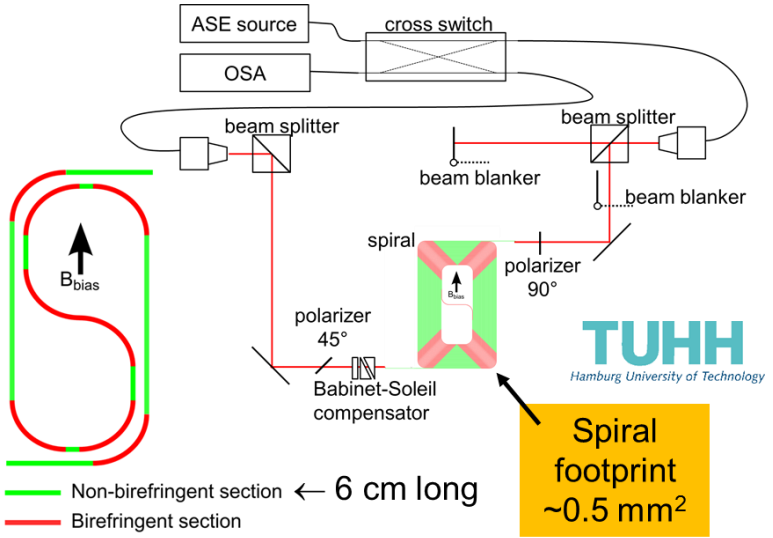
EU project

First design and experimental demonstration of Faraday rotation in 3 µm SOI waveguide spirals

- Demonstration of Faraday rotation in Si
- Layout fine tuning is needed to demonstrate a broadband isolator with high extinction ratio





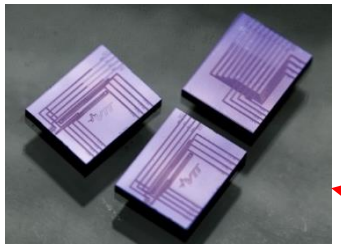


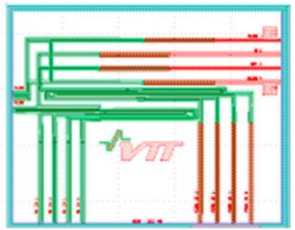
Dirk Jalas et al., "Faraday rotation in silicon waveguides", Proc. IEEE 14th Int. Conf. Group IV Photonics (GFP'17), pp. 141-142, 2017

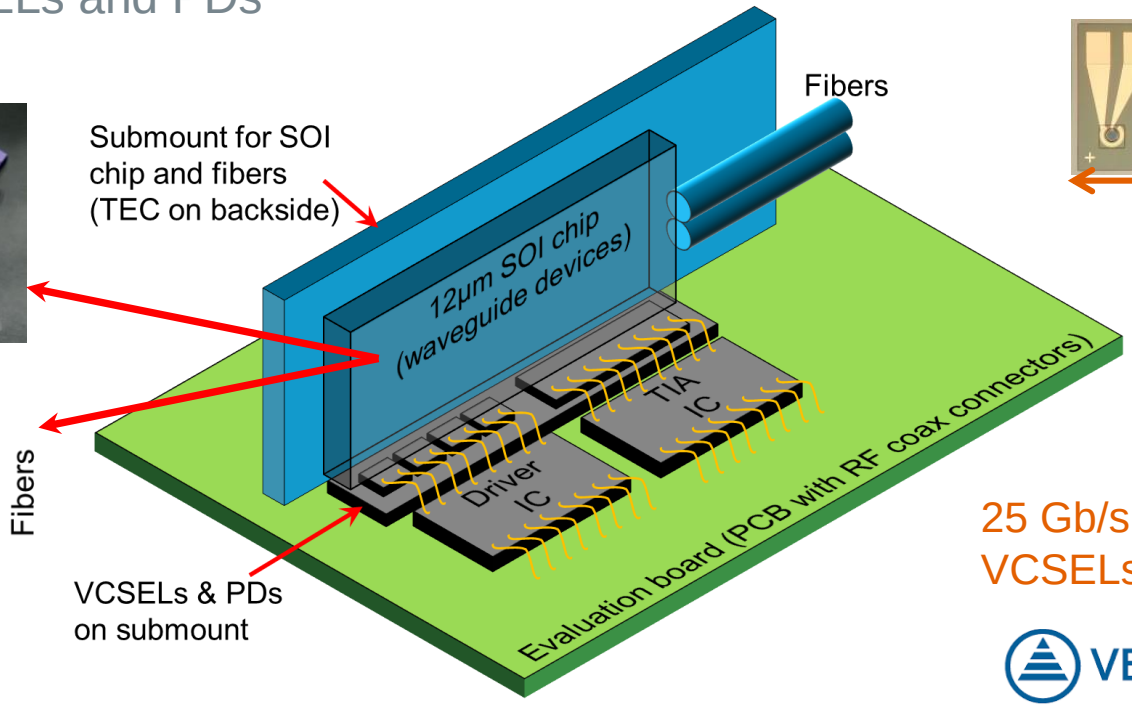
4x25G transceiver on 12 µm SOI

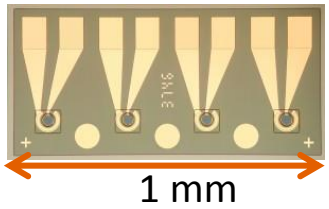
Hybrid VCSEL and PD integration with 12 µm SOI for 4x25G transceiver

- Passive SOI chip added on top of VCSELs and PDs

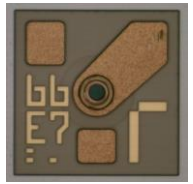








28 Gb/s PD arrays

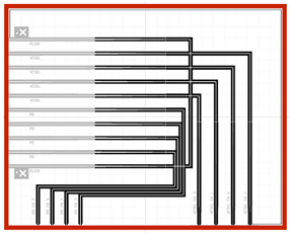


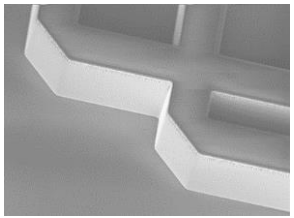
25 Gb/s VCSELs

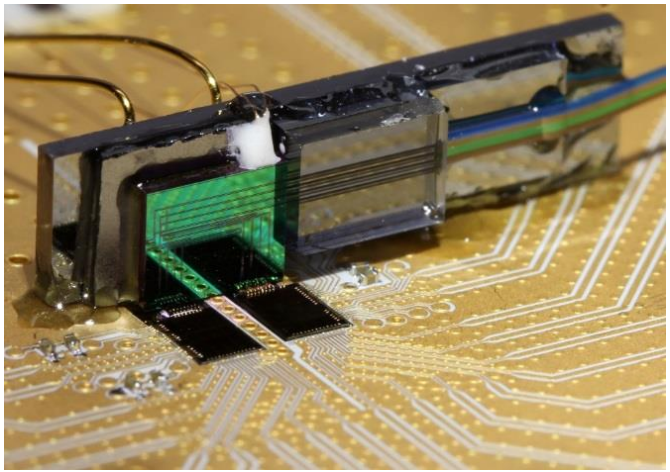
VERTILAS®

Hybrid VCSEL and PD integration with 12 µm SOI for 4x25G transceiver

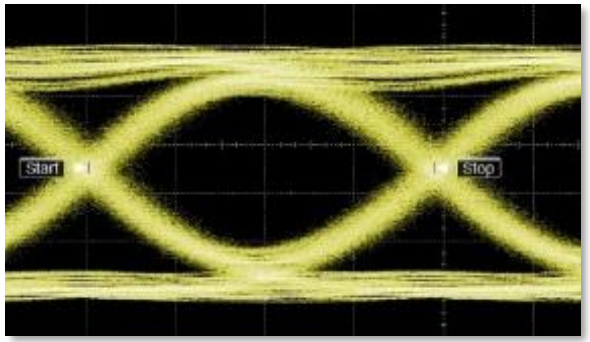
- Optical SDM & WDM transceivers were assembled and tested
- Optical links were tested up to 25.7 Gbps (SDM)
- Total link loss ~10 dB (mainly from misalignments & VCSEL-SOI mismatch)







Assembled transceiver

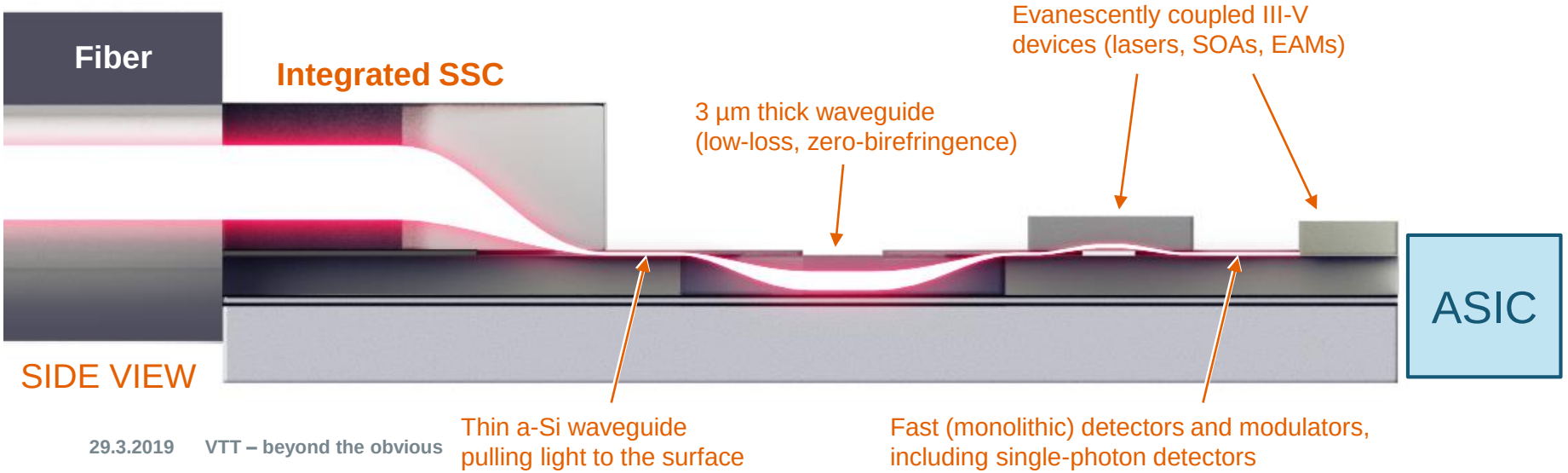


25.7 Gbps eye diagram from VCSEL-SOI-SMF-SOI-PD link

What next?

Local spot-size conversions on 3 µm SOI for I/O coupling and ultra-fast components

- Low-loss, low-cost coupling from 3 µm SOI to standard SM fiber arrays
- High-speed modulators and photodetectors based on locally thinned waveguides
  - Plasmonic devices with ability to reach >>100 GHz



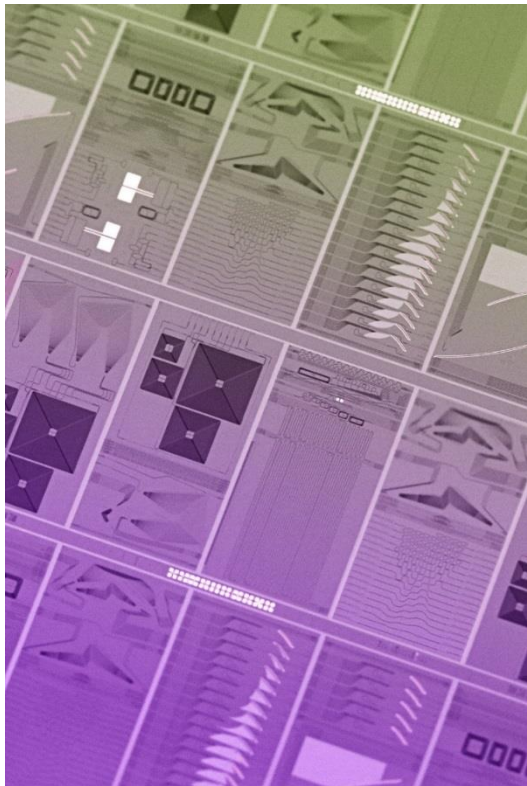
CONCLUSIONS

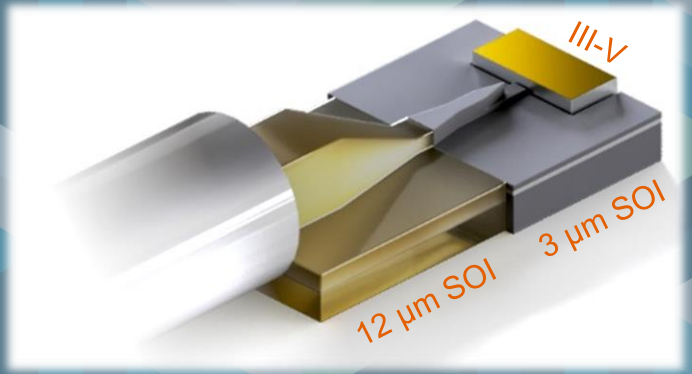
Micron-size silicon waveguides already offer

- Low losses in small footprint
- Polarization independent, ultra-broadband operation
- Monolithic & hybrid integration of active components
- Path ready from R&D to volume production

…and in the future they are aimed to also offer

- Isolators & circulators on chip
- Fast monolithic modulators & photodiodes
- Even lower losses to support microwave photonics, optical computing and other new applications
- Single-photon detectors for quantum photonics





Thank you!

@VTTFinland
#VTTbeyondtheobvious

silicon.photonics@vtt.fi
www.vtt.fi/siliconphotonics