2021 Workshop on Optical/Photonic Interconnects for Computing Systems

14-15 April, 2021
Starting at 07:00 Pacific Daylight Time (UTC-7) daily

OPTICS 2021

Online Workshop
April 14 - 15, 2021

Despite the slowdown of Moore's Law, applications from machine learning and edge computing to scientific computing and mobile computing continuously demand more performance under tighter cost, energy, and size constraints. Silicon-based photonic technologies advanced rapidly in the last two decades and have become promising solutions to complement electronic technologies. The OPTICS (optical/photonic interconnects for computing systems) workshop aims at discussing the latest advances in optics/photonics for computing systems, covering topics from fabrications, photonic devices, photonic circuits, architectures, system integrations, and design automation and optimization. The workshop targets researchers and engineers working on optics/photonics, electronics, architectures, systems, applications and design automation.

Topics to be discussed include but are not limited to:

- PEDA (Photonic-Electronic Design Automation): layout, placement and routing, floorplan, crosstalk, thermal, process variation, etc.
- Photonic-electronic system integration and application: data center, HPC, automobile, aviation, etc.
- Photonics-based architecture: optical neural network, rack-scale optical network, inter/intra-chip optical network, optical switching, etc.
- Photonic/optic circuits: OE conversion, optical interconnect, optical computing circuit, etc.
- Photonic device and fabrication: laser, photodetector, modulator, switch, filter, etc.

Organizing Committee

Luca Ramini received the M.S. degree in Electrical Engineering from the University of Ferrara in 2010 and the PhD from the same University in 2014. He has been technical leader of system-level cross-benchmarking efforts between optical interconnects and their electrical counterparts. Luca has been visiting researcher at Columbia University in 2011, PostDoc at the University of Ferrara and Contract Professor at the University of Verona from 2014 to 2016. From May 2016 to June 2019 he was senior silicon photonics designer at STMicroelectronics, in Agrate Brianza (Italy). Luca's key activities included modeling, simulation and design of photonics devices and on chip electro-optical systems for low-power and high-speed transceivers in the domain of data centers applications. Since July 2019 Luca joined the Hewlett Packard Labs as a research scientist, and his main activities rely on the design of silicon photonic systems and circuits. Luca is co-author of more than 25 publications including conference and journal papers, as well as two book chapters, and gave more than 10 international talks.

Mahdi Nikdast is an Assistant Professor in the Department of Electrical and Computer Engineering at Colorado State University (CSU), Fort Collins. Prof. Nikdast received his Ph.D. in Electronic and Computer Engineering from The Hong Kong University of Science and Technology (HKUST), Hong Kong, in 2014, where he was a member of the Mobile Computing System Lab (now called the Big Data System Lab). From 2014 to 2017, he was a post-doctoral fellow at McGill University and Polytechnique Montreal, Canada, where he was a member of the Photonics System Group and Heterogenous Embedded System Lab. He is the director of Electronic-PhotoniC System Design (ECSyD) Laboratory at CSU. Prof. Nikdast has authored and coauthored numerous papers in refereed journals and international conference publications. His research interests include various topics related to integrated photonics and high-performance computing. Prof. Nikdast currently serves as an Associate Editor for IEEE Transactions on Very Large Scale Integration Systems (IEEE TVLSI). He was the recipient of various awards, including the Second Best Project Award at the AMD Technical Forum and Exhibition (AMD-TFE 2010, Taiwan), the Best Paper Award at the Asia Communications and Photonics Conference (ACP 2015, Hong Kong), the Best Paper Award at the Design, Automation, and Test in Europe (DATE) Conference (DATE 2016 - Test Track, Dresden), the Best Paper Award Candidate at ACM Great Lake Symposium on VLSI (GLSVLSI 2018, USA), the Best Paper Honorable Mention Award at ACM Great Lake Symposium on VLSI (GLSVLSI 2020, China), and the National Science Foundation (NSF) CAREER Award in 2021. Prof. Nikdast is a Senior Member of IEEE.

Ulf Schlichtmann holds a doctorate in electrical engineering from TUM, as well as a technology business degree. He spent about 10 years in the semiconductor industry (Siemens, Infineon) in various engineering, management and executive positions, working on design automation, design libraries, IP reuse, and product development. In 2003, he joined TUM as professor and head of the Chair of Electronic Design Automation. From 2007-2013 he served as Dean and Vice Dean of TUM's Department of Electrical and Computer Engineering (ECE). Since 2013, he serves as Associate Dean of Studies for International Programs, overseeing both the Department's educational programs in Singapore and English language programs in Munich. Since 2016, Ulf is an elected member of TUM's Academic Senate as well as the TUM Board of Trustees. Ulf is a member of the German National Academy of Science and Engineering. Ulf's current research interests include computer-aided design of electronic circuits and systems, with an emphasis on designing reliable and robust systems. His research also addresses emerging technologies, such as microfluidic biochips and photonic interconnects.

Workshop Overview

Time Zone: Pacific Daylight Time (UTC-7)

Wednesday, April 14, 2021:

07:00 **Workshop Opening**

07:10 **Session 1: Silicon Photonic Device & System Characterization and Optimization**

- Jiang Xu: Towards Error-Free Photonic Interconnects
- Ahsan Alam: Towards Accurate Yield Analysis for Real-life Photonic Integrated Circuits
- Jinsung Youn: DWDM Silicon Photonics: From PDK to 3D-Integrated SiPh Receiver Design
- Gaetano Bellanca: On-chip Wireless Optical Interconnects: Results and Perspectives

08:45 **Session 2: Advances on Silicon Photonic Technology and System Integration**

- Siming Chen: Monolithic Quantum Dot Laser for Silicon Photonics
- Antonio Fincato: Silicon Photonic Optical Interfaces for Free-Space Transmissions
- Timo Aalto: Silicon Photonics with 4 dB/m Loss and 40 GHz Photodetectors
- Mark Wade: Optical I/O Chiplets for Heterogeneous Computing

10:15 **Special Session: Photonics Manufacturing and Design Services**

- Kholdoun Torki: Si, SiN, and Glass Photonics Prototyping Services at CMP

Thursday, April 15, 2021:

07:00 **Day 2 Introduction**

07:10 **Session 3: Silicon Photonic Design Automation & Methodologies**

- Tsun-Ming Tseng: Efficiency-Oriented Design Automation for Wavelength-Routed ONoC
- Ashkan Seyedi: Enabling an Automated Photonic VLSI Design Experience
- David Z. Pan: Light for AI: Hardware-Software Codesign in Optical Neural Networks

08:30 **Session 4: Novel Programmable Computing Paradigms using Silicon Photonics**

- Bhavin Shastri: Neuromorphic Silicon Photonics and Applications
- Bert Jan Offrein: Photonic Analog Signal Processing for Neuromorphic Computing
- Sudeep Pasricha: Cross-Layer Design of Deep Learning Accelerators with Silicon Photonics
- Grace Li Zhang: Countering Variations and Thermal Effects for Accurate Optical Neural Networks

Wednesday, April 14, 2021

Workshop Opening

Time Zone: Pacific Daylight Time (UTC-7)

Time: 07:00
Mahdi Nikdast – *Colorado State University*
Luca Ramini – *Hewlett Packard Labs*
Ulf Schlichtmann – *Technical University of Munich*

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Session 1: Silicon Photonic Device & System Characterization and Optimization

Session Chair: Mahdi Nikdast – *Colorado State University*

1.1 Towards Error-Free Photonic Interconnects

Time: 07:10
Jiang Xu – *Hong Kong University of Science and Technology, Hong Kong, China*

1.2 Towards Accurate Yield Analysis for Real-life Photonic Integrated Circuits

Time: 07:30
Ahsan Alam – *Ansys, Canada*

1.3 DWDM Silicon Photonics: From PDK (Process Design Kit) to 3D-Integrated SiPh Receiver Design

Time: 07:50
Jinsung Youn – *Hewlett Packard Labs, USA*

1.4 On-chip Wireless Optical Interconnects: Results and Perspectives

Time: 08:10
Gaetano Bellanca – *University of Ferrara, Italy*

Wednesday, April 14, 2021

Towards Error-Free Photonic Interconnects

7:10am PDT, 10:10am EDT, 3:10pm BST, 4:10pm CEST, 10:10pm Asia

Jiang Xu
Hong Kong University of Science and Technology,
Hong Kong, China

Abstract

Photonic interconnects are facing reliability issues induced by thermal and process variations. Tuning techniques are commonly used to minimize the impacts of such variations and stabilize photonic interconnects. This talk will present a low-cost tuning method, indirect feedback tuning (IFT), to simultaneously alleviate thermal and process variations. IFT can improve the BER of photonic interconnects from 10E-4 to 10E-9 under different situations. We will discuss methods further improve BER to 10E-12 in the near future.

Speaker Bio:

Prof. Jiang Xu received his Ph.D. from Princeton University. He is the acting Department Head of Microelectronics Thrust at Hong Kong University of Science and Technology (HKUST). Before joining HKUST, he worked at Bell Labs, NEC Labs, and a startup company. Jiang established Big Data System Lab, Xilinx-HKUST Joint Lab, and OPTICS Lab at HKUST. He currently serves as the Associate Editor for IEEE TCAD and TVLSI. He served on the steering committees, organizing committees, and technical program committees of many international conferences, including DAC, DATE, ICCAD, CASES, ICCD, CODES+ISSS, NOCS, HiPEAC, ASP-DAC, etc. Jiang was an IEEE Distinguished Lecturer and an ACM Distinguished Speaker. He authored and coauthored more than 130 book chapters and papers in peer-reviewed international journals and conferences. His research areas include machine learning system, photonic-electronic codesign, MPSoC, power delivery and management, low-power embedded system, hardware/software codesign, interconnection network.

Wednesday, April 14, 2021

Towards Accurate Yield Analysis for Real-life Photonic Integrated Circuits

7:30am PDT, 10:30am EDT, 3:30pm BST, 4:30pm CEST, 10:30pm Asia

Ahsan Alam
ANSYS Canada Ltd.,
Vancouver, British Columbia, Canada

Abstract

Photonic Integrated Circuits (PICs) are pervasive in modern technology and enable everything from 5G/6G communications to taking the next big step in quantum computing. For PICs to be successful, we need to equip the photonic circuit designer with the necessary tools to create robust and manufacturable designs for their circuits. Fabricated photonic circuits are always different from their nominal design due to variations in the foundry process as well as SOI chip variations. As a photonics designer, it is important to understand how these variations affect the expected output and hence the yield. Statistical simulations provide insight to these variations. These variations in fabricated photonic circuits are often spatially correlated and so the statistical simulation must be layout aware and account for the spatial correlation between the different circuit elements. However, manufacturing variability is just one of the many challenges faced by a photonic circuit designer. Thermal effects from the drivers in the electronic IC, distortions in the electrical driving signal due to loading effects, and RF losses from packaging can all affect the yield of a real-life PIC. To address these challenges, we need compact models that can capture these effects and solvers that can accurately predict yield with electro-optical co-simulation. This presentation will focus on the research and development at Ansys, which is pioneering PIC simulation and the PIC design ecosystem.

Speaker Bio:

Dr. Ahsan Alam is a Senior R&D Engineer at ANSYS Canada Ltd. His focus is on simulation of active photonic devices and developing compact models for photonic integrated circuit simulation. He holds an MSc in Electrical and Electronic Engineering from BUET and a PhD in Solid State Electronics from the University of Alberta. His research involved studying RF linearity of carbon-based nanoscale field-effect transistors.

Wednesday, April 14, 2021

DWDM Silicon Photonics: From PDK (Process Design Kit) to 3D-Integrated SiPh Receiver Design

7:50am PDT, 10:50am EDT, 3:50pm BST, 4:50pm CEST, 10:50pm Asia

Jinsung Youn
Hewlett Packard Labs,
Milpitas, California, United States

Abstract

Silicon Photonics (SiPh) is a promising solution for data centers and high-performance computing systems as SiPh can provide higher bandwidth and better energy efficiency. To lower the entry barriers for SiPh design, a well-defined process design kit (PDK) is an integral part. In this presentation, we introduce HPEâĂŹs SiPh PDK which contains accurate and intuitive simulation models, layouts, and design rules for various optical devices. Next, a receiver front-end simulation methodology using behavioral models is presented. Finally, we show a 3D-integrated SiPh receiver design and high-speed data transmission results with the fabricated SiPh receiver chip.

Speaker Bio:

Dr. Jinsung Youn is currently working as an SI/PI engineer and a CMOS circuit designer at Hewlett Packard Labs, California, USA. He received a combined M.S. and Ph.D. degree in Electrical and Electronic Engineering from Yonsei University, South Korea, in 2014. His doctoral dissertation concerned the high-speed and power-efficient 850-nm Si optoelectronic integrated circuit design for optical interconnect applications. From 2014 to 2018, he worked as an SI/PI/EMI engineer at Memory Division of Samsung Electronics Ltd., South Korea. In 2018, he joined HPE Labs, his current interests include high-speed optical transceiver design and 3D IC SI/PI analysis for Silicon Photonics.

Wednesday, April 14, 2021

On-chip wireless optical interconnects: results and perspectives

8:10am PDT, 11:10am EDT, 4:10pm BST, 5:10pm CEST, 11:10pm Asia

Gaetano Bellanca
University of Ferrara,
Ferrara, Italy

Abstract

In the last years, optical on-chip data transmission has been proposed as a key technology to overcome the bandwidth and energy limitations of electrical interconnects in networks-on-chip for high-density multi-core architectures. Solutions based on Silicon Photonics (SiP), using waveguides for long interconnects and ring-resonator-based switching fabric, have been extensively investigated.

Optical-Networks-on-Chip (ONoCs) realized in Silicon have the benefit of large bandwidths, low propagation losses and compatibility with electronics. However, this approach suffers of problems related to complex layout, crosstalk, sophisticated routing technologies and high power consumption. Wireless networks are a viable alternative to overcome these issues. Different approaches ranging from microwave to THz have been investigated. Optical Wireless Networks (OWNoCs) is another possible approach that, by combining optical waveguide-based interconnections with optical wireless links, aims at overcoming the limitations of NOC.

In this presentation, the results obtained in the last years by our group on the development of OWNoCs will be summarized. Antenna design, channel modeling and optimization, fabrication and measurement steps will be illustrated and discussed. In particular, the critical aspects of the modeling will be presented, and measurements results for some point-to-point links will be illustrated. Finally, an Optical Wireless Interconnection Block allowing wireless reconfigurable interconnections among different transmitters and receivers will be shown.

Speaker Bio:

Gaetano Bellanca is Associate Professor of Electromagnetic Fields at the Department of Engineering of the University of Ferrara, where he teaches Propagation and Antennas. He also holds courses on Wired and Wireless Interconnections and Anti-Collision Systems and on Electromagnetic Compatibility for the Inter-University Degrees of Automotive (Advanced Automotive Electronic Engineering and Electrical Vehicle Engineering).). The research activities of Gaetano Bellanca fall within the sphere of numerical simulation with applications in various sectors of electromagnetics, ranging from microwave heating to integrated optics. In this context, the activities carried out concern both the design and the characterization of components and devices for telecommunications and optical interconnections at a chip level, optical dielectric and plasmonic antennas and the study of components with applications in the field of sensors and bio-photonics.

Wednesday, April 14, 2021

Session 2: Advances on Silicon Photonic Technology and System Integration

Time Zone: Pacific Daylight Time (UTC-7)
Session Chair: Luca Ramini – *Hewlett Packard Labs*

2.1 Monolithic Quantum Dot Laser for Silicon Photonics

Time: 08:45
Siming Chen – *University College London, UK*

2.2 Silicon Photonic Optical Interfaces for Free-Space Transmissions

Time: 09:05
Antonio Fincato – *ST Microelectronics, Italy*

2.3 Silicon Photonics with 4 dB/m Loss and 40 GHz Photodetectors

Time: 09:25
Timo Aalto – *VTT Technical Research Center of Finland, Finland*

2.4 Optical I/O Chiplets for Heterogeneous Computing

Time: 09:45
Mark Wade – *Ayar Labs, USA*

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Special Session: Photonics Manufacturing and Design Services

Si, SiN, and Glass Photonics Prototyping Services at CMP

Time: 10:15
Kholdoun TORKI – *Circuits Multi-Projets, France*

Wednesday, April 14, 2021

Monolithic Quantum Dot Laser for Silicon Photonics

8:45am PDT, 11:45am EDT, 4:45pm BST, 5:45pm CEST, 11:45pm Asia

Siming Chen
University College London,
London, UK

Abstract

The available of silicon-based laser is the key technology for the whole silicon photonics industry. But the indirect bandgap of silicon is a severe limitation, and, despite recent advances, Group IV-based light emitters will not, in the foreseeable future, outperform their III-V counterparts. Much effort has been directed toward the hybrid integration of III-V lasers with silicon photonics platforms. Although impressive results have been achieved, in the longer-term, the direct epitaxial growth of III-V semiconductor lasers on silicon remains the 'holy grail' for full-scale deployment of silicon photonics with reduced cost and added flexibility. Semiconductor lasers with active regions made from quantum dots (QDs) have shown superior device performance over conventional quantum well (QW) counterparts and offer new functionalities. Furthermore, there are other advantages of QDs for monolithic III-V-on-Si integration over QWs, such as QD devices being less sensitive to defects and optical feedback. It is, therefore, not surprising that the past decade has seen rapid progress in research on the direct growth of III-V QD lasers on Si, with a view to leveraging the beneïňĄts of QD gain region technology while beneïňĄtting from the economics of scale enabled by direct growth.

This talk has a special focus on 1310 nm InAs/GaAs quantum dot lasers in silicon photonics. The challenges and Strategies for developing high-quality III-V materials on silicon using direct epitaxy methods are discussed.

Speaker Bio:

Dr Siming Chen obtained his PhD in Electrical Engineering from the University of Sheffield in 2014. In September 2013, upon submission of his PhD thesis, he joined the UCL as a Research Associate and was awarded a Royal Academy of Engineering Research Fellowship in 2017 in recognition is pioneering work on Si-based QD light sources. Dr Chen is now a Lecturer and a member of the Photonics Group in the Department of Electronic & Electrical Engineering at UCL. He has published more than 80 refereed papers and has an h-index of 20.

Wednesday, April 14, 2021

Silicon Photonic Optical Interfaces for Free-Space Transmissions

9:05am PDT, 12:05am EDT, 5:05pm BST, 6:05pm CEST, 12:05am Asia

Antonio Fincato
ST Microelectronics,
Italy

Abstract

Light transmission outside a Silicon Photonics chip is a problem that has become important in recent years. There are many optical systems that utilize free-space propagating beams such as free-space data communication, Intra-Chip Free-Space Optical Interconnect, LiDAR and sensing.

By means of an Optical Phased Array (OPA) it is possible to generate an adaptive beam by tuning the individual phases and amplitudes of an array of optical emitters. However, the performance normally suitable to this type of components, easily leads to having OPA with hundreds or even thousands of emitters. The imperfections of manufacture in such a large circuit lead to errors both on the amplitude and phase of the outgoing optical signals with the consequent degradation of the shape of the beam. Advanced technology to create both low-loss and accurate devices will therefore be essential for these applications.

The challenge is to realize an electro-optical system in which the optical part is very large and the electronic part very complex. One possibility is to design an electronic integrated chip (EIC) with the task of controlling thousands of closed loop signals and leaving the photonic chip (PIC) the task of transmitting light with the lowest possible loss. A second possibility is to design a photonic chip with an architecture allowing to easily control, and with very few electrical signals, the phase delay on all emitters. In this case the electronic chip is very simplified, but technological control on the photonic chip is more demanding. The laser used as a source works in the telecom C-band at 1550nm, which is eye safe and inside the atmosphere transparency window.

In this presentation these aspects will be addressed, problems discussed, and possible solutions proposed, showing and commenting on the latest experimental data.

Speaker Bio:

Antonio Fincato obtained his degree in Physics from Pavia University in 1984. In the following years he worked at Milano University and at CERN in Geneva on an Elementary particle Physics experiment. In 1986 he joined CSELT laboratories in Turin where he started his studies in Integrated Optics. In 1988 He joined ITALTEL, in 1993 worked for one year at AT&T Bell Labs in Murray Hill and since 2000 he is working in STMicroelectronics, Milan. His research interests include various topics related to integrated photonics and micro-optics. He worked on technologies like Ionic exchange in glass, Glass on Silicon and Silicon Photonics. He developed micro-optical and integrated-optical components and architectures for Datacom and Sensing applications. He is author or co-author of more then 20 patents and 30 articles in journals and conferences.

Wednesday, April 14, 2021

Silicon photonics with 4 dB/m loss and 40 GHz photodetectors

9:25am PDT, 12:25am EDT, 5:25pm BST, 6:25pm CEST, 12:25am Asia

Timo Aalto
VTT Technical Research Centre of Finland,
Espoo, Finland

Abstract

Increasing the thickness of silicon-on-insulator (SOI) waveguides from 220 nm to 3 Âţm leads to dramatic reduction in propagation loss and polarization dependency without compromising ultra-dense integration and single-mode operation in the system-level. Some recent highlights from the 3 Âţm SOI technology are presented here and their relevance to optical interconnects is discussed. The propagation loss of 3 Âţm thick SOI waveguides was pushed as low as 0.04 dB/cm, which enables ultra-long delay lines and on-chip Faraday rotators. Arrayed waveguide gratings were demonstrated with up to 40 ports, which supports the scaling of wavelength division multiplexing. Ge PDs were demonstrated with up to 40 GHz bandwidth.

Speaker Bio:

Timo Aalto works as a Research Team Leader at VTTâĂŹs Silicon Photonics research group. His research focuses on the micron-scale silicon waveguides that are used to make ultra-compact and low-loss photonic integrated circuits for communication, imaging and sensing applications at near and mid infrared wavelengths. Aalto has contributed to over 80 scientific publications, reviewed several EU projects, journal articles and theses and coordinated large projects funded by the EU and the European space agency. Aalto received his D.Sc. (tech) degree in optoelectronics technology from the Helsinki University of Technology in 2004 and has worked in Silicon photonics research at VTT since 1997.

Wednesday, April 14, 2021

Optical I/O Chiplets for Heterogeneous Computing

9:45am PDT, 12:45am EDT, 5:45pm BST, 6:45pm CEST, 12:45am Asia

Mark Wade
Ayar Labs,
Emeryville, California, United States

Abstract

Applications such as machine learning require large, distributed computing systems to continue scaling performance. Chip-to-chip I/O metrics (bandwidth density, energy efficiency, latency) present a bottleneck that limits the overall performance of distributed systems. As bandwidths increase, electrical signaling over long distances (centimeters - meters) becomes extremely challenging. In this talk, I will present progress on a new optical I/O technology that aims to solve the bandwidth-distance tradeoff and enable a new class of distributed and heterogenous computing systems.

Speaker Bio:

Mark Wade is the President and CTO at Ayar Labs. He received his PhD from the University of Colorado Boulder where he received the Best Dissertation award for work on electronic-photonics. He has held multiple PI positions on DARPA, NSF, and DOE research grants. He currently leads engineering and product development at Ayar Labs.

Wednesday, April 14, 2021

Si, SiN, and Glass Photonics Prototyping Services at CMP

Time: 10:15am PDT, 1:15pm EDT, 6:15pm BST, 7:15pm CEST, 1:15am Asia

Kholdoun Torki
Circuits Multi-Projets,
Grenoble, France

Abstract

CMP is a service organization enabling prototype and low volume production fabrications on industrial process lines. Services are provided at very attractive costs thanks to MPW runs (Multi-Project Wafer) using cost sharing for masks and wafer fabrications. CMP is pioneering such service offer since 1981. Technology processes offered at CMP include microelectronics processes, MEMS, and Photonics processes. CMP is a Service Centre and partner in EUROPRACTICE.

Photonics processes offered at CMP are presently from:

CEA-Leti : Si-Photonics 220nm with passive, 310nm passive and active, Si3N4 with passives.

AMF : Si-Photonics with SiN option.

TEEM Photonics with NIR and Visible processes on glass, as well as WAFT.

The service offer from CMP comes with access to design-kits, technical support, and Multi-Projects Wafer fabrication. The Photonics packaging service is also provided by CMP in the frame of EUROPRACTICE where the assembly can be done either for the PIC packaging or with an electronic component integration.

CMP service is available to Universities, Research Labs, and Industrial companies. 660 customers from 71 countries have been served, more than 8480 projects have been prototyped through 1180 MPW runs and 74 different technologies have been interfaced.

Speaker Bio:

Dr. Kholdoun TORKI received his Ph.D. degree in Microelectronics in 1990 from the INPG Grenoble, France. He is currently Director of CMP, since 2020. His research interest includes CAD tools design-flows and methodologies, 2.5/3D-IC System Integration. He is currently involved in Europractice European project, where CMP is partner and service center. He authored and co-authored more than 120 scientific papers, designed more than 30 ASIC circuits, and since 1986 has participated and/or coordinated 15 European and National projects. He is co-founder and member of the board of directors of iRoC Technologies.

Thursday, April 15, 2021

Day 2 Introduction

Time Zone: Pacific Daylight Time (UTC-7)

Time: 07:00
Mahdi Nikdast – *Colorado State University*
Luca Ramini – *Hewlett Packard Labs*
Ulf Schlichtmann – *Technical University of Munich*

Session 3: Silicon Photonic Design Automation & Methodologies

Session Chair: Ulf Schlichtmann – *Technical University of Munich*

3.1 Efficiency-Oriented Design Automation for Wavelength-Routed Optical Network-on-Chip

Time: 07:10
Tsun-Ming Tseng – *Technical University of Munich, Germany*

3.2 Enabling an Automated Photonic VLSI Design Experience

Time: 07:30
Ashkan Seyedi – *Hewlett Packard Labs, USA*

3.3 Light for AI: Hardware-Software Codesign in Optical Neural Networks

Time: 07:50
David Z. Pan – *UT Austin, USA*

Thursday, April 15, 2021

Efficiency-Oriented Design Automation for Wavelength-Routed Optical Network-on-Chip

7:10am PDT, 10:10am EDT, 3:10pm BST, 4:10pm CEST, 10:10pm Asia

Tsun-Ming Tseng
Technical University of Munich,
Munich, Germany

Abstract

Among different types of optical network-on-chip (ONoC), wavelength-routed optical network-on-chip (WRONoC) is renowned for its arbitration-free data communication. On WRONoCs, signal transmission does not suffer from unpredictable delay for signal path construction in congested networks. This is because the signal path between each pair of communicating nodes is pre-determined during the design phase and signal collision is guaranteed not to occur even when all nodes are talking at the same time. Implementing this feature, however, makes the design of WRONoCs very challenging. Thus far, a wide scope of different WRONoC design automation tools has been proposed for automatic topology generation and physical design. However, all these tools become starved of computing power when the network size grows. This talk will address this issue and discuss methodologies for WRONoC design automation for better efficiency.

Speaker Bio:

Tsun-Ming Tseng is a postdoctoral researcher and a research group leader at the chair of electronic design automation, Technical University of Munich. Tsun-Ming develops and applies design automation methods for different kinds of engineering problems, including microfluidics, optical network-on-chip, and novel microfabrication. Tsun-Ming received the dissertation award "Bund-der-Freunde-der-TUM" from Technical University of Munich in 2017. He is in the blue ribbon panel of NSF - LEAP HI.

Thursday, April 15, 2021

Enabling an Automated Photonic VLSI Design Experience

7:30am PDT, 10:30am EDT, 3:30pm BST, 4:30pm CEST, 10:30pm Asia

Ashkan Seyedi
Hewlett Packard Labs,
Milpitas, California, United States

Abstract

This talk will outline the recent work done at Hewlett Packard Labs to enable an automated, schematic-driven design flow for co-packaged silicon photonics. It will discuss the device model implementation, electro-optical co-simulation, initial schematic-to-layout conversion and DRC. Finally, recent hardware demonstration results will be shown.

Speaker Bio:

Ashkan received a dual Bachelor's in Electrical and Computer Engineering from the University of Missouri-Columbia and a Ph.D. from University of Southern California working on photonic crystal devices, high-speed nanowire photodetectors, efficient white LEDs and solar cells. While at Hewlett Packard Enterprise as a research scientist, he has been working on developing high-bandwidth, efficient optical interconnects for exascale and high performance computing applications.

Thursday, April 15, 2021

Light for AI: Hardware-Software Codesign in Optical Neural Networks

7:50am PDT, 10:50am EDT, 3:50pm BST, 4:50pm CEST, 10:50pm Asia

David Z. Pan
The University of Texas at Austin,
Austin, Texas, United States

Abstract

Deep neural networks have demonstrated superior performance in various artificial intelligence tasks. However, as Moore's law winds down, it becomes increasingly difficult for traditional electrical digital computers to support the escalating computation demands with tight performance and energy constraints. As an emerging neuromorphic framework, the optical neural network (ONN) shows promising potentials for next-generation AI acceleration due to its ps-level latency, TOPS-level throughput, and sub-fJ/MAC-level energy consumption. In this talk, I will talk about recent progress in leveraging light for efficient AI computing and how hardware-software co-design plays a key role in this synergistic exploration. I will give an overview of how to jointly optimize the efficiency and robustness of ONNs via circuit-algorithm co-design, and show some recent results, including device-aware quantization, circuit pruning, structured matrices, frequency-domain computing, and power-aware on-chip learning.

Speaker Bio:

David Z. Pan is a Professor and holder of Silicon Laboratories Endowed Chair at the Department of Electrical and Computer Engineering, The University of Texas at Austin. His research interests include bidirectional AI and IC interactions, electronic design automation, design for manufacturing, hardware security, and CAD for analog/mixed-signal ICs and emerging technologies. He has published over 400 refereed journal/conference papers and 8 US patents. He has served in many journal editorial boards and conference committees, including various leadership roles such as ICCAD 2019 General Chair, ASP-DAC 2017 TPC Chair, and ISPD 2008 General Chair. He has received many awards, including SRC Technical Excellence Award, 19 Best Paper Awards (ISPD 2020, ASP-DAC 2020, DAC 2019, GLSVLSI 2018, VLSI Integration 2018, HOST 2017, SPIE 2016, ISPD 2014, ICCAD 2013, ASP-DAC 2012, ISPD 2011, IBM Research 2010 Pat Goldberg Memorial Best Paper Award in CS/EE/Math, ASP-DAC 2010, DATE 2009, ICICDT 2009, SRC Techcon in 1998, 2007, 2012 and 2015), DAC Top 10 Author Award in Fifth Decade, ASP-DAC Frequently Cited Author Award, Communications of ACM Research Highlights, ACM/SIGDA Outstanding New Faculty Award, NSF CAREER Award, IBM Faculty Award (4 times), and many international CAD contest awards. He has graduated 37 PhD students and postdocs who have won many awards, including the First Place of ACM Student Research Competition Grand Finals in 2018, ACM/SIGDA Student Research Competition Gold Medal (three times), ACM Outstanding PhD Dissertation in EDA Award (twice), EDAA Outstanding Dissertation Award (twice), etc. He is a Fellow of IEEE and SPIE.

Thursday, April 15, 2021

Session 4: Novel Programmable Computing Paradigms using Silicon Photonics

Time Zone: Pacific Daylight Time (UTC-7)
Session Chair: Thomas Van Vaerenbergh – *Hewlett Packard Labs*

4.1 Neuromorphic Silicon Photonics and Applications

Time: 08:30
Bhavin Shastri – *Queen's University, Canada*

4.2 Photonic Analog Signal Processing for Neuromorphic Computing

Time: 08:50
Bert Jan Offrein – *IBM Research Institute, Switzerland*

4.3 Cross-Layer Design of Deep Learning Accelerators with Silicon Photonics

Time: 09:10
Sudeep Pasricha – *Colorado State University, USA*

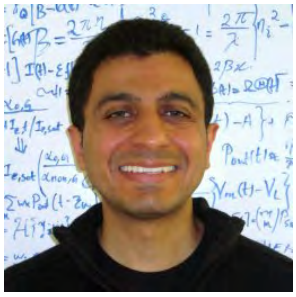
4.4 Countering Variations and Thermal Effects for Accurate Optical Neural Networks

Time: 09:30
Grace Li Zhang – *Technical University of Munich, Germany*

Thursday, April 15, 2021

Neuromorphic Silicon Photonics and Applications

8:30am PDT, 11:30am EDT, 4:30pm BST, 5:30pm CEST, 11:30pm Asia



Bhavin J. Shastri
Queen's University,
Kingston, Ontario, Canada

Abstract

Artificial intelligence enabled by neural networks has enabled applications in many fields (e.g. medicine, finance, autonomous vehicles). Software implementations of neural networks on conventional computers are limited in speed and energy efficiency. Neuromorphic engineering aims to build processors in which hardware mimic neurons and synapses in brain for distributed and parallel processing. Neuromorphic engineering enabled by silicon photonics can offer sub nanosecond latencies, and can extend the domain of artificial intelligence and neuromorphic computing applications to machine learning acceleration (vector-matrix multiplications, inference and ultrafast training), nonlinear programming (nonlinear optimization problem and differential equation solving) and intelligent signal processing (wideband RF and fiber-optic communications). We will discuss current progress and challenges of neuromorphic photonics to scale to practical systems.

Speaker Bio:

Dr. Bhavin J. Shastri is an Assistant Professor of Engineering Physics at Queen's University, Canada, and a Faculty Affiliate at the Vector Institute for Artificial Intelligence. He was an Associate Research Scholar (2016-2018) and Banting and NSERC Postdoctoral Fellow (2012-2016) at Princeton University. He received the Ph.D. degree in electrical engineering (photonics) from McGill University in 2012. With research interests in silicon photonics, photonic integrated circuits, neuromorphic computing, and machine learning, he has published more than 65 journal articles and 80 conference proceeding, 5 book chapters, and given over 40 invited talks and lectures including 2 Keynotes. He is a co-author of the book, Neuromorphic Photonics (Taylor & Francis, CRC Press, 2017). Dr. Shastri is the winner of the 2020 IUPAP Young Scientist Prize in Optics "for his pioneering contributions to neuromorphic photonics" from the ICO. He is a Senior Member of OSA and IEEE, recipient of the 2014 Banting Postdoctoral Fellowship from the Government of Canada, the 2012 D. W. Ambridge Prize for the top graduating Ph.D. student, an IEEE Photonics Society 2011 Graduate Student Fellowship amongst others awards.

Thursday, April 15, 2021

Photonic Analog Signal Processing for Neuromorphic Computing

8:50am PDT, 11:50am EDT, 4:50pm BST, 5:50pm CEST, 11:50pm Asia

Bert Jan Offrein
IBM Research Institute,
Zurich, Switzerland

Abstract

The power consumption and related carbon emission of neural network training and inference is a tremendous challenge. Novel dedicated hardware based on analog signal processing and in-memory computing concepts provide a path to more efficient neuromorphic computing. Implementations in integrated photonics for convolution signal processing and neural network training will be discussed.

Speaker Bio:

Bert Offrein received his Ph.D. degree in nonlinear integrated optics from the University of Twente (NL) in 1994. He then joined IBM Research - Zurich and contributed to establishing and commercializing adaptive integrated optical technology for DWDM networks. From 2004 to 2016, Bert Offrein was managing the photonics group, addressing optical interconnects for computing systems. Since 2016, he is leading the neuromorphic devices and systems group, focussing on novel hardware for neural networks. Bert Offrein is a principal research staff member at IBM Research and the co-author of over 150 publications and the co-inventor of more than 35 patents.

Thursday, April 15, 2021

Cross-Layer Design of Deep Learning Accelerators with Silicon Photonics

9:10am PDT, 12:10am EDT, 5:10pm BST, 6:10pm CEST, 12:10am Asia

Sudeep Pasricha
Colorado State University,
Fort Collins, Colorado, United States

Abstract

Domain-specific deep learning accelerators have seen growing interest in recent years due to their improved energy-efficiency and inference performance compared to CPUs and GPUs. In this talk, I will discuss our recent work on a novel cross-layer optimized deep learning accelerator called CrossLight that leverages silicon photonics. CrossLight includes device-level engineering for resilience to process variations and thermal crosstalk, circuit-level tuning enhancements for inference latency reduction, and architecture-level optimization to enable higher resolution, better energy-efficiency, and improved throughput. On average, CrossLight offers 9.5x lower energy-per-bit and 15.9x higher performance-per-watt at 16-bit resolution than several state-of-the-art photonic deep learning accelerators.

Speaker Bio:

Sudeep Pasricha (sudeep@colostate.edu) is a Walter Scott Jr. College of Engineering Professor in the Department of Electrical and Computer Engineering, the Department of Computer Science, and the Department of Systems Engineering at Colorado State University. He is Director of the Embedded, High Performance, and Intelligent Computing (EPIC) Laboratory and the Chair of Computer Engineering. He received the B.E. degree in Electronics and Communication Engineering from Delhi Institute of Technology, India, in 2000, and his Ph.D. in Computer Science from the University of California, Irvine in 2008. His research broadly focuses on software algorithms, hardware architectures, and hardware-software co-design for energy-efficient, fault-tolerant, real-time, and secure computing. These efforts target multi-scale computing platforms, including embedded and Internet of Things (IoT) systems, cyber-physical systems, mobile devices, and datacenters. He has published more than 200 research articles in peer-reviewed conferences and journals, which have received 7 best paper awards and multiple best paper award nominations. He has also been recognized with several awards for his research, including the 2019 George T. Abell Outstanding Research Faculty Award, the 2018 IEEE Computer Society TCVLSI Mid-Career Research Achievement Award, the 2015 IEEE TCSC Award for Excellence for a Mid-Career Researcher, and the 2013 AFOSR Young Investigator Award. He is currently a Senior Associate Editor for the ACM Journal of Emerging Technologies in Computing (JETC), and an Associate Editor for multiple IEEE/ACM journals. He is an ACM Distinguished Member and a Senior Member of IEEE.

Thursday, April 15, 2021

Countering Variations and Thermal Effects for Accurate Optical Neural Networks

9:30am PDT, 12:30am EDT, 5:30pm BST, 6:30pm CEST, 12:30am Asia

Grace Li Zhang
Technical University of Munich,
Munich, Germany

Abstract

Optical neural networks (ONNs) have emerged as a promising high-performance computing platform to accelerate deep neural networks. However, ONNs are very sensitive to process variations and thermal effects. This sensitivity leads to a significant degradation of inference accuracy of ONNs and thus renders them unusable in practice. In this talk, a framework to calibrate process variations and counter thermal effects is presented. This framework can recover the inference accuracy of ONNs under variations and thermal effects up to the level of the accuracy after software training, so that ONNs can provide their high bandwidth for neural network acceleration without sacrificing the accuracy.

Speaker Bio:

Grace Li Zhang received the Dr.-Ing. degree from the Technical University of Munich (TUM), Munich, Germany, in 2018. She is currently a postdoctoral researcher pursuing Habilitation at the Chair of Electronic Design Automation, TUM, where she leads the research team on heterogeneous computing. Her research interests include neural networks and neuromorphic computing, computer architectures, and machine learning for EDA. She has served/is serving on the technical committee of several conferences including ICCAD, ASP-DAC, GLSVLSI etc.

Registration Information

OPTICS 2021 will be conducted virtually using Zoom. There will be no charge to attend the workshop.

Access information will be sent to all registered participants, probably one day before the workshop.

To attend, please register yourself here: https://forms.gle/X8GDNVW5k5B8HNZ78

Registration deadline: April 12, 23:59 PDT.