Towards Error-Free Photonic Interconnects

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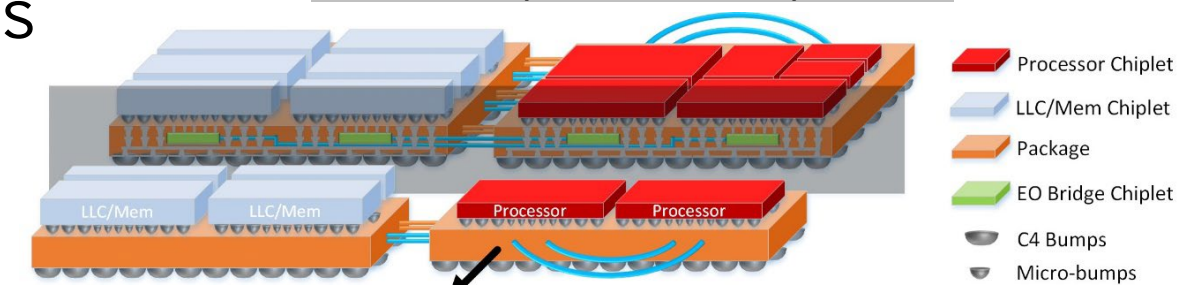
Photonics can Complement Electronics

- Electronics is good for computation and memory
- Photonics is good for communications

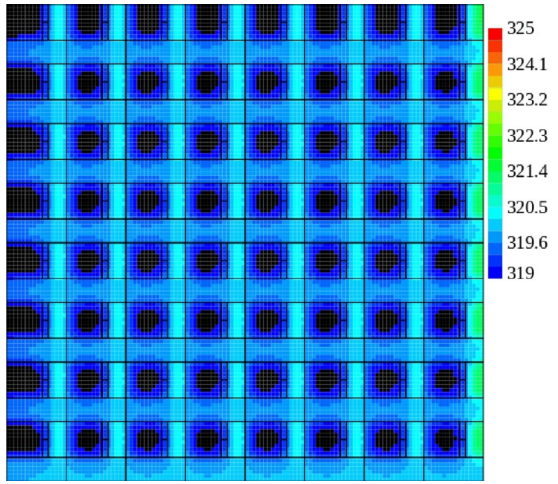
+ Advantages
  + Ultra-high bandwidth
  + Low propagation delay
  + Low propagation loss
  + Low sensitivity to environmental EMI

- Challenges
  - Thermal variation -> errors and even failures
  - Crosstalk noise
  - Process variation
  - Nonlinear effects
  - Difficult to buffer
  - OE conversions

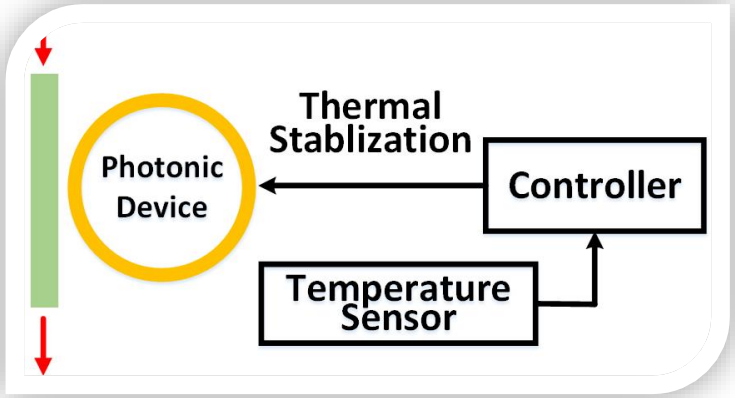
Photonic Chiplet-Based Multiprocessor

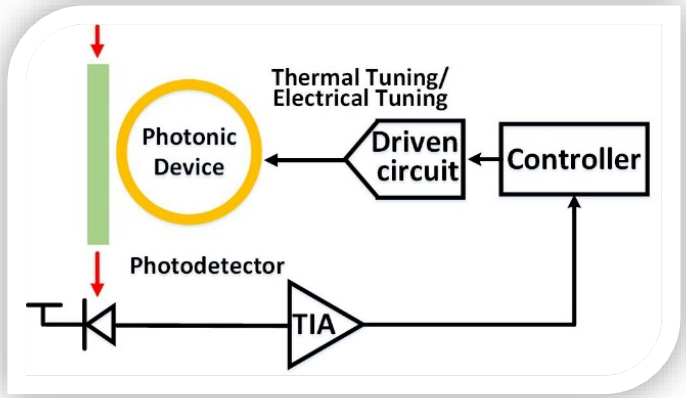


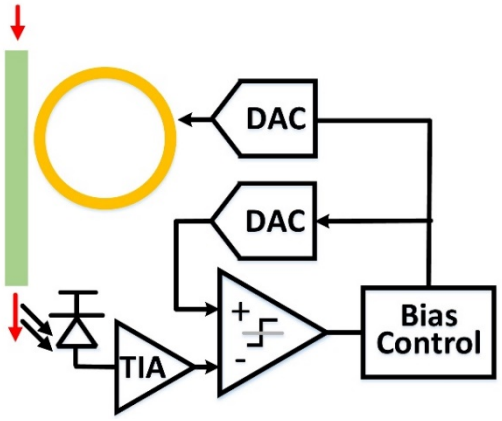
Thermal Variation on a Chip



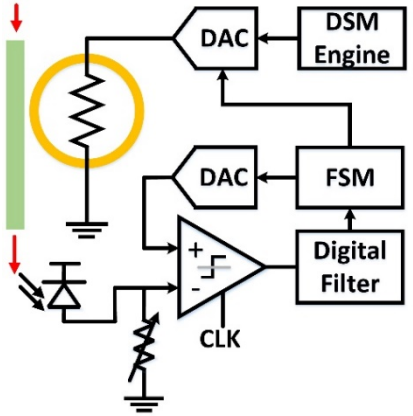
Thermal Stabilization vs. Device Turning



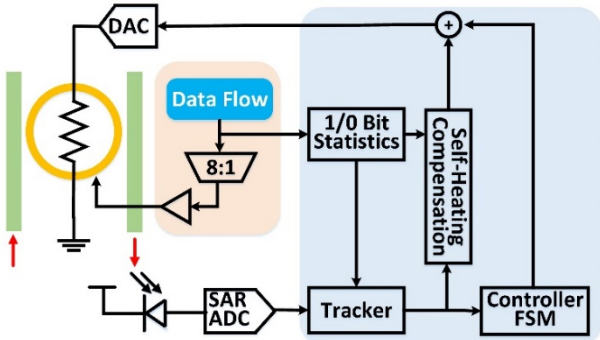




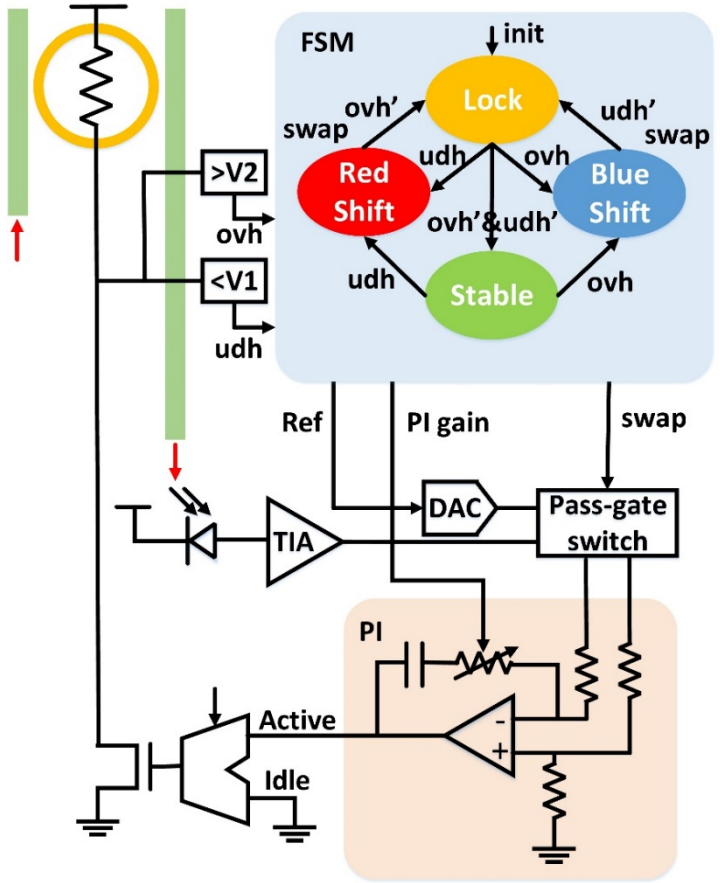
C. Li *et al*, JSSC 2014



K. Yu *et al*, ISSCC 2015



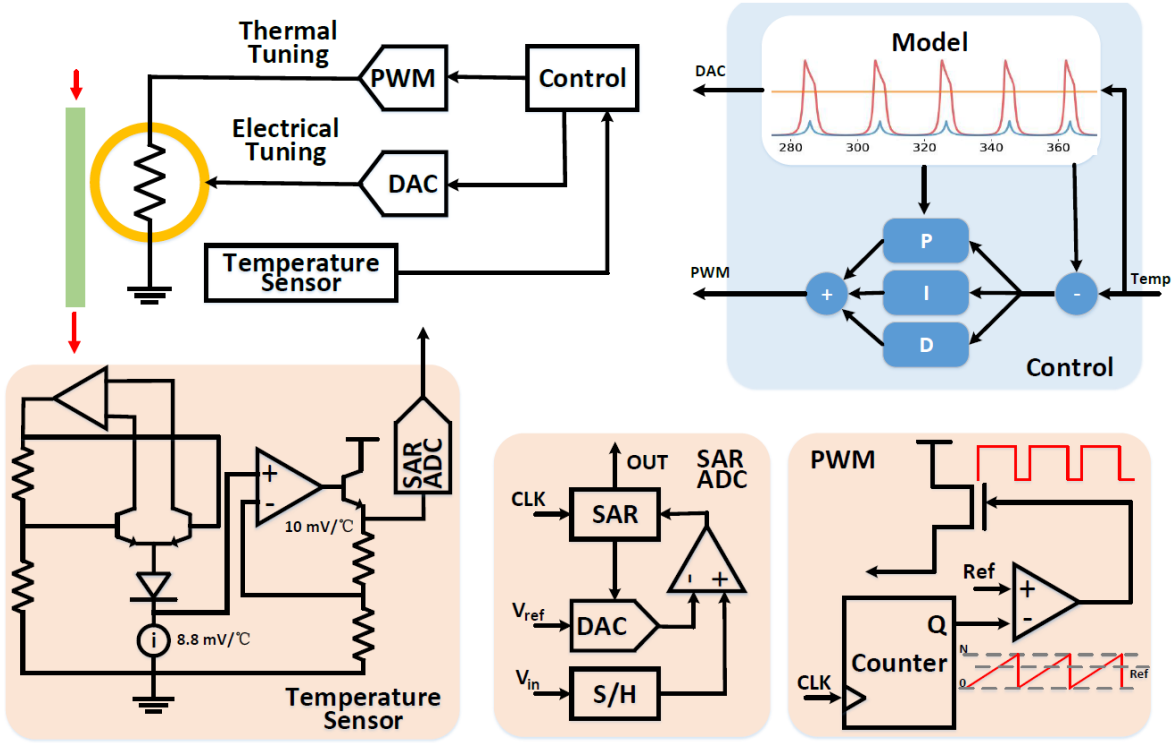
C. Sun *et al*, JSSC 2016



Y. Thonnart *et al*, ISSCC 2018

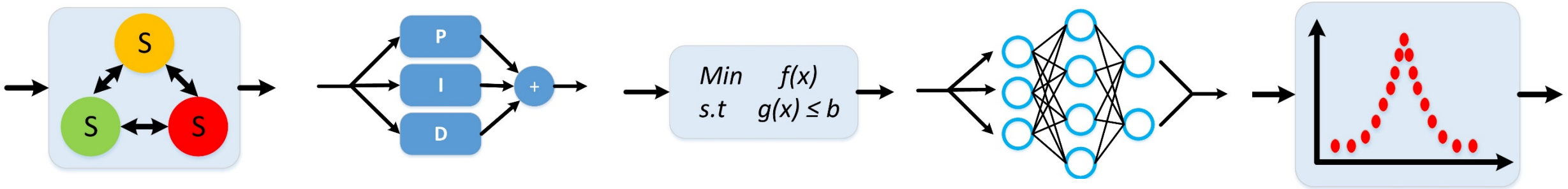
Indirect Feedback Tuning (IFT)

- Tune device characteristics based on device temperature
- Complemented electrical and thermal tuning
  - Electrical tuning is fast (*ns*) but has a small tuning range
  - Thermal tuning is slow (μs) but has a large tuning range
- More responsive
- Low cost and low power
- Do not need any optical port



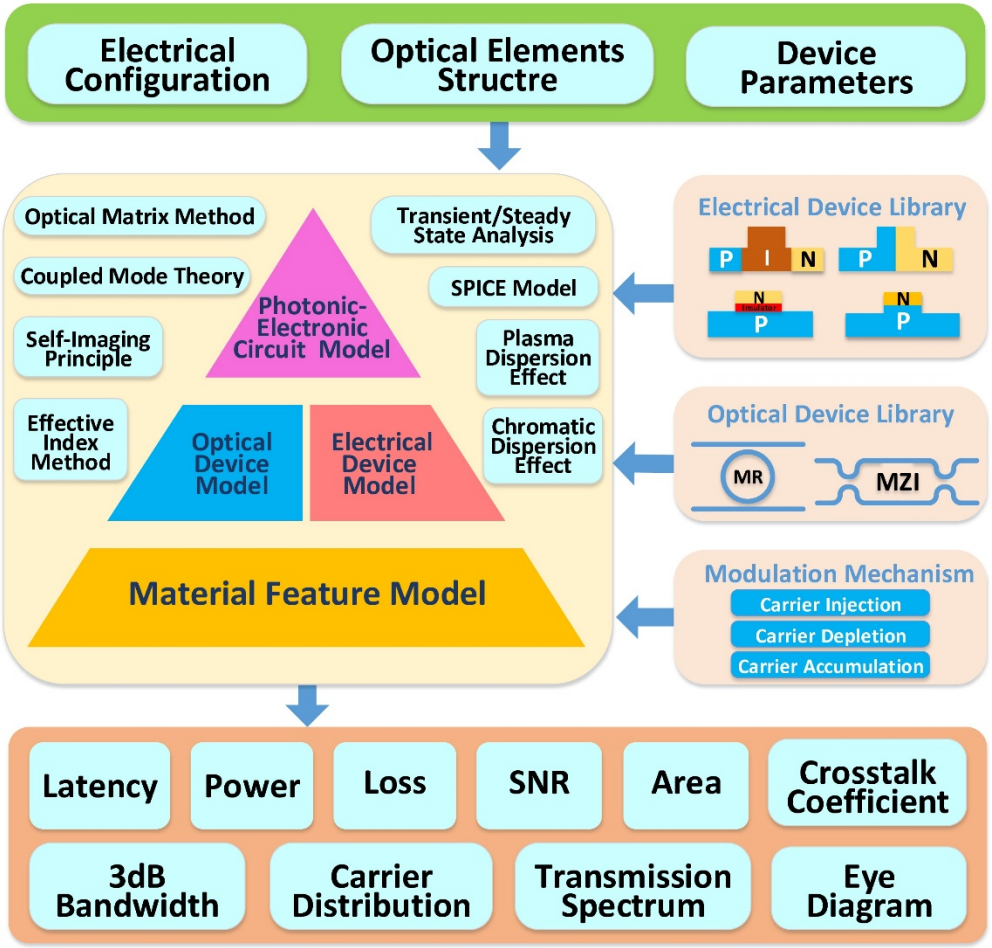
*X. Chen, *et al.* "Simultaneously Tolerate Thermal and Process Variations through Indirect Feedback Tuning for Silicon Photonic Networks," IEEE TCAD, 2020

IFT Control Logic



FSM	PID	Optimal Control	Q-Learning	Model Predictive
Pros				
HW-efficient	HW-efficient, no expertise knowledge	optimal point, cost function	Intelligent, no expertise knowledge	nonlinear control, prediction, HW-efficient,
Cons				
linear control, finite state, large granularity	linear control, oscillation issue, parameter tuning	hardware cost $O(n^{3.5})$, expertise knowledge	HW cost for large numbers of states/actions	Need a model

BOSIM is Used to Develop a Control Model



https://eexu.home.ece.ust.hk/BOSIM.html

- BOSIM is a photonic device design, modeling, and simulation tool
- Validated by fabricated devices from 8 companies and institutes
- Study transit and static device characteristics
- Understand device structures and material choices
- Accelerate design exploration

Component Design and System-level Simulation Setup

Circuit *							
	ADC	DAC	TIA	OA	Sensor [42]	PD	Calibration
Power (mW)	0.52	2.5	0.71	0.2	1.2	0.03	0.2
Area (μm^2)	183.4	138.3	123.5	123.5	48	10	183.4
Laser efficiency			0.33 [48]		Laser Extinction Ratio		10
Photodetector Sensitivity		-14.2 dBm (BER 10^{-12})[49]			Communication Band		O-Band

Switch °			
WDM channel amount	14	Ring Radius	near 10 μm
Phase Shifter			
Rib Width	0.4 μm	Film Height	0.4 μm
Etching Depth	0.3 μm	Cladding Height	1.2 μm
PN Horizontal Offset	-0.15 μm	PN Vertical Offset	0.1 μm
Directional Coupler			
Length	0.1 μm	Gap	0.18 μm
Doping			
Device Type	L-shaped PN	Modulation Mechanism	Carrier Depletaion
P-area-NA	1.0×10^{18} cm^{-3}	N-area-ND	2.0×10^{18} cm^{-3}
P-area-x	0.6 μm	N-area-x	0.6 μm
SPICE Model			
τ	0.5 ns	R_S Series Resistance	55 Ω
I_S	1.0×10^{-8} μA	n_{pn}	1
V_0	1.0 V	$C_j(0)$	0.4 pF
IBV	1000 μA	BV	40.0 V
DC Bias	-4 V	Vpp	11 V

Material	substrate/cladding	guiding film	air
refractive index	SiO_2: 1.45	Si: 3.45	1
absorption (mm^{-1})	N.A.	0.015	N.A
thermal diffusivity (mm^2/s)	SiO_2: 0.83	Si: 88	19
permittivity ($\epsilon_0 = 8.854 \times 10^{-14}$)	$3.9\epsilon_0$	$11.7\epsilon_0$	ϵ_0

System level simulations use

- JADE multiprocessor simulation environment
- COSMIC application benchmark suite

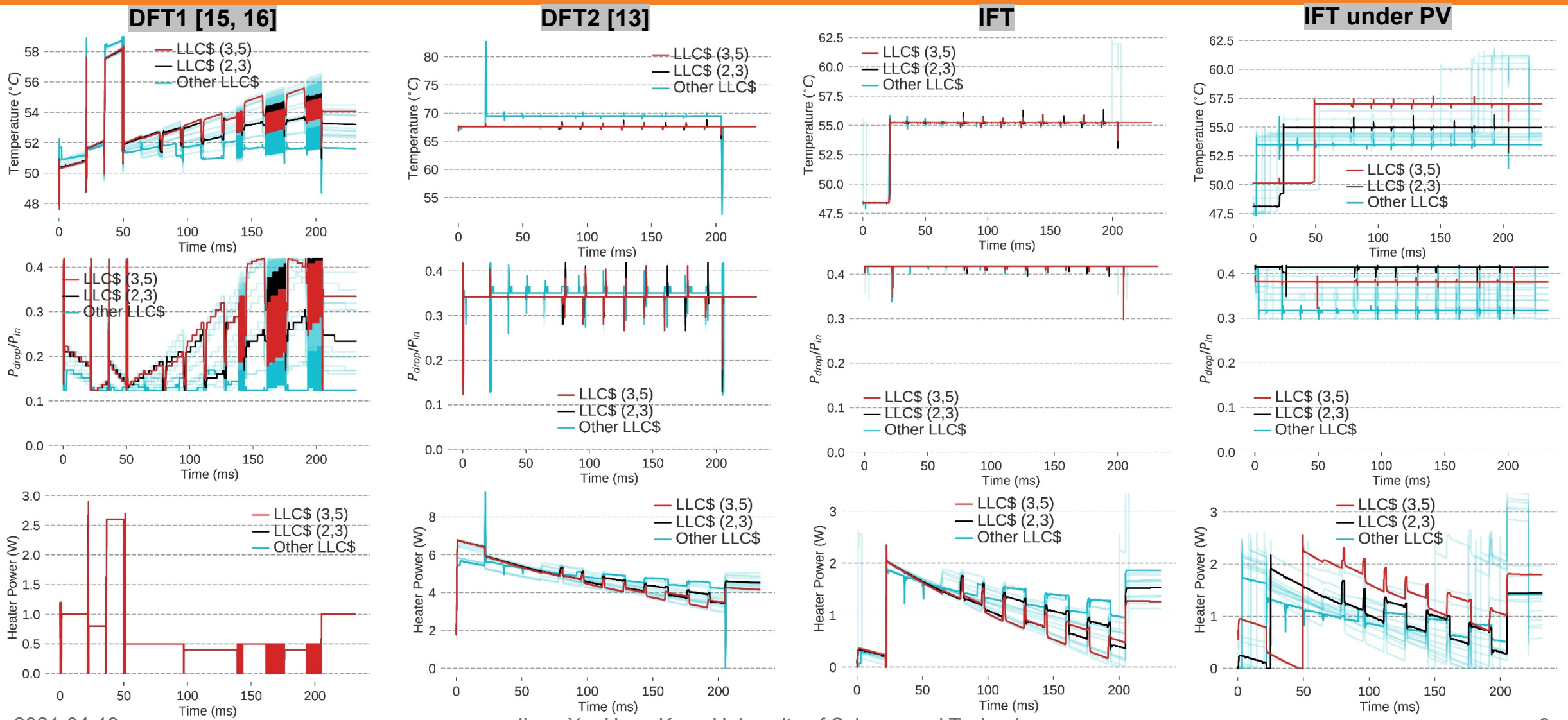
Parameter	**Value**	**Parameter**	**Value**
Architecture			
Core	RISC-V, 64-Core	Working frequency	3 GHz
Core cluster	4 core/cluster	L1 I/D cache	Private, 32 KB/Core
L2 cache	Shared, 128 KB/Core	Coherence Protocol	Directory-based MOSI
Cache line size	64 Byte	NoC Topology	Ring

Variation					
wafer diameter		200 mm	chip die area		236.7 mm^2
chip thermal threshold		354.95 K			
Process Variation †					
	linewidth	gap	film thickness	waveguide loss	dopant
noise type	Simplex	Simplex	Joint Gaussain	Simplex	Perlin
noise radius	20 mm	20 mm	N.A.	30 mm	N.A.
noise amplitude PV1	2.4 nm	1 nm	2 nm	1.5 dB	$10^{17} cm^{-3}$
noise amplitude PV2	1.6 nm	0.6 nm	1.2 nm	1.0 dB	$10^{17} cm^{-3}$

Thermal Variation ‡	silicon chip	heat sink	spreader
thermal conductivity ($W/(m \cdot K)$)	100.0	400.0	400.0
specific heat ($J/(m^3 \cdot K)$)	1.75×10^6	3.55×10^6	3.55×10^6
thickness (mm)	0.15	6.9	1.0
side (mm)	N/A	60	30

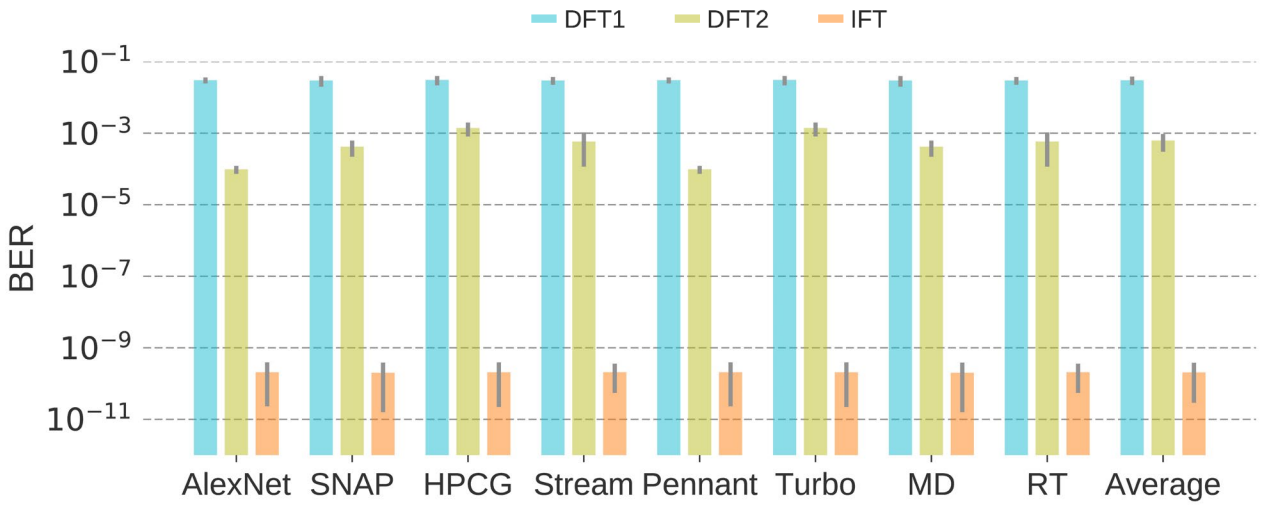
heat sink convection resistance	0.1 K/W	heat sink convection capacitance	140.4 J/K

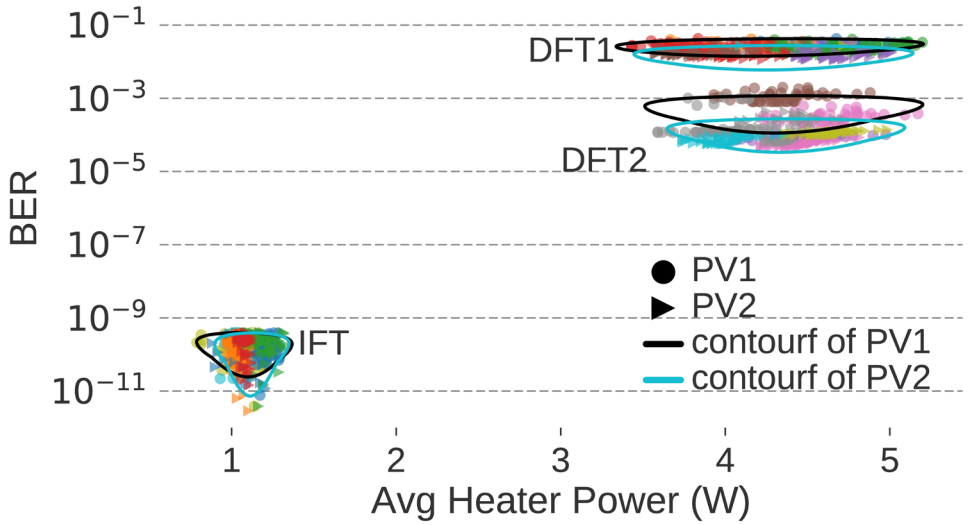
Case Analysis: SNAP Benchmark



Bit Error Rate

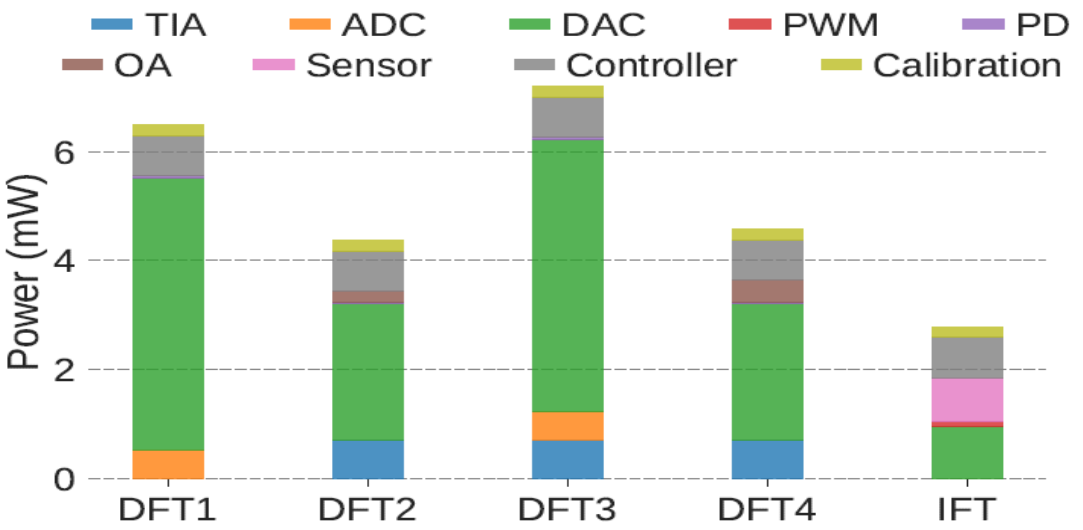
- IFT can achieve BER better than 10^{-9}
  - Based on the simulation results under COSMIC benchmark suite
- IFT shows 10^{5}~10^{8} improvement over other methods
- IFT is robust under process variations

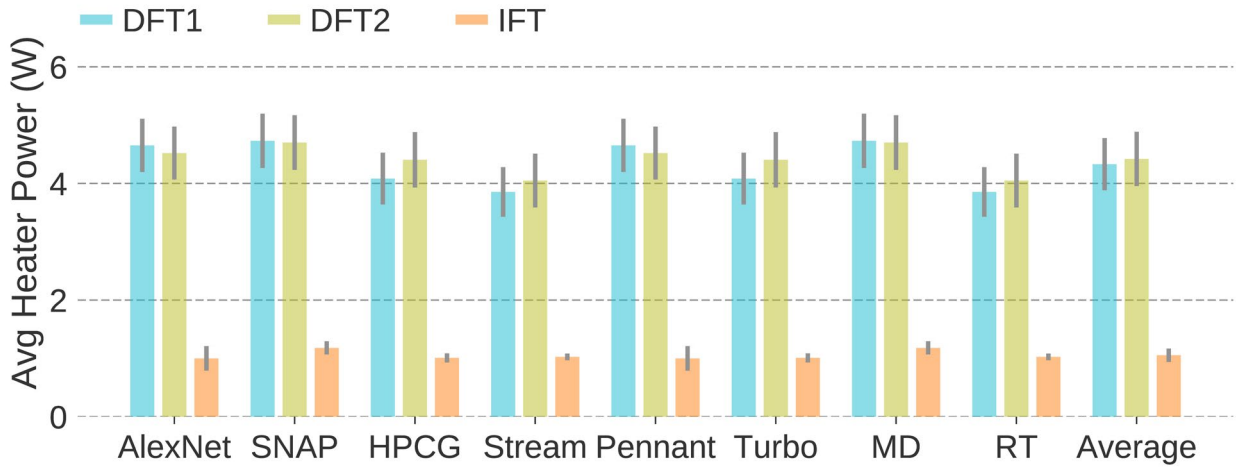


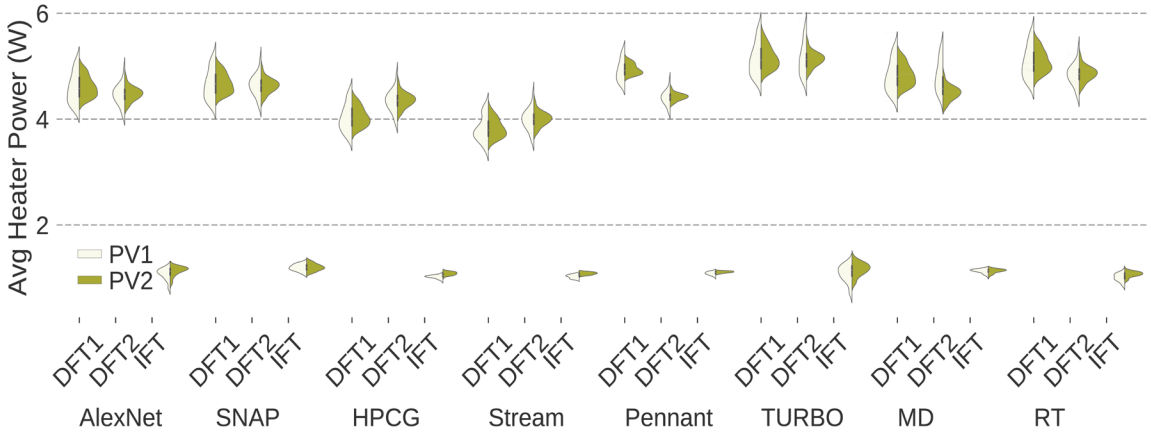


Power Overhead

- Dominated by heater power
- IFT is up to 4X more power efficient than other methods
- IFT is more robust under process variations than other methods

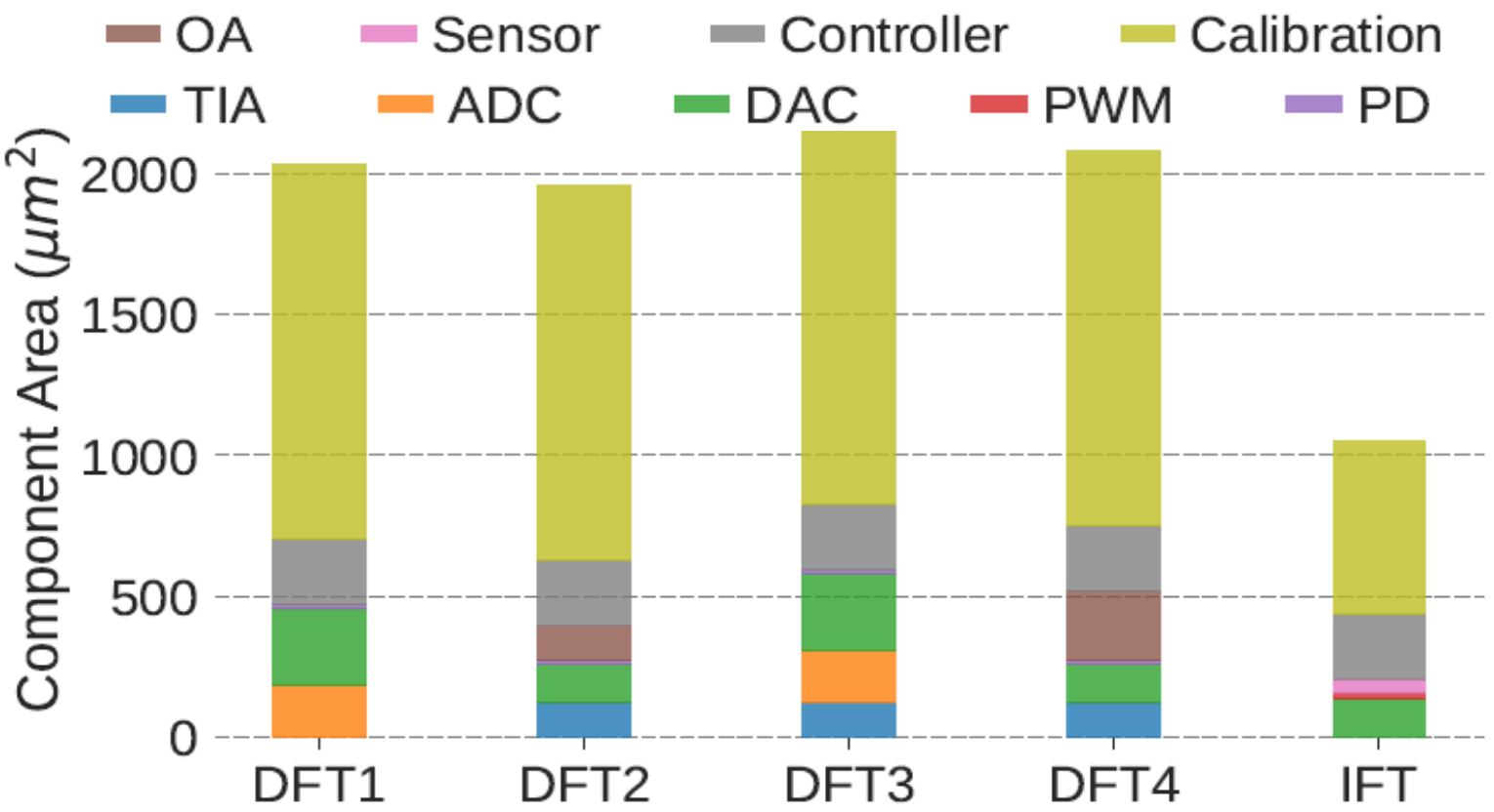






Area Overhead

- IFT is up to 51% smaller than other methods



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Thanks!