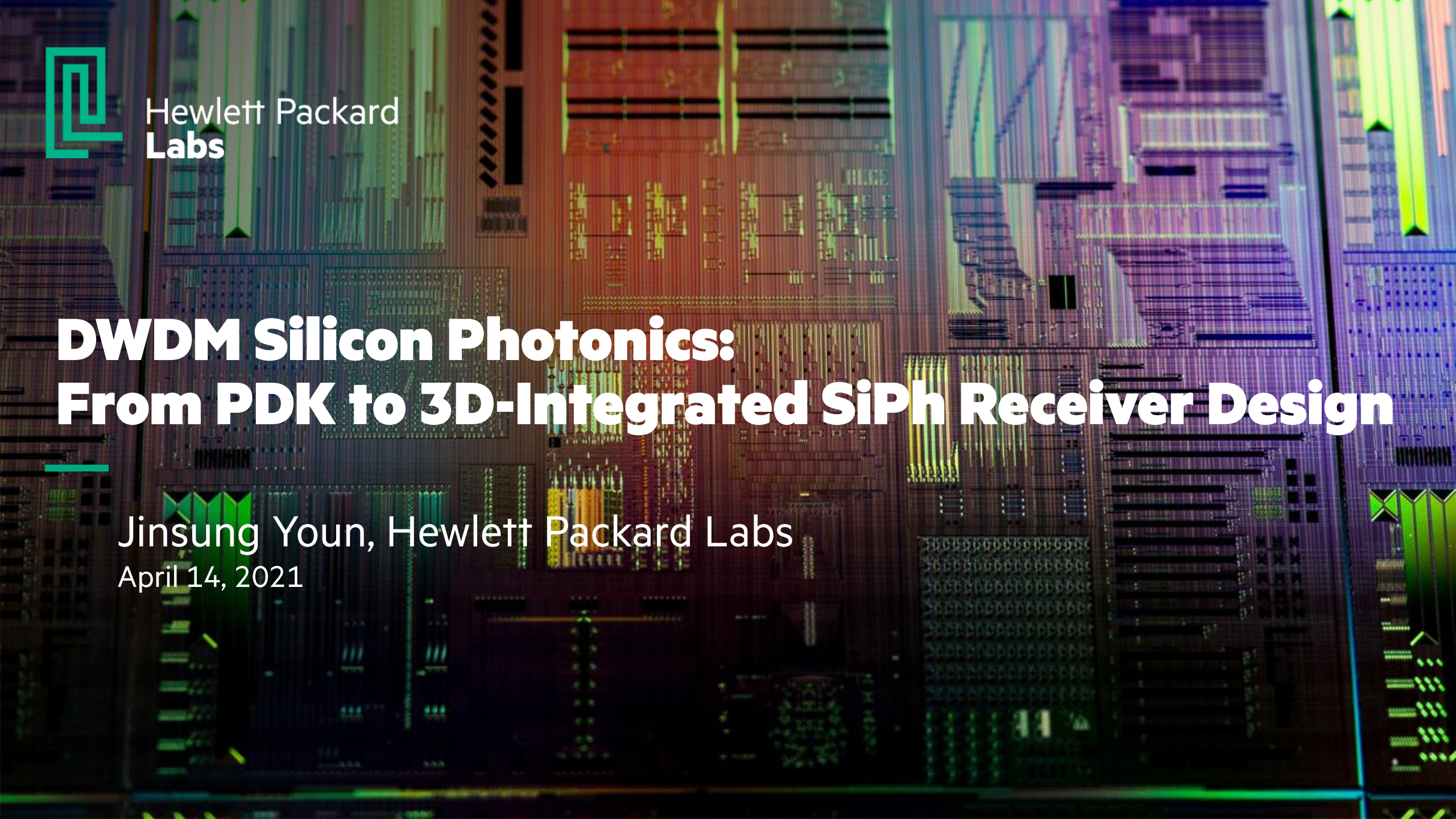

Hewlett Packard Labs

DWDM Silicon Photonics: From PDK to 3D-Integrated SiPh Receiver Design

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April 14, 2021

Outline

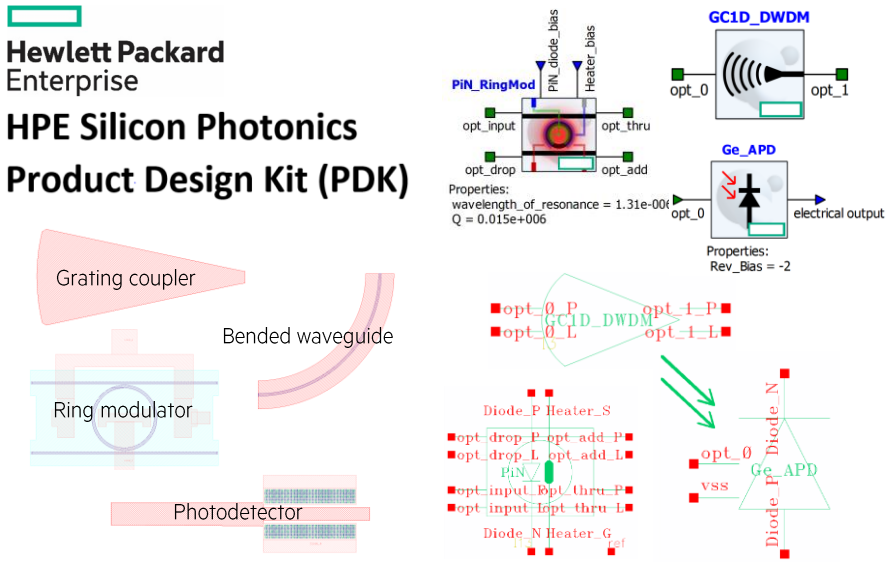
- **HPE Silicon Photonics (SiPh) Research**
- **HPE SiPh PDK**
  - One example: Photodetector behavioral model for receiver design
- **3D-Integrated DWDM Receiver Design**
- **Summary**

HPE SILICON PHOTONICS RESEARCH

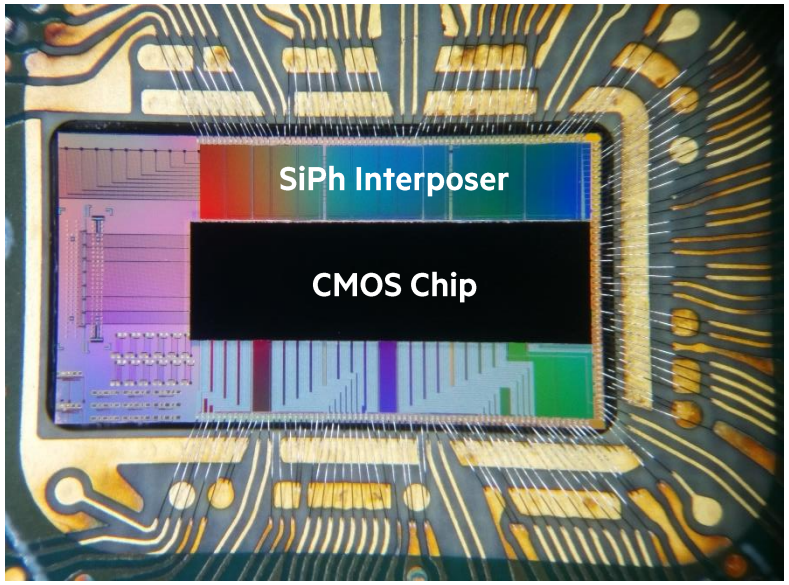
- **Silicon Photonics PDK development**
  - To lower the entry barriers for Silicon Photonic design

- **3D-integrated DWDM SiPh transceiver design**
  - Microring-based optical link to achieve high aggregate bandwidth in a small form factor

SiPh PDK development



DWDM SiPh design



PROCESS DESIGN KIT

- **What is a PDK?**
  - PDK is a set of files used within the semiconductor industry to model a fabrication process **for the design tools** used to design an integrated circuit. The designers use the PDK **to design, simulate, draw and verify the design** before handling the design back to the foundry to produce chips. The data in the PDK is specific to the foundry's **process variation** and is chosen early in the design process. An **accurate PDK** will increase the chances of first-pass successful silicon (Source: *Wikipedia*)

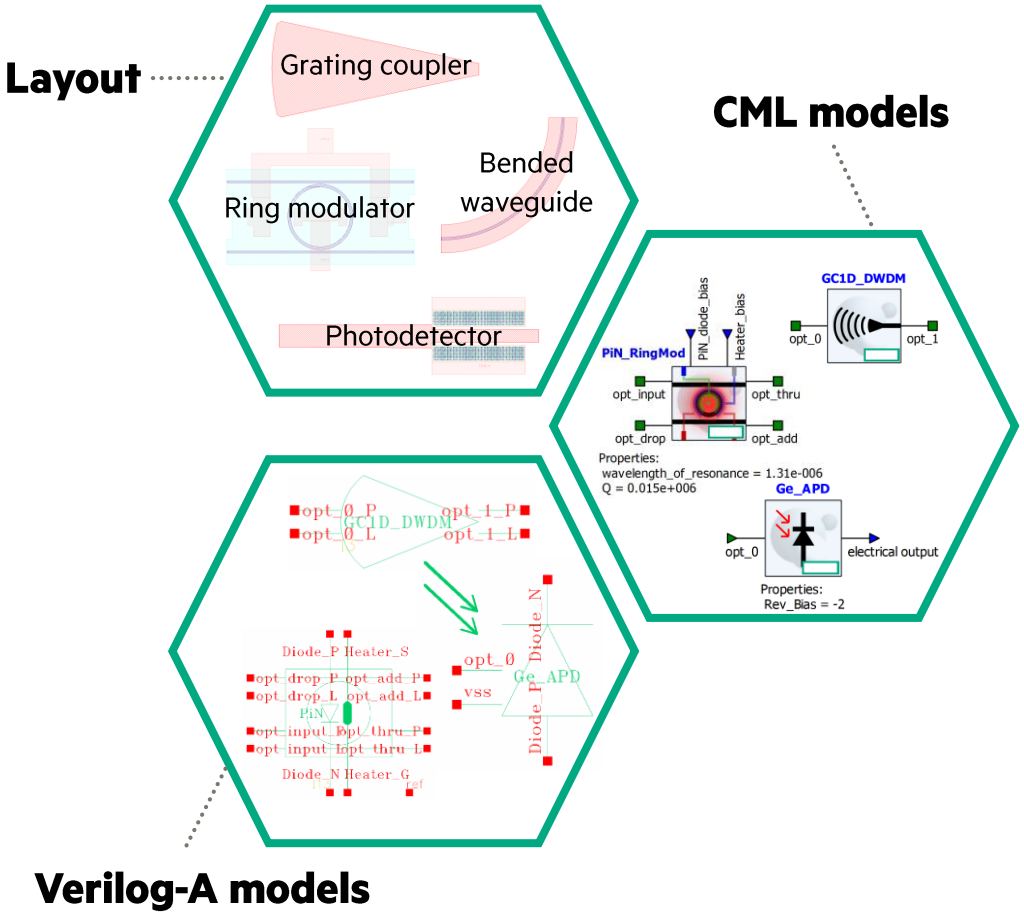
- **Key requirements**
  - Accurate simulation models
  - Compatibility with EDA tools
  - User-friendly interfaces
  - Statistical parameters

HPE'S SILICON PHOTONICS PDK

- **Schematic symbols and layouts**
  - Grating couplers
  - Passive devices
    - Waveguides, tapers, splitters …
  - Active devices
    - Modulators, photodetectors, phase shifters
  - Packaging devices
    - TSV, microbump, high-speed metal pads

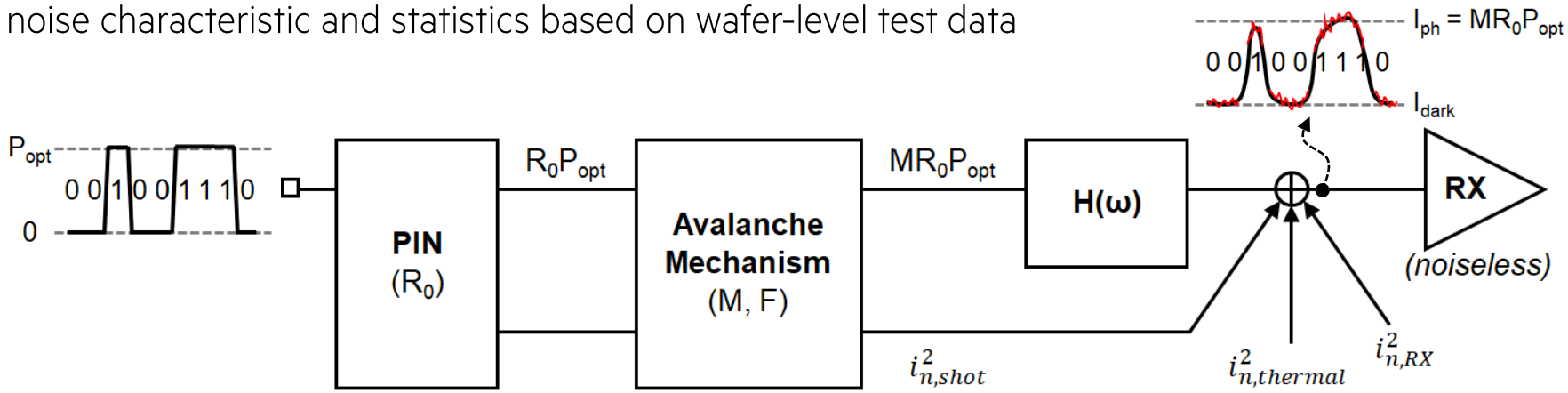
- **Behavioral models**
  - Verilog-A models for co-simulation with electronic circuits
  - CML models for system-level simulation

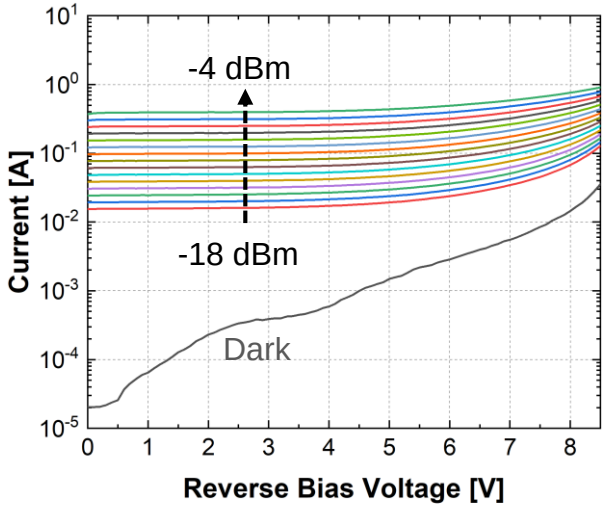
- **PDK manual**
  - Device parameters and wafer-level test data
  - Design guidelines

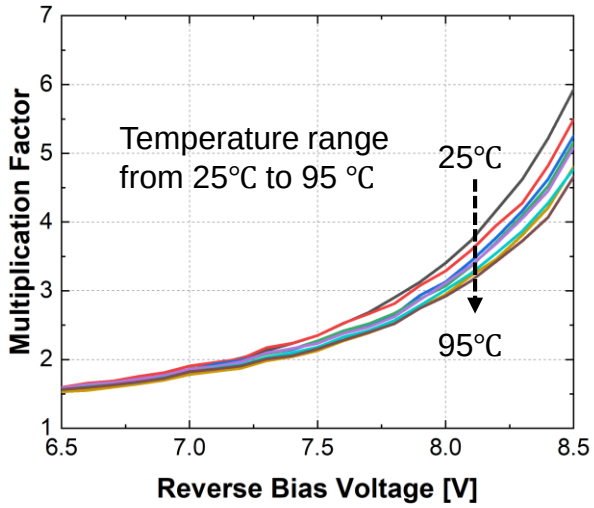


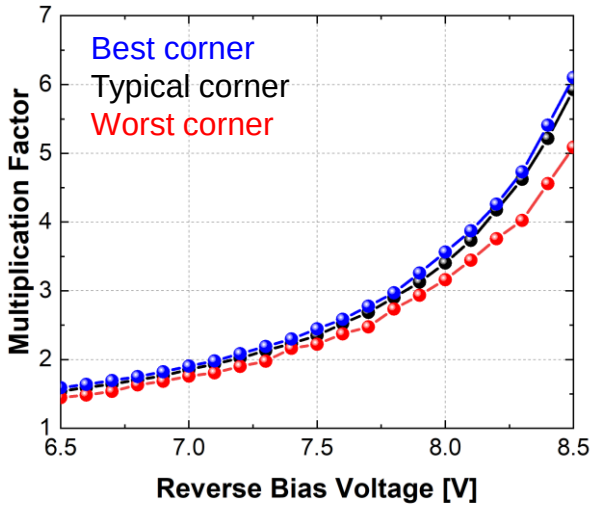
PHOTODETECTOR BEHAVIORAL MODELING

- **Accurate PD behavioral model over a wide range of bias voltages**
  - Included noise characteristic and statistics based on wafer-level test data





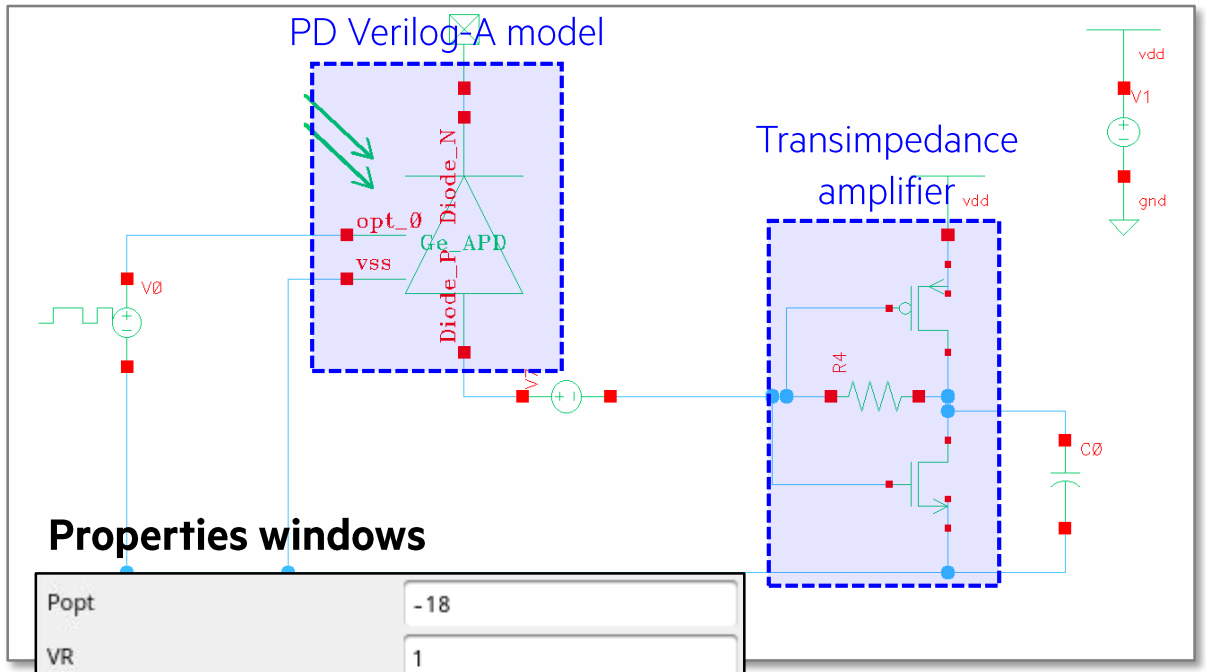




PHOTODETECTOR BEHAVIORAL MODELING (CONT'D)

- **User-friendly interface with Cadence Virtuoso**
  - Co-simulation with transistor-level electronic circuits

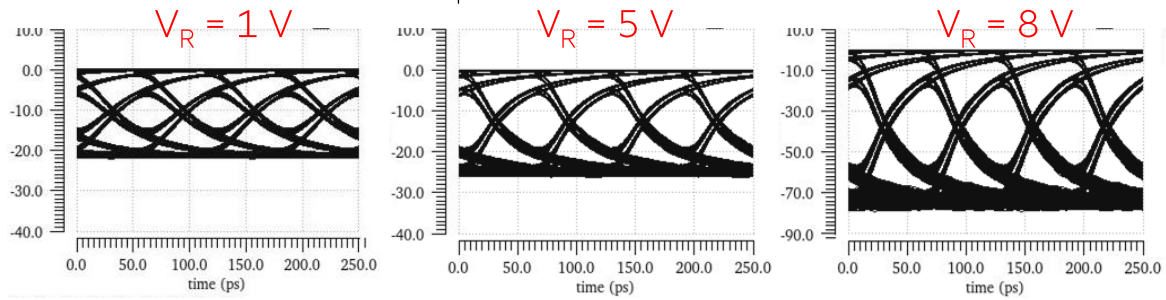
Cadence Virtuoso Schematic Editor



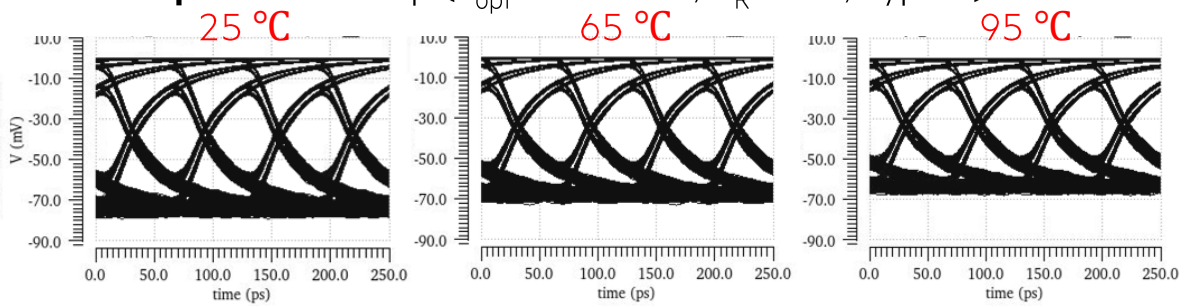
Properties windows

Popt	-18
VR	1
Temp	25
Corner	typ

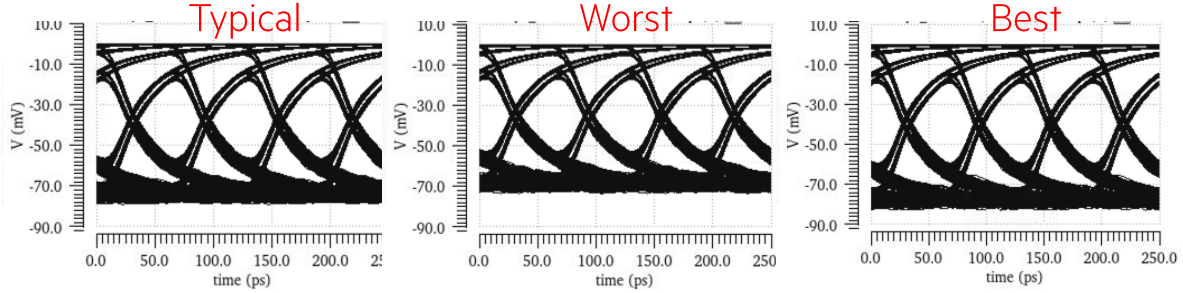
- **Bias voltage** sweep (P_{opt} = -18 dBm, 25℃, Typical)



- **Temperature** sweep (P_{opt} = -18 dBm, V_R = 8 V, Typical)

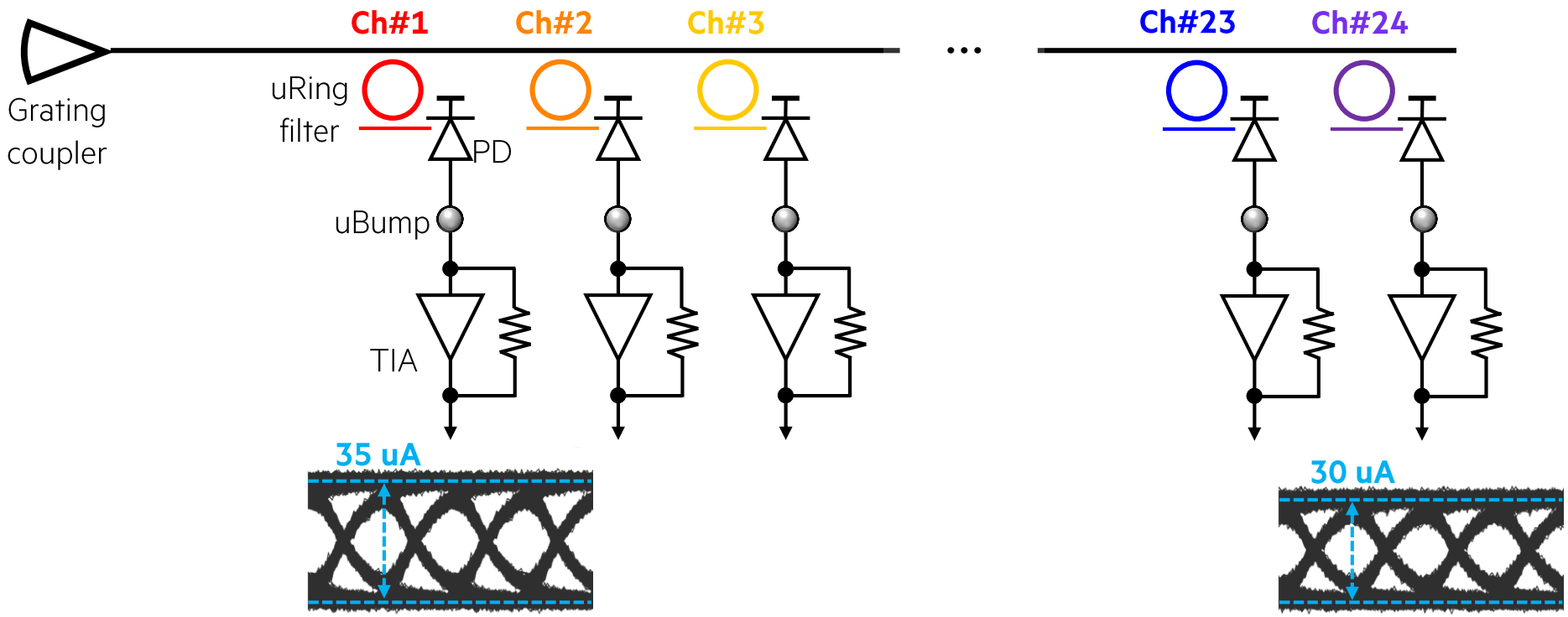


- **Process corner** sweep (P_{opt} = -18 dBm, V_R = 8 V, 25℃)



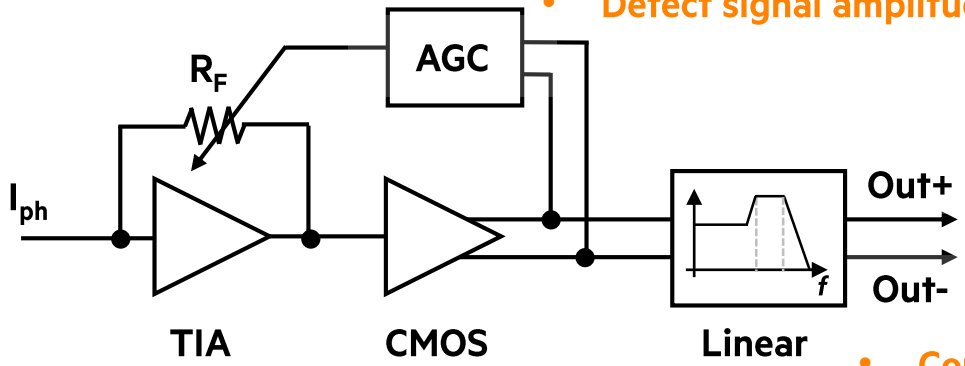
3D-INTEGRATED DWDM RECEIVER DESIGN

- **CMOS receiver chip is flip-chipped onto SiPh interposer**
  - CMOS receiver has 24 front-end channels operated at 16 Gb/s (≈ aggregate bandwidth of 384 Gb/s)
  - SiPh interposer has a single grating coupler and a bus waveguide with 24 microrings and 24 photodetectors
- **Transient simulation with Verilog-A models from PDK**



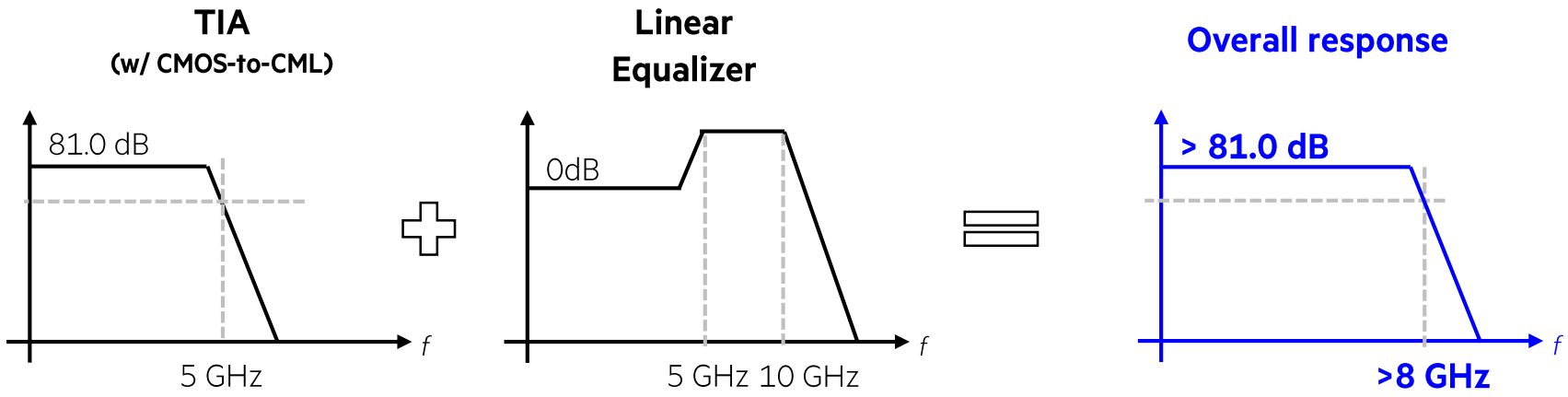
RECEIVER CIRCUIT DESIGN

- Wide input dynamic range
- Detect signal amplitude and control TIA gain



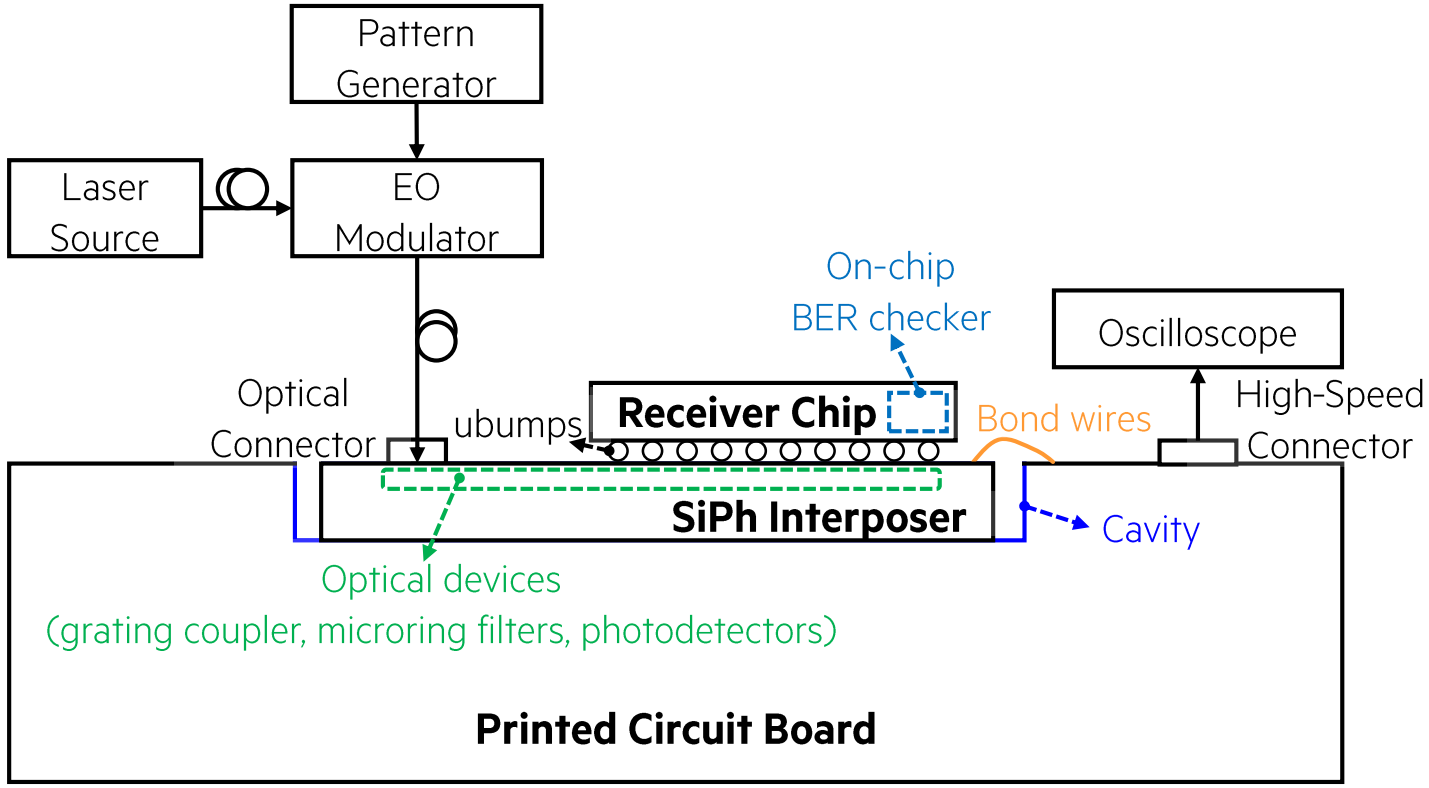
- Converts PD current to voltage signal
- High-gain and low-noise characteristics

- Compensate bandwidth limit due to TIA and packaging
- Boosting gain controllability to optimize bandwidth



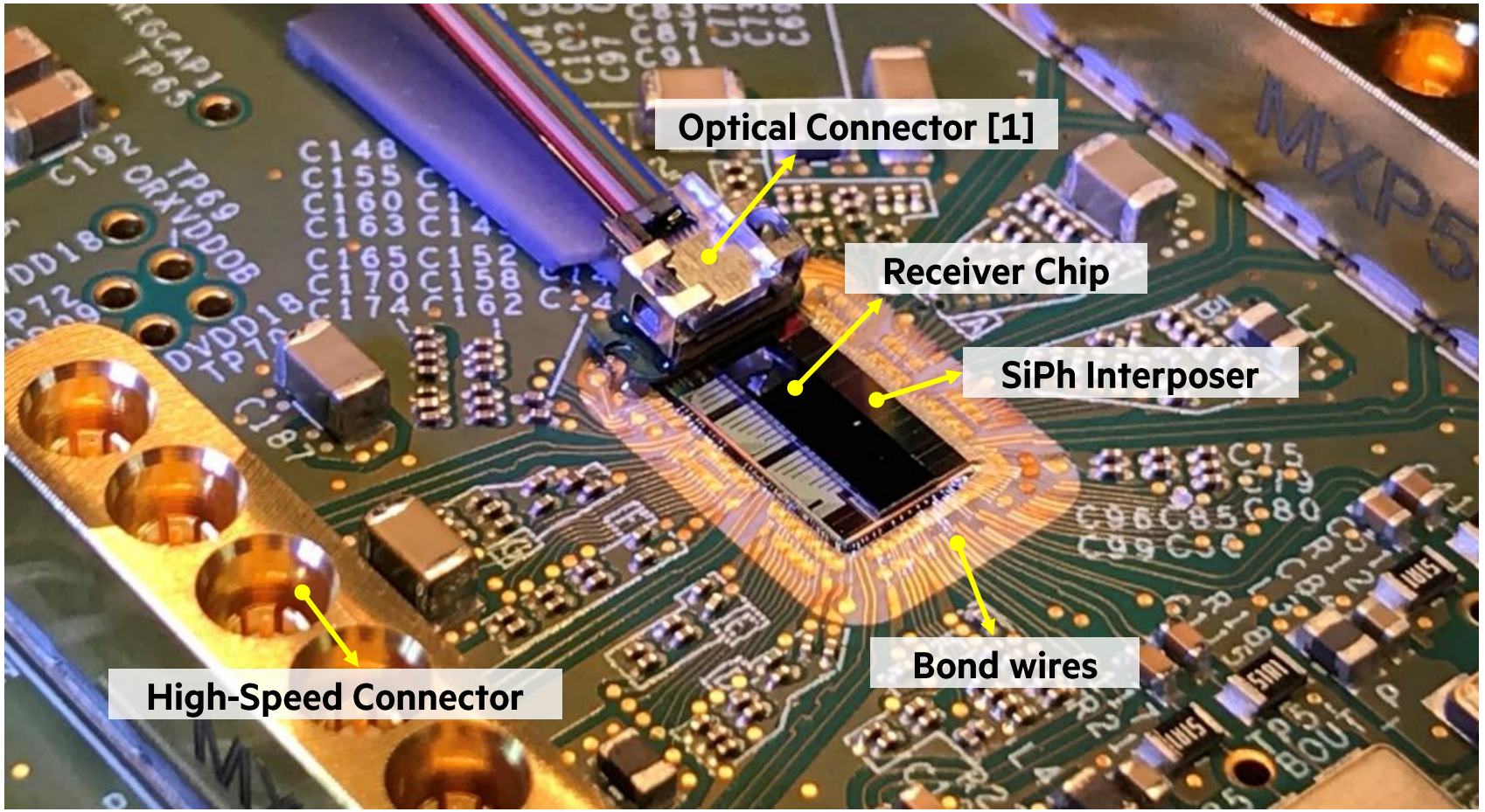
MEASUREMENT SETUP

- **CMOS receiver chip is flip-chipped onto SiPh interposer**
- **3D-integrated SiPh package is mounted and wirebonded to printed circuit board**
- **Power consumption: 384 mW with 1.2-V (≈ Energy efficient of 1 pJ/bit)**



MEASUREMENT SETUP (CONT'D)

- Picture of SiPh receiver mounted on the test board



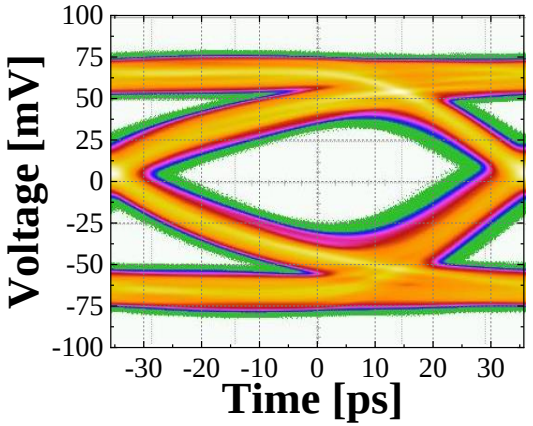
[1] S. Mathai, Optical Interconnects, 2020

MEASUREMENT RESULTS

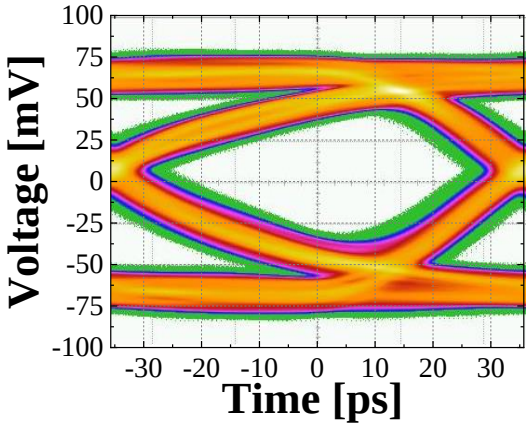
- **Measured 14- and 16-Gb/s eye diagrams at the first channel (λ = 1305.7 nm)**
- **Clean eye diagrams with optimized equalizer coefficients**
- **BER < 10^{-12} measured with on-chip BER checker**

14-Gb/s eye diagrams

Minimum EQ coefficient

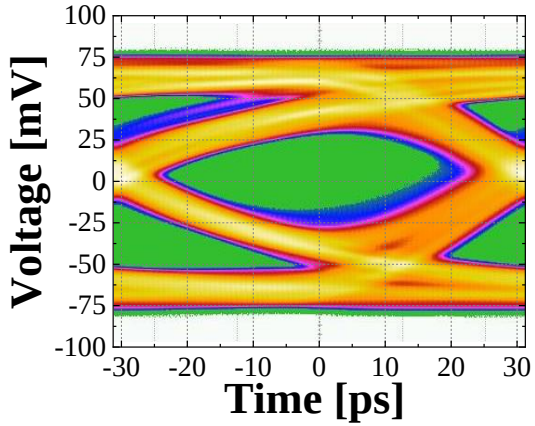


Optimal EQ coefficient

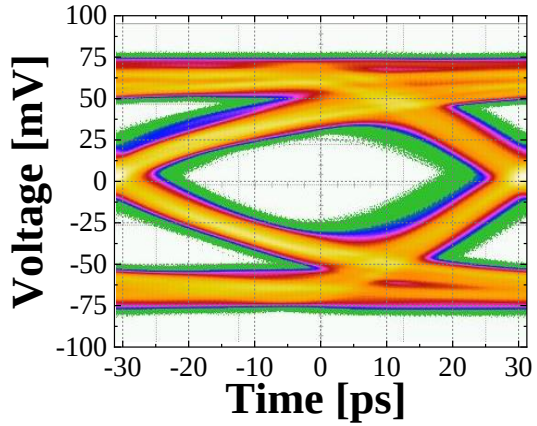


16-Gb/s eye diagrams

Minimum EQ coefficient



Optimal EQ coefficient



SUMMARY

- HPE's Silicon Photonics PDK
- 3D-Integrated SiPh Receiver Design
- Demonstration of 16-Gb/s optical data transmission with error-free condition
- SI/PI/TI analysis of 3D-integrated SiPh system will be presented at DesignCon2021

THANK YOU

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- Hewlett Packard Labs' R&D interests in EU: Photonics, AI & quantum computing
- Looking for consortium partners and EU funding opportunities!
  Thomas.Van-Vaerenbergh@hpe.com
- Upcoming special issue: APL photonics – Photonics and AI in IT, deadline July 9