OPTICS

Optical/Photonic Interconnects for Computing Systems

Si, SiN, and Glass Photonics Prototyping Services at CMP

Kholdoun TORKI

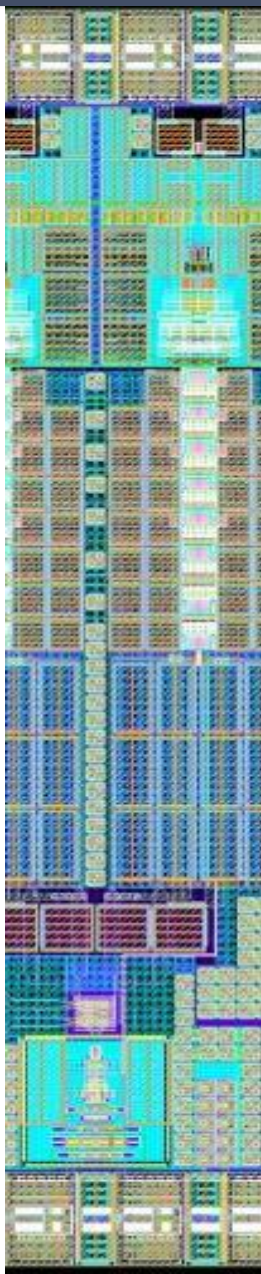
CMP

Circuits Multi-Projets®
46, Avenue Félix Viallet,
38031 Grenoble, France
https://mycmp.fr
Kholdoun.Torki@mycmp.fr

Horizon 2020
European Union funding
for Research & Innovation

Outline

- Introduction : CMP General Presentation
- CEA-LETI Process offer overview
- AMF Process offer overview
- TEEM Photonics process offer overview
- Photonics Packaging / System Integration

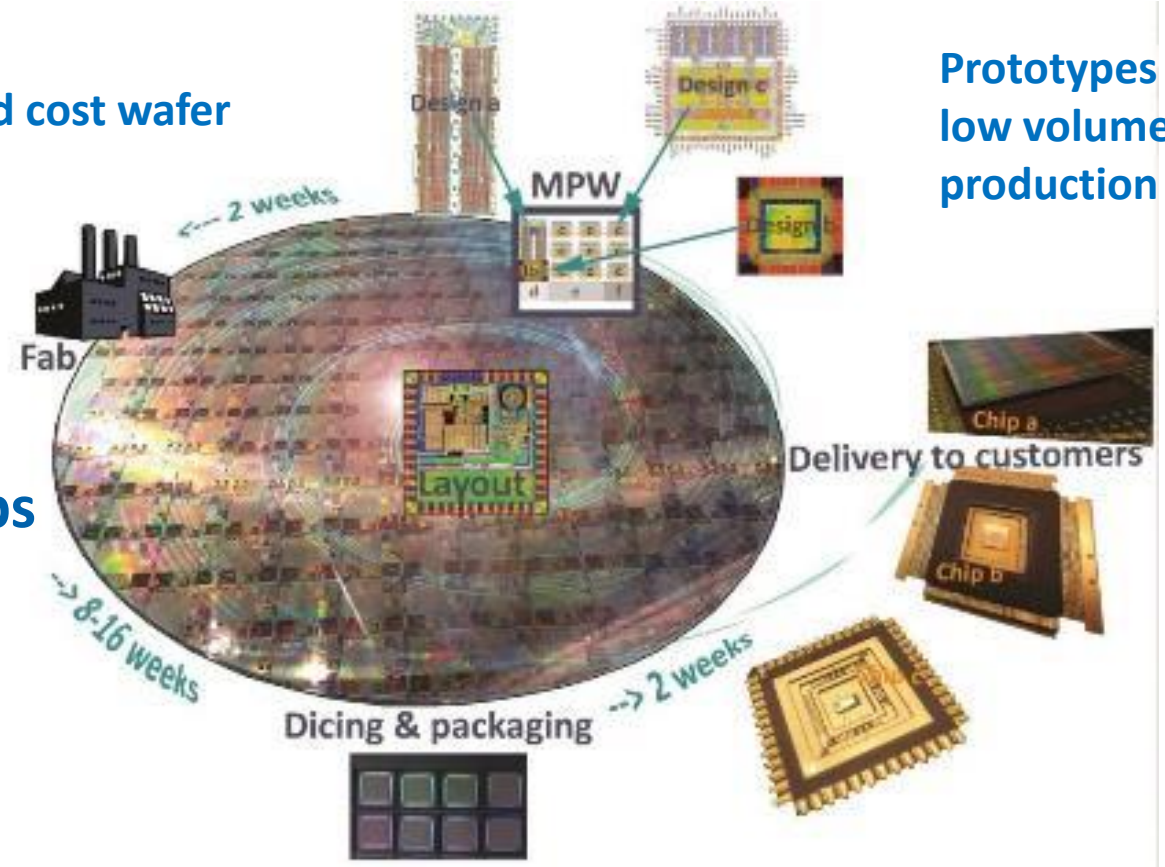


MPW services for prototyping and Low Volume Production

CMP makes available and affordable **advanced CMOS, MEMS, Photonics technologies** as well as **mature and/or niche market technologies** to cover a wide range of applications.

Shared cost wafer

Prototypes or low volume production



Affordable prototyping service

CMP shares manufacturing cost of ICs prototyping and small volumes.

From layout to chips

Technical supports

CMP provides supports & training for Design Kit implementation and usage

CMP offers several companion services for packaging and test.

Technology Portfolio in 2021 (1/2)

IC

ams	0.35µ CMOS 4LM 0.35µ CMOS-Opto 4LM	0.35µ SiGe 4LM 0.35µ HV-CMOS (50V / 120V)
ST	65nm CMOS 7LM 130nm CMOS 6LM 130nm HV-CMOS 4LM	28nm FDSOI 130nm SOI - FEM 0.16µ BCD-SOI	55nm SiGe BiCMOS 130nm SiGe BiCMOS 0.16µ BCD
ON Semi	0.18µ CMOS 5LM 0.35µ CMOS 4LM	0.18µ HV-CMOS (45/70V) 0.35µ HV-CMOS (25/50V)
EM Microelectronic	0.18µ CMOS 5LM (ULP / ULV)	

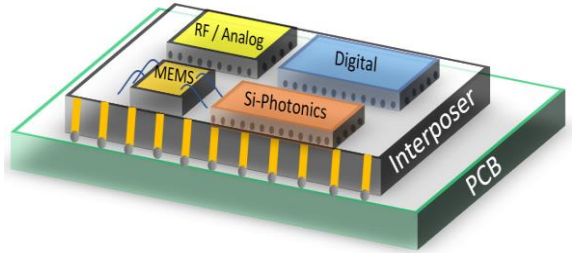
MEMS

CMP / ams	0.35 µ CMOS front-side bulk micromachining		
MEMSCAP	PolyMUMPS	SOIMUMPS	PiezoMUMPS

Technology Portfolio in 2021 (2/2)

Photonics	CEA-LETI	Silicon Photonics / Si-310 / Si-220 / SiN4-800
	AMF / CMC	Silicon Photonics / SiP
	TEEM Photonics	Photonics on Glass / ioNext-NIR / ioNext-VIS / WAFT

3D-IC	CEA-LETI	UBM, micro-bumps, RDL, TSV / 3D assembly / Open3D
	ams	0.35um 4 LM Active or Passive Interposer + UBM
	ams	UBM + Bumps at Wafer Level on 0.35µ
	ST	UBM + Copper pillar at Wafer Level (processes on 300mm wafers)
	ON Semi	Passive Interposer + UBM



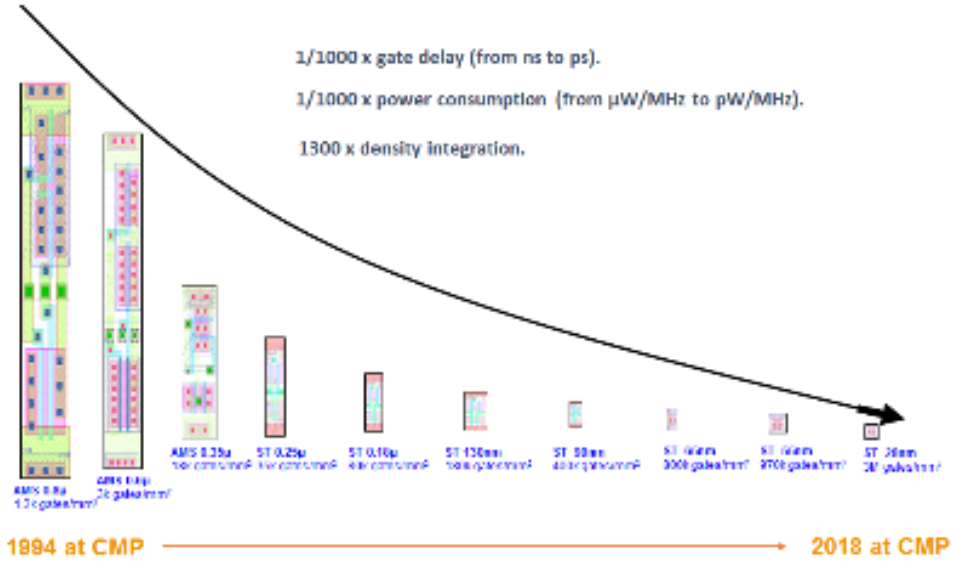
History of CMP technology portfolio

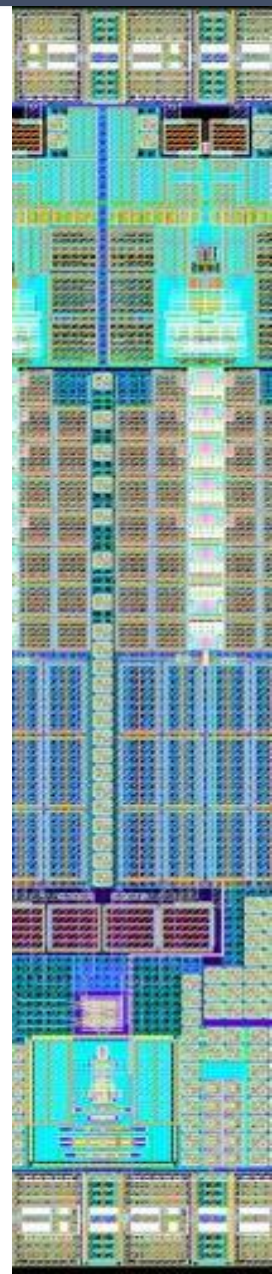
1981 : launching CMP with NMOS
1983 : development of NMOS / launching CMOS
1984 : development of CMOS
1987 : abandon NMOS / increase the frequency of CMOS runs
1990 : launching Bipolar / BiCMOS / MESFET GaAs / HEMT GaAs / advanced CMOS (0.5µm TLM)

1995 : launching CMOS / BiCMOS and GaAs compatible MEMS / DOEs / deep-submicron CMOS (0.25µm 6LM)
1998 : launching surface micromachined MEMS / abandon MESFET GaAs
1999 : launching SiGe / 0.18µm CMOS
2001 : 0.35µm HBT SiGe BiCMOS
2003 : 130nm CMOS
2003 : PolyMUMPS / MetalMUMPS / SOIMUMPS
2004 : 90nm CMOS
2005 : ASIMPS / SUMMIT / SANDIA

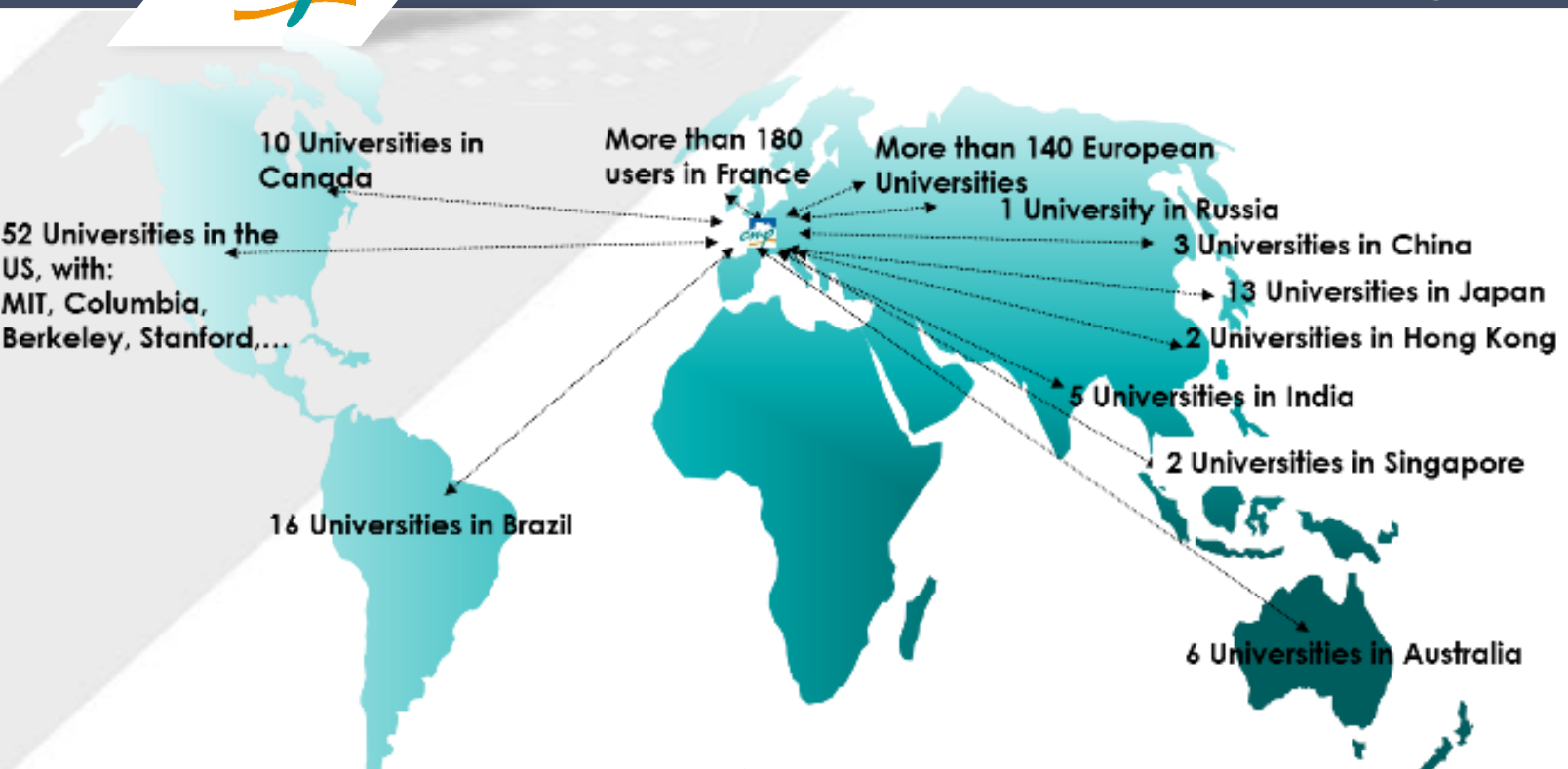
2006 : 65nm CMOS GP
2008 : 45nm CMOS / 65nm SOI
2009 : 40nm CMOS
2010 : 130nm 3D-IC / 20nm FDSOI
2011 : 28nm CMOS / 150nm GaAs pHEMT / 180nm CMOS CIS

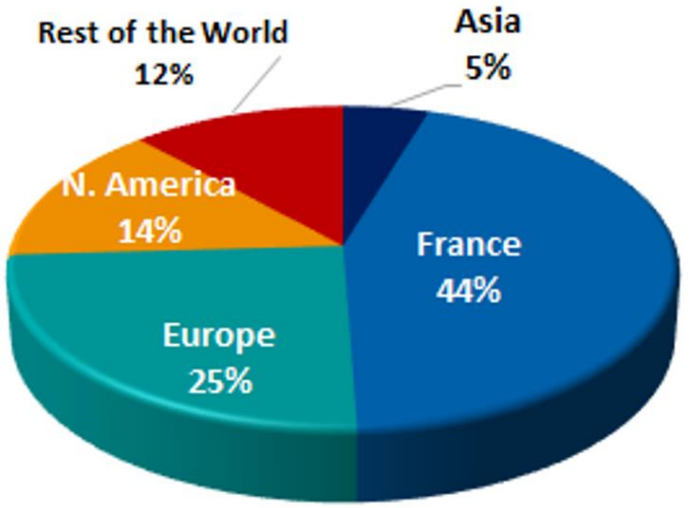
2012 : 28nm FD-SOI / 0.18µm CMOS/HV-CMOS
2013 : Analog 130nm H9A CMOS / THELMA MEMS
2014 : 30nm SOI FEM / Bulk micromachining / DALSA MEMS / PiezoMUMPS
2015 : 160nm BCD8sP / Micralyne MEMS / Open 3D CEA / 55nmBiCMOS
2016 : CEA Si-Photonics / active and passive interposers
2017 : 160nm BCD8s-SOI
2018 : EU Mirphab Pilotline / CEA MAD200 OxRAM NVM
2019 : ON Semi / AMF / EM
2020 : SMIC / TEEM Photonics





Worldwide service & partnership





Distribution of circuits per geographical area in 2020

Since 1981, over 614 customers from 71 countries have been served, more than 8100 projects have been prototyped through 1043 MPW runs and 74 different technologies have been interfaced.

CMP is partner in EUROPRACTICE

EUROPRACTICE IC SERVICE

Fraunhofer IIS · imec · UKRI Science and Technology Facilities Council · Tyndall National Institute Institiúid Náisiúnta

Photonics Portfolio at CMP

3 Processes :

- **Si-310 :** 300mm SOI substrate with 310 nm Si (SiN option)
- **Si-220 :** 300mm high uniformity SOI substrate with 220 nm Si (SiN option)
- **Si3N4-800 :** 800nm High Quality LPCVD Si3N4

AMF-SiP : Silicon-on-insulator, 220-nm top Si film, 2000-nm buried oxide (BOX)

3 Processes :

- **ioNext-NIR :** Glass Photonics for Near Infrared
- **ioNext-VIS :** Glass Photonics for Visible
- **WAFT :** Wave-guide Array to Fiber Transposers (standard device components)

CEA/LETI Photonic – Si-310 PHMP2M

Photonic – Si-310 PHMP2M

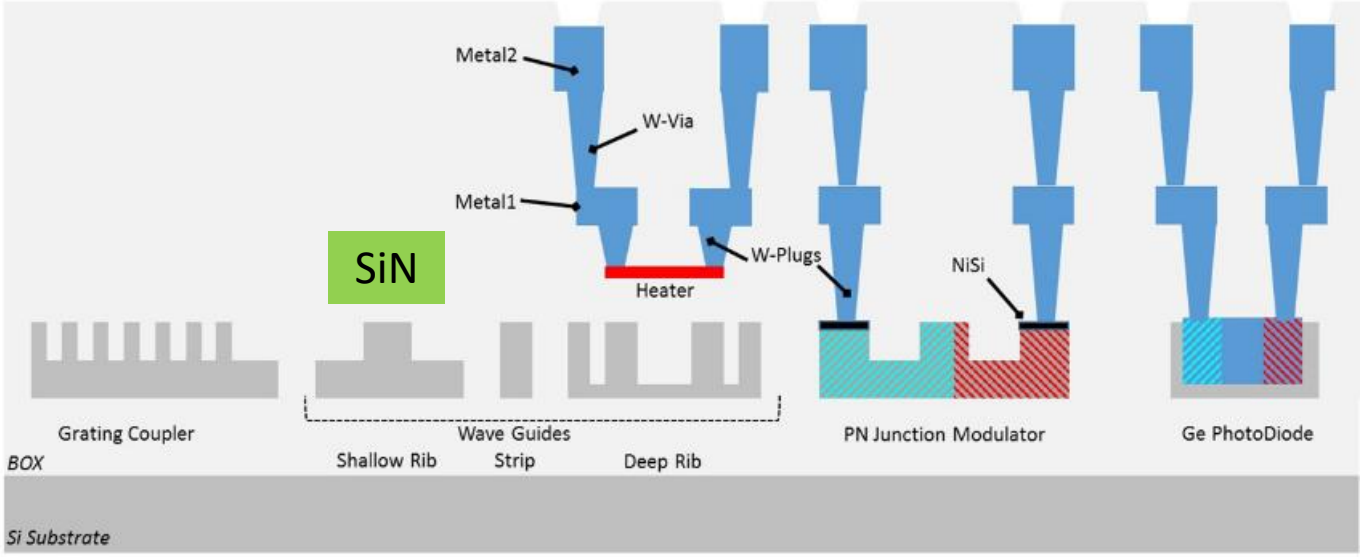
- 300mm CMOS SOI platform
- Silicon film 310nm and 2µm buried oxide
- Multilevel patterning allowing silicon heights of 0, 65, 165 and 300nm
- 2 metal layers (MET1 and Alucap)
- SiN layer

Passive components

- Fiber grating coupler 1D/2D
- Shallow/rib/strip waveguides and bends
- Ring filter
- Multimode interferometers

Active components

- Mach Zehnder modulator
- Ring racetrack modulator
- Ge photodiode
- TiTin metal heater



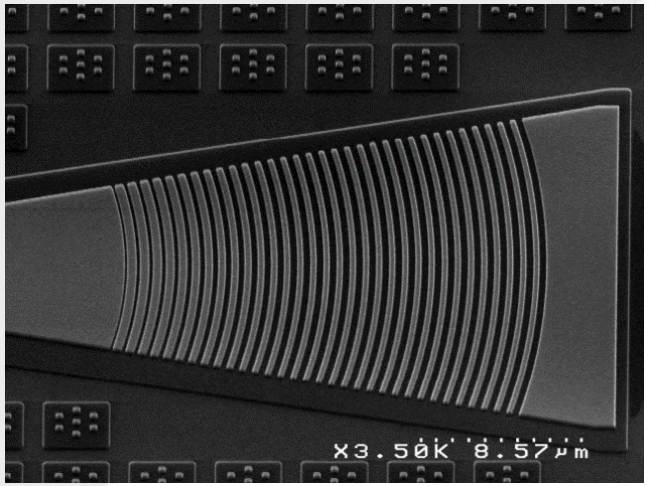
Si-310 PHMP2M Process cross-section

New Features :

- SiN option for 900nm wavelength applications
- Switch from a 200 to a **300mm** wafer platform

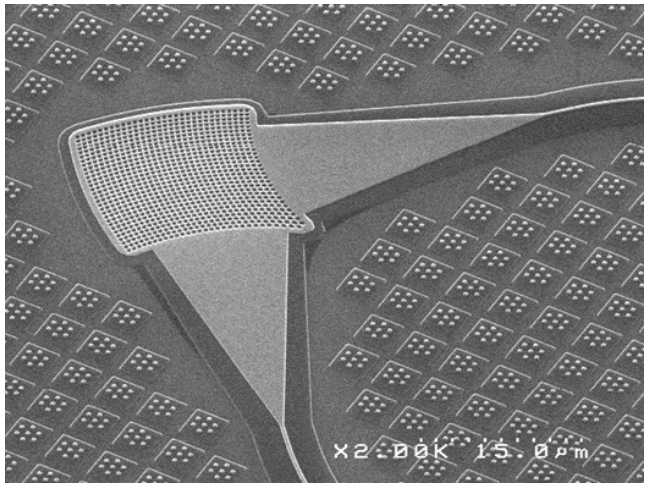
CEA/LETI Photonic – Si-310 PHMP2M

Realization examples



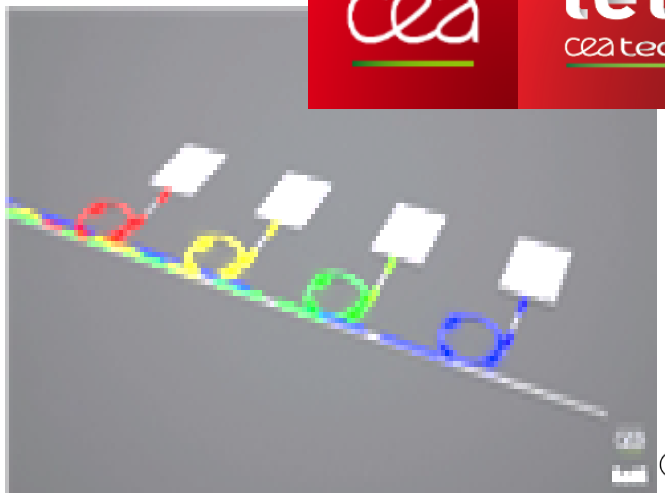
© CEA

1D fiber coupler

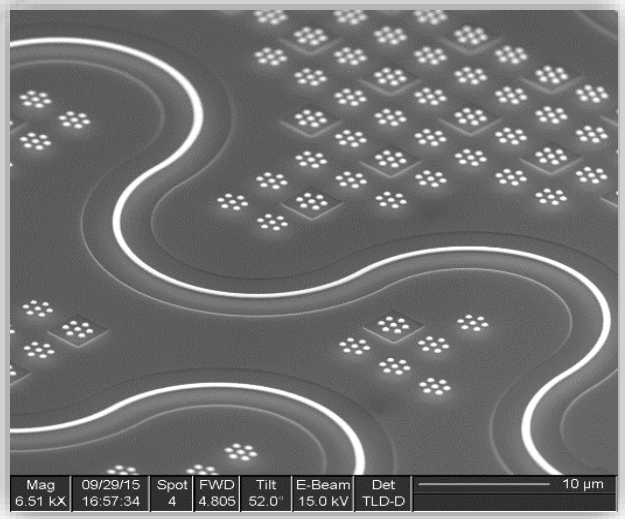


© CEA

2D fiber coupler

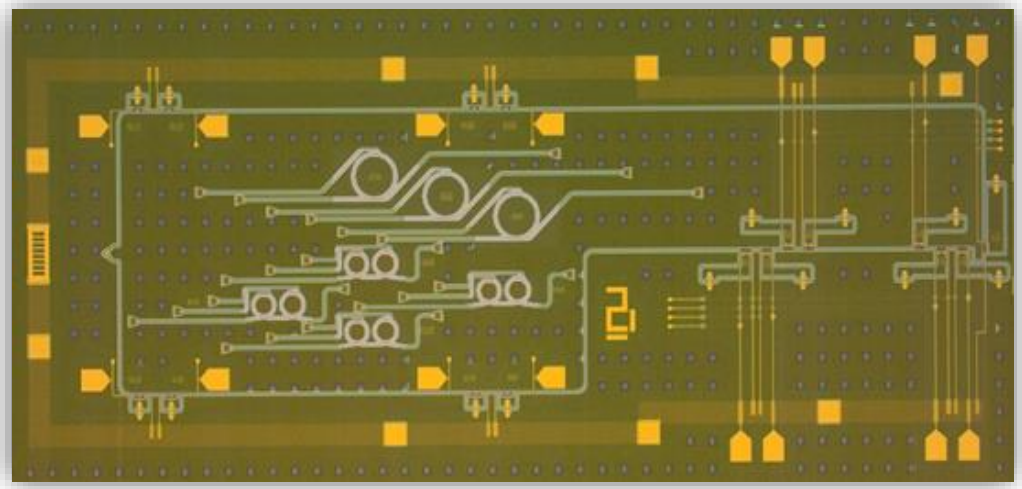

© CEA

Optical receptors

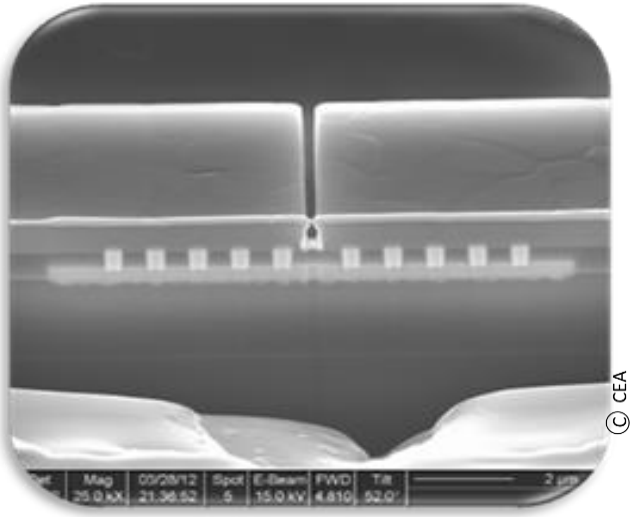


© CEA

Highly confined waveguides



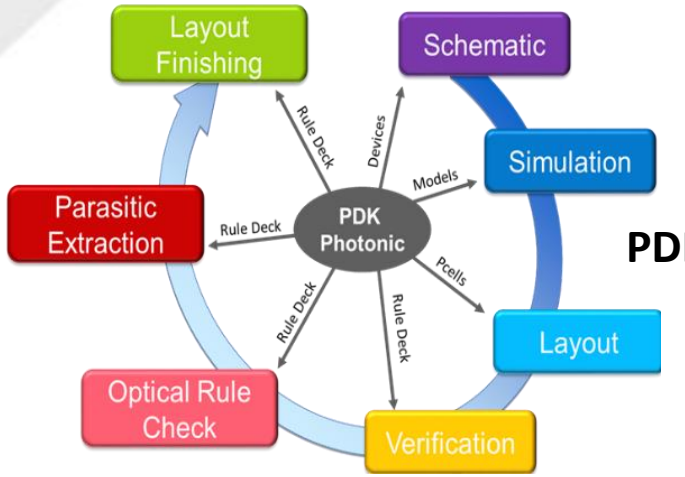
Optical transceiver circuit


© CEA

Ge PIN diode

CEA-LETI Si-photonics technology

- **Supported PDK :**
  - Cadence IC
  - Synopsys OptoDesigner
  - Mentor-Tanner L-Edit for the design
  - Mentor Eldo for simulation
  - Mentor Calibre for verification



PDK Design-Flow

- **MPW runs** : Minimum quantity of 25 prototypes

Prototyping Pricing

LETI-CEA – IRT Nanoelec [1]	STANDARD €/mm²
Silicon Photonics Si-220	760 [2]
Silicon Photonics Si-310	1600 [2]
Silicon Photonics Si-310 + SiN	1920 [2]
Silicon Nitride Photonics Si3N4-800	960 [2]

Notes:
[1] Area = X*Y including seal-ring.
[2] Minimum price is the charge for 10mm².

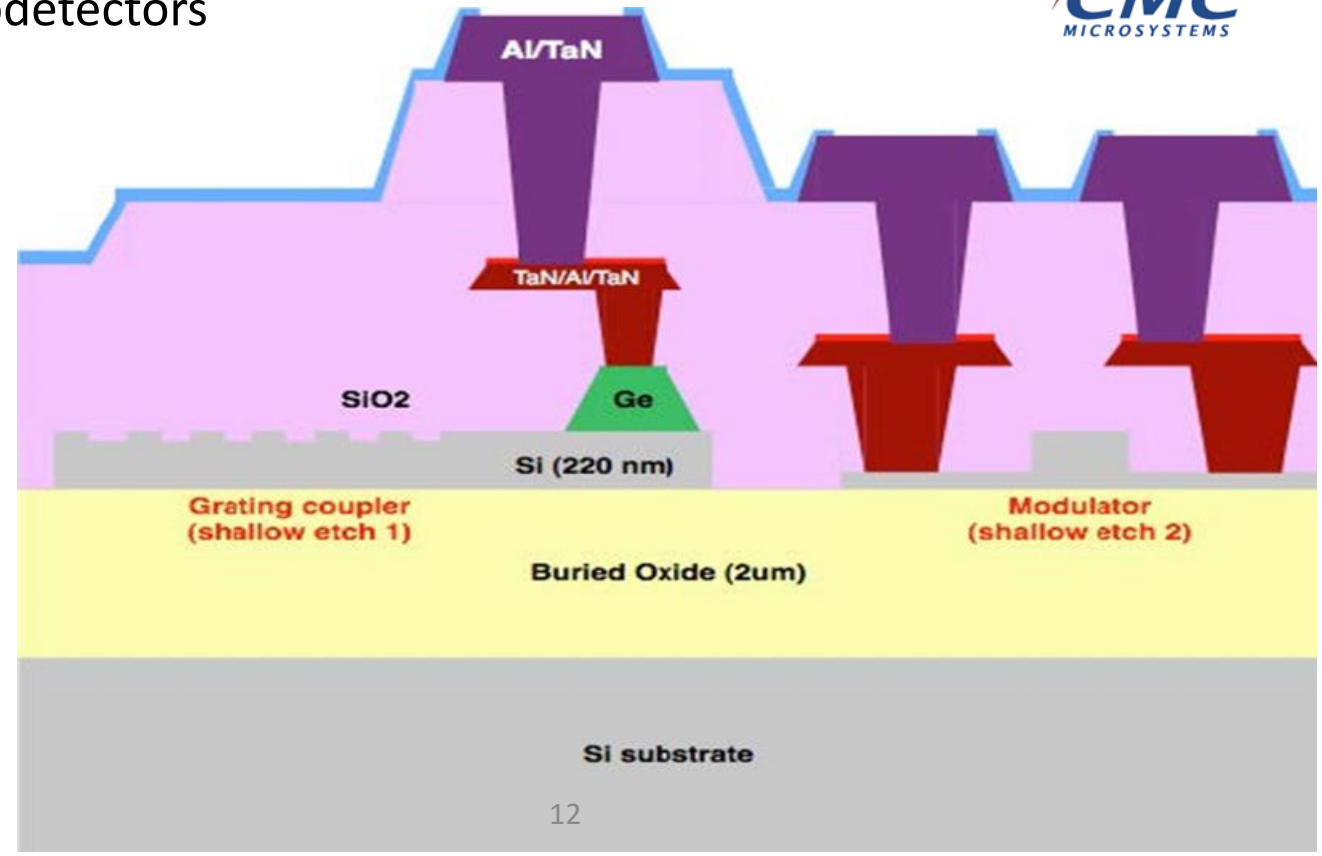
MPW run schedule

IRT Nanoelec/CEA-LETI	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Si-Photonics IC Si-220		15										1
Si-Photonics IC Si-310									6			
SiN-Photonics IC Si3N4-800				26								

AMF Silicon Photonics Platform

Process Features

- ❑ Silicon-on-insulator, 220nm top Si film, 2µm buried oxide (BOX)
- ❑ Two partial etches and one full etch of the top silicon
- ❑ 6 implants for optical modulators (P++, P+, P, N++, N+, N)
- ❑ Germanium deposition and implanting for photodetectors
- ❑ Two metal levels for routing
- ❑ Metal heaters
- ❑ Supports design and fabrication of :
  - modulators
  - detectors
  - waveguides (strip or ridge)
  - gratings for fiber coupling
  - multiplexers (diffraction or arrayed waveguide)
  - filters (resonators, Bragg gratings)
  - ring and disk resonators



AMF Si-photonics technology

- **Supported PDK :**
  - Mentor Graphics Pyxis
  - Tanner/Luceda L-Edit/IPKISS
  - Tanner L-Edit Photonics
  - Synopsys OptoDesigner

- **MPW runs** : Minimum quantity of 20 prototypes

Prototyping Pricing

AMF [1]	STANDARD €/block
Silicon Photonics	3mm x 4mm: 15600 3mm x 8mm: 20100 6mm x 8mm: 37900 3mm x 16mm: 37900

Notes:
[1] Area = X*Y including seal-ring.

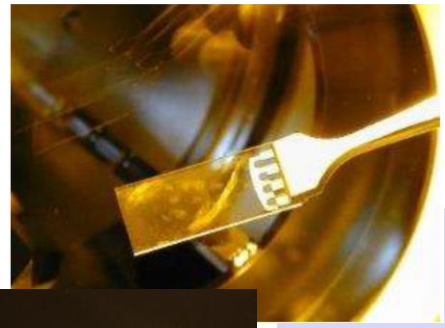
MPW run schedule

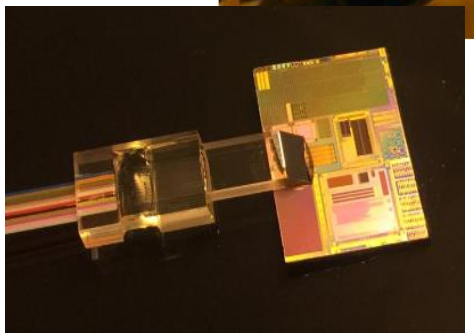
AMF	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Si-Photonics IC SiP			22							25		

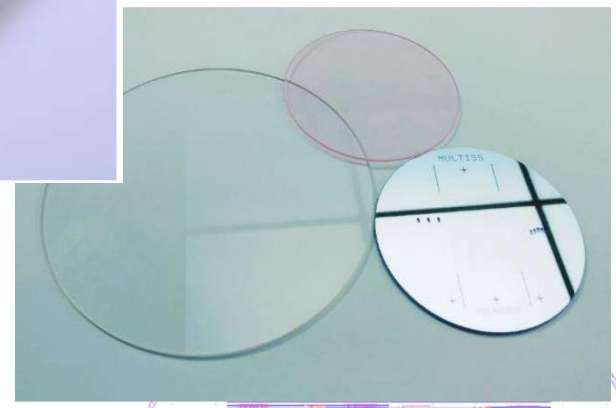
Teem Photonics Technology

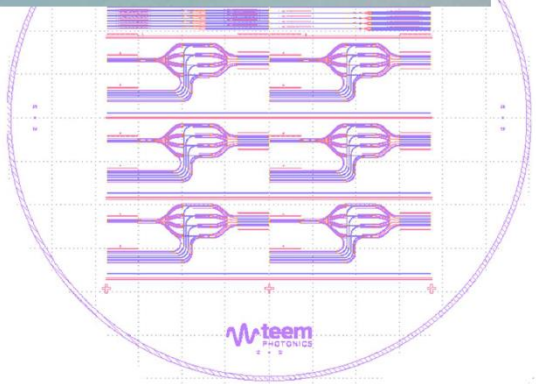
Glass Photonics Process Main features

- Based on a local exchange of doping ions to define gradient-index waveguides wafer-level
- Uses 60mm or 100mm diameter glass wafers
- Requires only one photolithography step

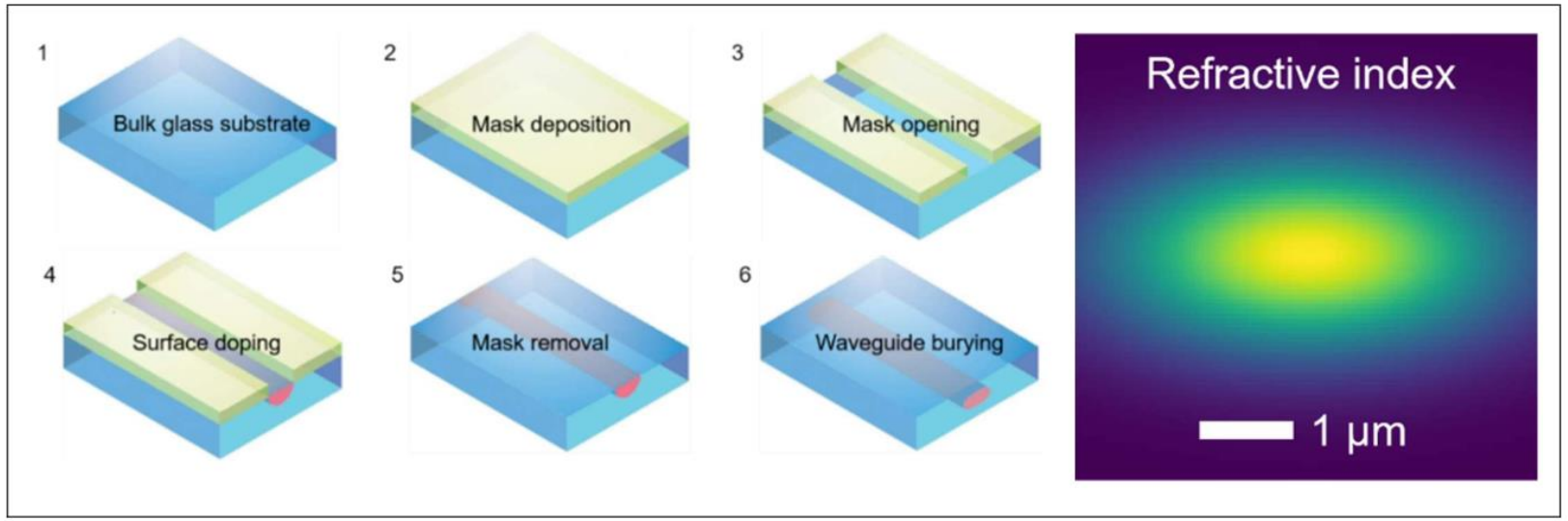








Process Flow



Teem Photonics Process Features

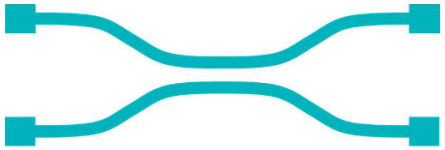
Operating range:
- Bandwidth from 1520 to 1570nm
- On-chip MFD (modal field diameter) of 4.2 x 3.2µm^2
- MFD converters at chip facet to match optical fibers' MFD.

Performance:
- Propagation loss of 0.15dB/cm at 1550nm
- Minimum radius of curvature of 800µm
- Low temperature dependence: 0,01nm/°C

Optical functions:
- I/O port
- Spot size converter
- Surface waveguide
- 50/50 splitter
- 50/50 directional coupler
- Waveguide crossing
- Mach-Zehnder interferometer
- Evanescent coupling

Straight waveguide
- Loss 0.15 dB/cm (O and C-band)
- n_{eff} 1.52 at 1550 nm
- MFD 4x3 µm at 1550 nm

S-bend and arc-bend
- radius 800 µm



Evanescent coupler
- 50/50 in C-band by default
- custom ratio on request
- custom spectral band on request
- very low extra-loss

Y-junction
- broadband (O and C-band)
- low extra-loss

1xN splitter
- up to N=512

Waveguide crossing
- low extra-loss
- no crosstalk

Spot size converter
- on PIC facet
- 10 µm to 4x3 µm MFD conversion
- low loss

MUX and DEMUX
- AWG
- Broadband evanescent coupler

Teem Photonics technology

Offering terms :

- 3 runs scheduled per year
- Rate per wafer or half-wafer
- Maximum of 30 dies per wafer
- Leadtime : 1 month
- Supported PDK software : NAZCA (free & open-source)
- WAFT standard devices on request

Prototyping Pricing

TEEM Photonics	STANDARD €/wafer	STANDARD €/ half-wafer
Glass-photonics IC ioNext-VIS	9100	4800
Glass-photonics IC ioNext-NIR	9100	4800
Glass-photonics IC WAFT	Contact CMP	Contact CMP

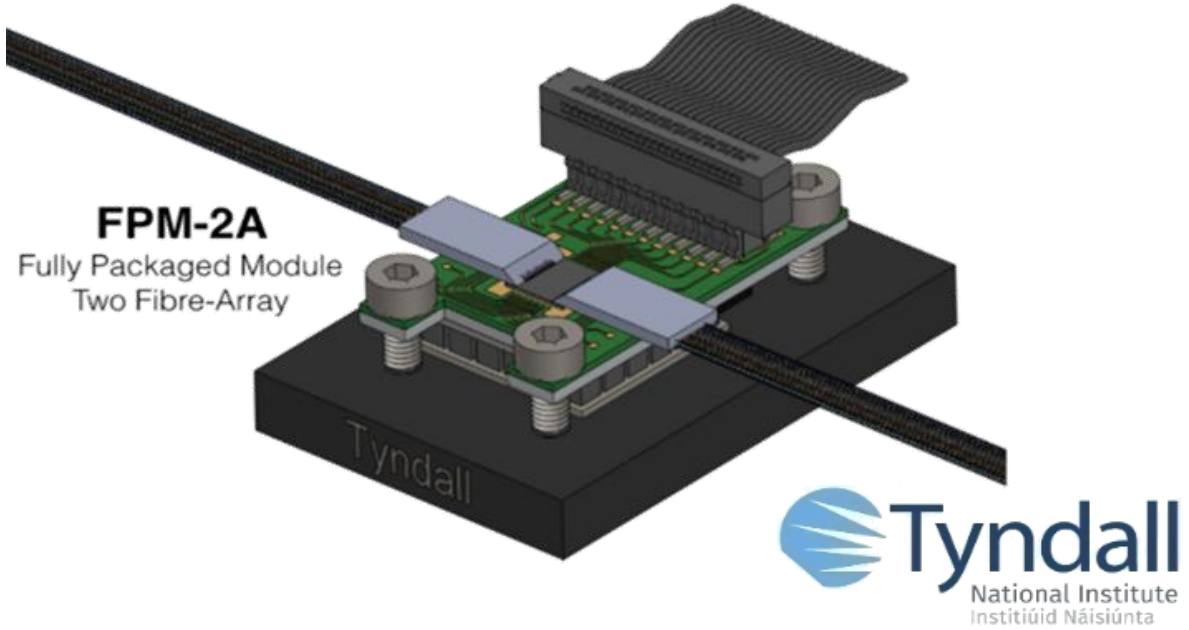
MPW run schedule

Teem Photonics	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Glass-photonics IC ioNext-NIR			22			21				25		
Glass-photonics IC ioNext-VIS			22			21				25		

Photonics Packaging / System Integration

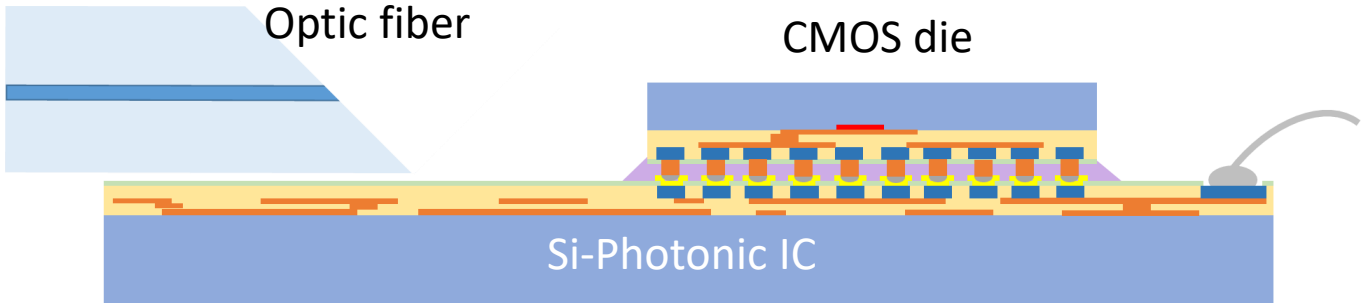
Partnership with Tyndall

- Fiber array alignment up to 128 channels
- Grating coupler (2D on the circuit face)
- Edge coupler (or the edge of the chip)
- 10 DC wire-bond connections
- Thermal management
- Fully Packaged Standard Modules



2.5D System Integration

- Si-photonics die as Interposer
- Face-to-Face flip-chip of CMOS die
- Optic fiber coupling
- Wire bonding for primary IOs



https://mycmp.fr

cmp@mycmp.fr

Horizon 2020
European Union funding
for Research & Innovation