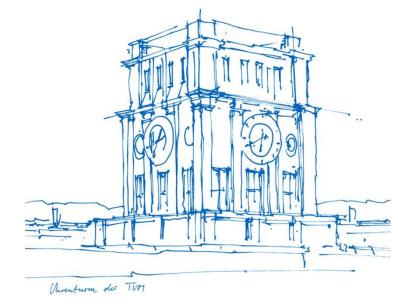


Efficiency-Oriented Design Automation for Wavelength-Routed Optical Network-on-Chip (WRONoC)

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- Need of efficient WRONoC design
- Efficiency-oriented WRONoC design automation
 - Design step separation: topology generation followed by physical design
 - Comprehensive template-based synthesis
 - Subtraction from fully-connected router
- Conclusion

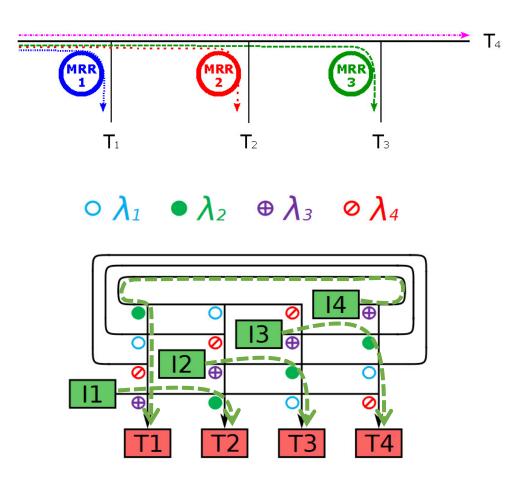


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WRONoC Working Mechanism

- Usage of microring resonators (MRRs) for multiplexing and demultiplexing
- Dedicated signal path determined in design phase for each tuple (initiator, target, wavelength)
- No path overlap between signals with the same wavelength → enable all-to-all simultaneous communications





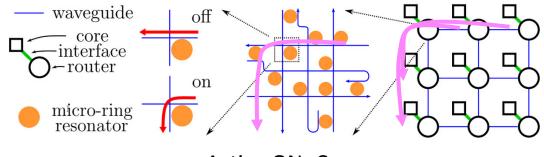
Passive WRONoC vs Active ONoCs

Advantages:

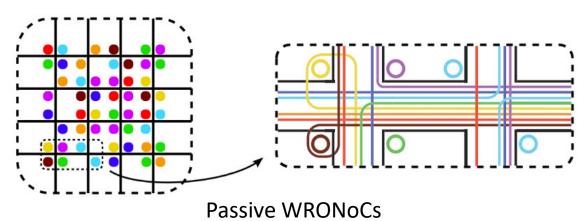
- No control resource
- No scheduling effort
- No congestion control
- No signal path construction → no uncertain signal delay

Disadvantages:

Extensive usage of MRRs (1 MRR serves constant #paths) →
Scalability issue! → suitable for application-specific usage → design optimization to save resources



Active ONoCs



WRONoC Design Features

Topological features:

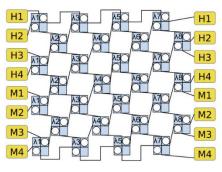
- Waveguide connection structure
- MRR topological locations
- MRR resonant wavelengths
- Signal wavelength assignment
- Signal path routing

Physical design features:

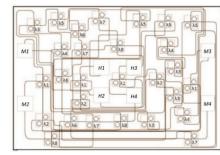
- Waveguide routing
- MRR placement

source: Engineering a Bandwidth-Scalable Optical Layer for a 3D Multi-core Processor with Awareness of Layout Constraints, NOCS'12, Luca Ramini, Davide

Bertozzi and Luca P. Carloni.



Manual topology



Manual layout

- All these need to be done during the design phase
- Application-specific optimization

- → Challenges of efficiency!
- & Beyond human capability!



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Design Step Separation

- Topology generation and then physical design – conventional and intuitive
- Advantages:
 - Intermediate solution, i.e. topology, is observable
 - Fast
- Disadvantages:
 - Mismatch of node positions → long waveguide detours and many waveguide crossings

H3 M3

Automatically-synthesized topology

Automatically-synthesized layout

M2

H2

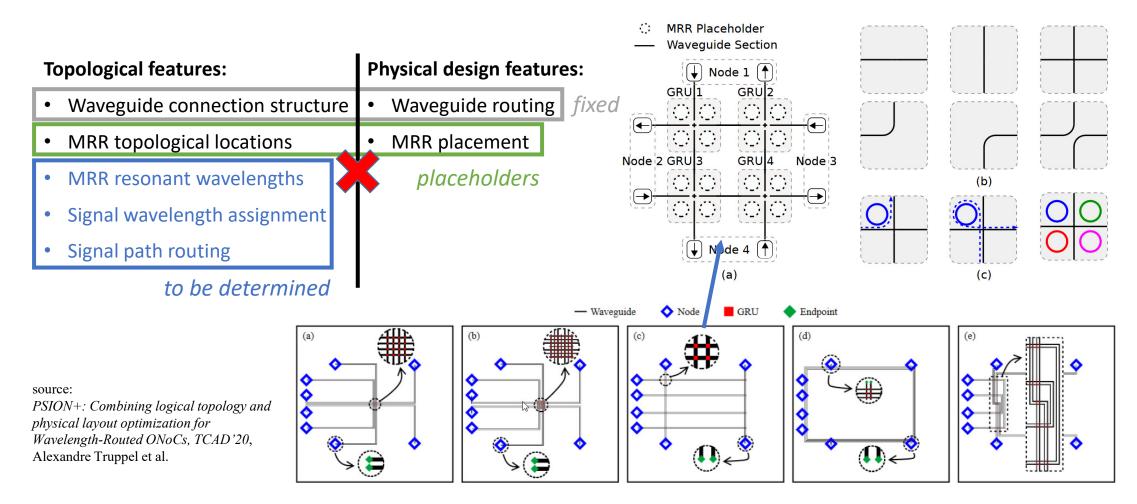
M4



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Comprehensive Template-Based Synthesis



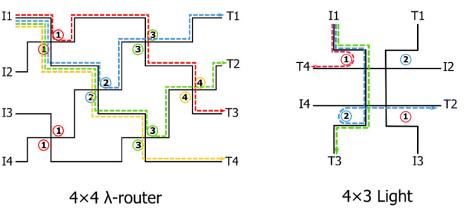


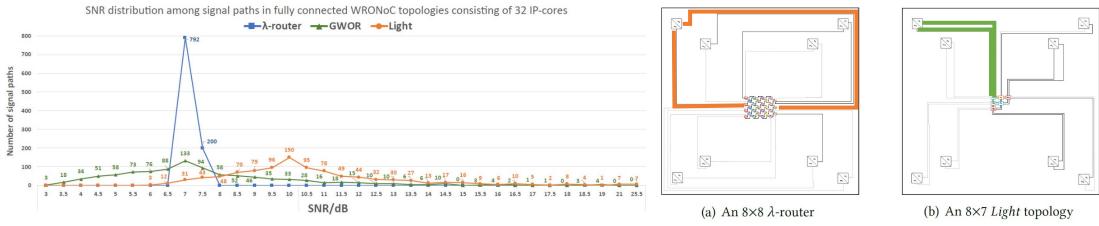
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Subtraction from Fully-Connected Router

- Optimization by signal path binding
- **Key** requirements:
 - Physical-design aware and friendly
 - Wide range of SNR distribution





source: Light: A Scalable and Efficient Wavelength-Routed Optical Networks-On-Chip Topology, ASP-DAC'21, Zhidan Zheng et al.



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Conclusion

- Optimization of application-specific WRONoC is worthwhile but difficult
- Being efficient is the prerequisite of WRONoC design automation tools
- The following methodologies are worth further exploration for efficient WRONoC design automation:
 - Design step separation: topology generation followed by physical design
 - Comprehensive template-based synthesis
 - Subtraction from fully-connected router
- Staying efficient will be more challenging considering the following aspects:
 - More design features, e.g. power distribution network
 - More optimization metrics, e.g., crosstalk and bandwidth

Many thanks to my colleagues: Mengchu Li, Alexandre Truppel, Zhidan Zheng, and Prof. Ulf Schlichtmann And Special thanks to our collaborator Prof. Davide Bertozzi

