100 GBAUD TRANSCEIVER CIRCUITS FOR OPTICAL INTERCONNECTS

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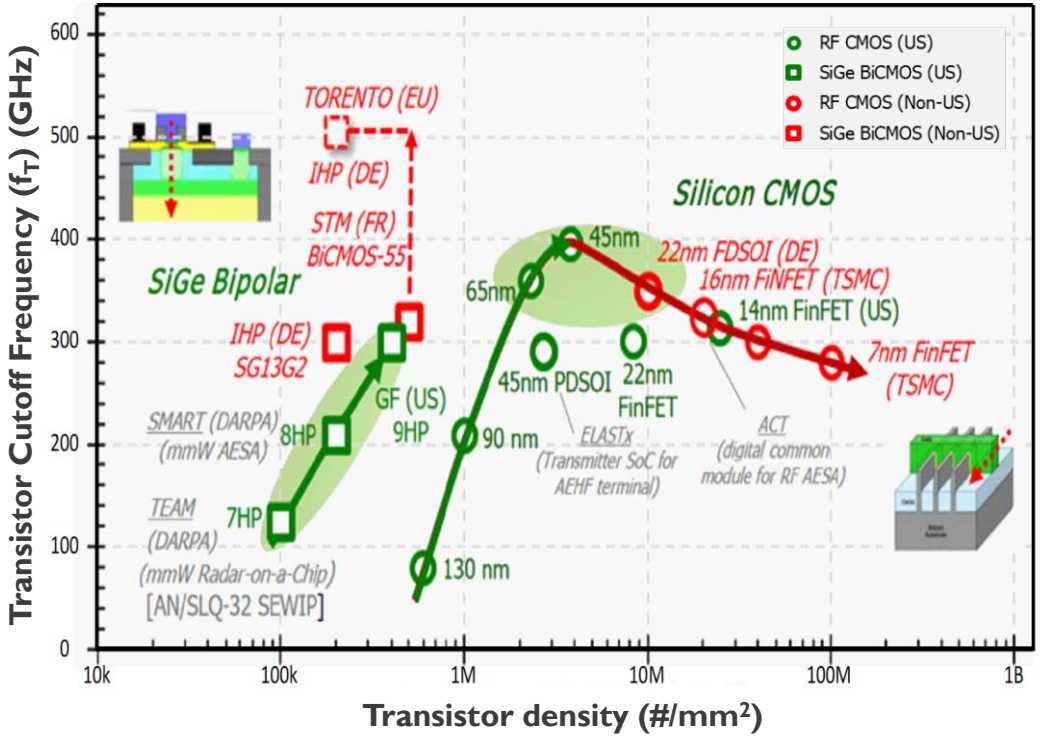
OUTLINE

- CMOS vs. SiGe BiCMOS
- Recent and ongoing work for 112 Gbaud in SiGe BiCMOS
  - Analog interleaver and MUX with integrated FFE
  - Quad MUX with EML driver and clock synthesis
  - Quad MZM driver and TIA
- Recently started in FinFET CMOS
  - Feasibility studies and proof-of-concept designs
  - 112 Gbaud DSP-based CDR and 150 GSa/s DAC
- Closing remarks
  - What comes next?
  - Acknowledgements

CMOS VS. SIGE BICMOS

Transceiver progress comes from **technology evolutions** and **smarter IC design**



Young-Kai Chen, DARPA Technologies for Mixed-mode Ultra Scaled Integrated Circuits Program, US Microsystems Technology Office, 2019

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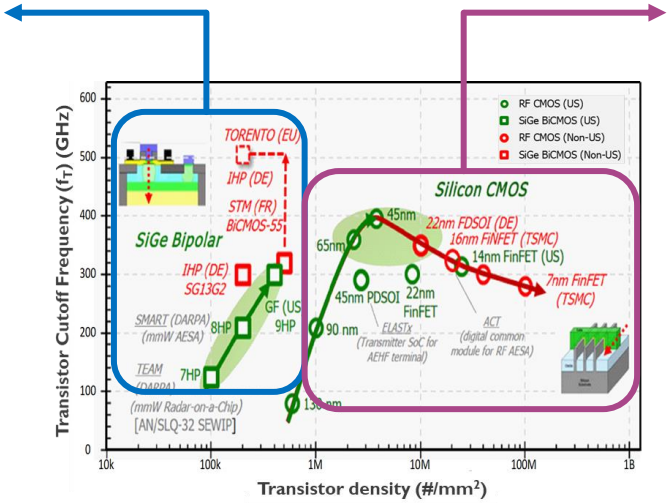
CMOS VS. SIGE BICMOS

HIGH-SPEED ANALOG / MIXED-SIGNAL DESIGNER'S PERSPECTIVE

SiGe BiCMOS

- Higher, still increasing ft/fmax
- Higher break down voltage
- Higher current
- Higher transconductance and intrinsic gain
- Lower noise
- Good metal stacks for high-Q passives and interconnects
- More intuitive/traditional design
- CMOS (55nm, 90nm,…) limits mixed-signal and DSP capabilities



CMOS

- Huge transistor density
- 1000s layout rules, increasing design time
- Sweetspot for analog ~ 28 nm
- Analog performance degrades, low supply voltage
- Higher device variability
- Digital performance increases: DSP, calibration & predistortion
- Economics: if it can be done in CMOS, it will be done in CMOS
- Enormous investments on next generation CMOS processes
- High product volume needed

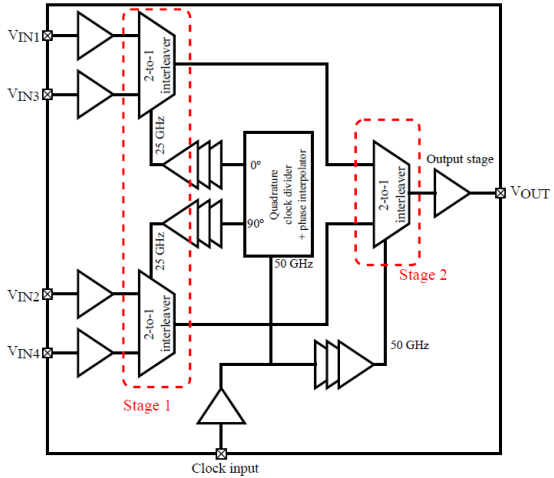
T. Zimmer, et al, "SiGe HBTs and BiCMOS Technology for Present and Future Millimeter-Wave Systems", IEEE Journal of Microwaves, 2021

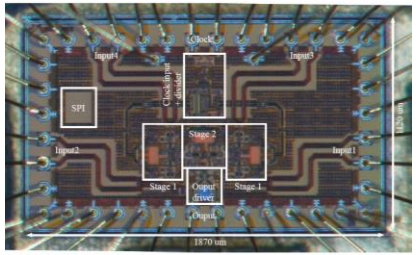
Young-Kai Chen, DARPA Technologies for Mixed-mode Ultra Scaled Integrated Circuits Program, US Microsystems Technology Office, 2019

100-120 GBAUD DESIGNS IN SIGE BICMOS

100GBAUD SIGE BICMOS ANALOG INTERLEAVER
OVERCOMES CMOS DAC BANDWIDTH LIMITATION

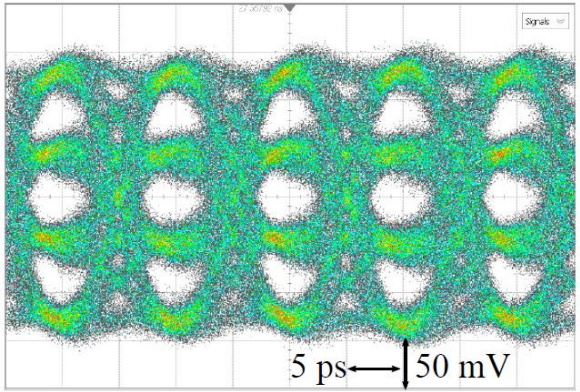
- Functionality: interleave outputs from sub-rate DAC's into broadband analog output
- Novel architecture (patent pending) based on explicit return-to-zero generation
  - Simultaneous programmable **equalization** at high-speed output
  - Lower **clock feedthrough**





	TYP	UNIT
SAMPLING RATE	100	GS/s
ANALOG BANDWIDTH	73	GHz
POWER CONSUMPTION	700	mW

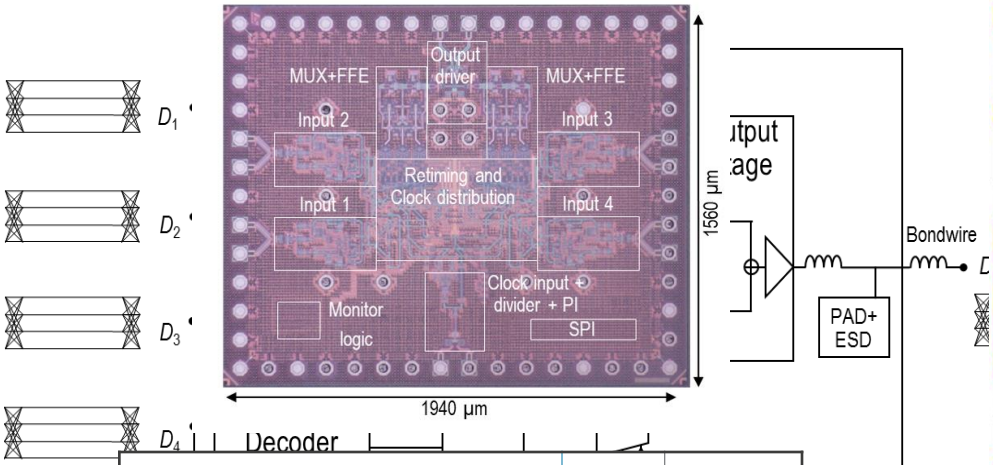
100GBd PAM-4 (equalizer ON)



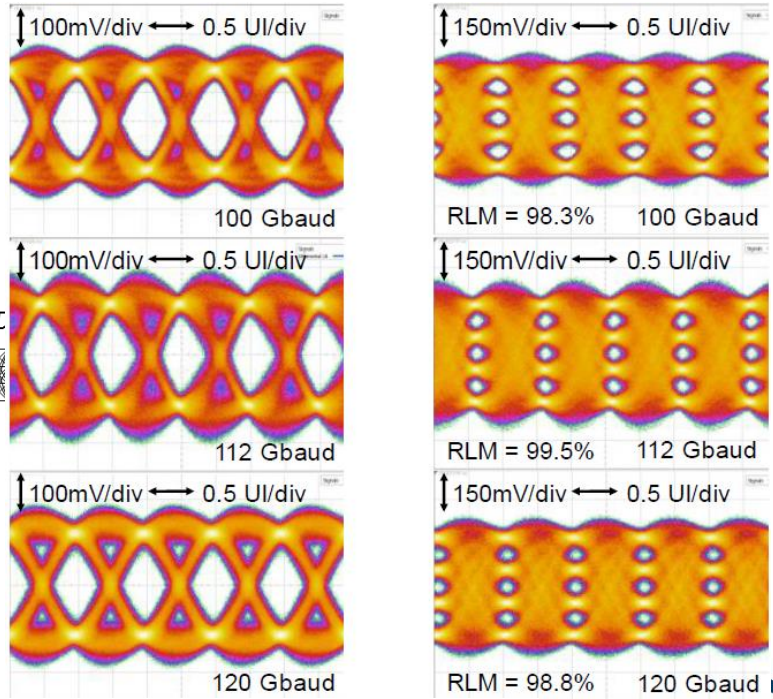
H. Ramon, et.al., “A 700mW 4-to-1 SiGe BiCMOS 100GS/s analog time-interleaver”, ISSCC, Feb. 2020.
H. Ramon, et al,,"A 100 GS/s Four-to-One Analog Time Interleaver in 55 nm SiGe BiCMOS", JSSC, Aug. 2021.

120GBAUD SIGE BICMOS MUX AND EQUALIZER

- 4:1 “digital” MUX, input decoders for NRZ and PAM-4
- 2 independent **compact** 7-tap FFE (LSB & MSB)



	TYP	Unit
Diff output swing (8dB loss at 60 GHz)	0.5	V_{pp}
Analog bandwidth	>80	GHz
Power consumption	2200	mW

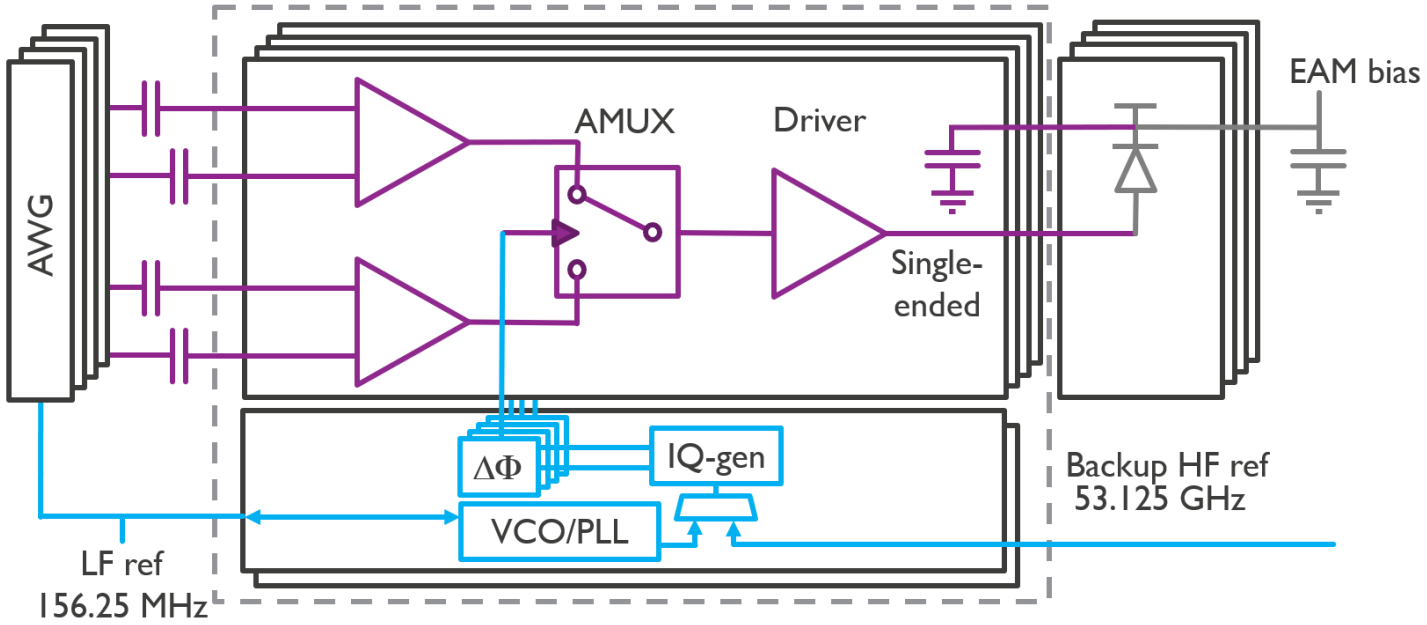


M. Verplaetse, et al, “A 4-to-1 240 Gb/s PAM-4 MUX with a 7-tap mixed-signal FFE in 55nm BiCMOS”, CICC, Apr. 2021

120GBAUD SIGE BICMOS ONGOING DESIGNS

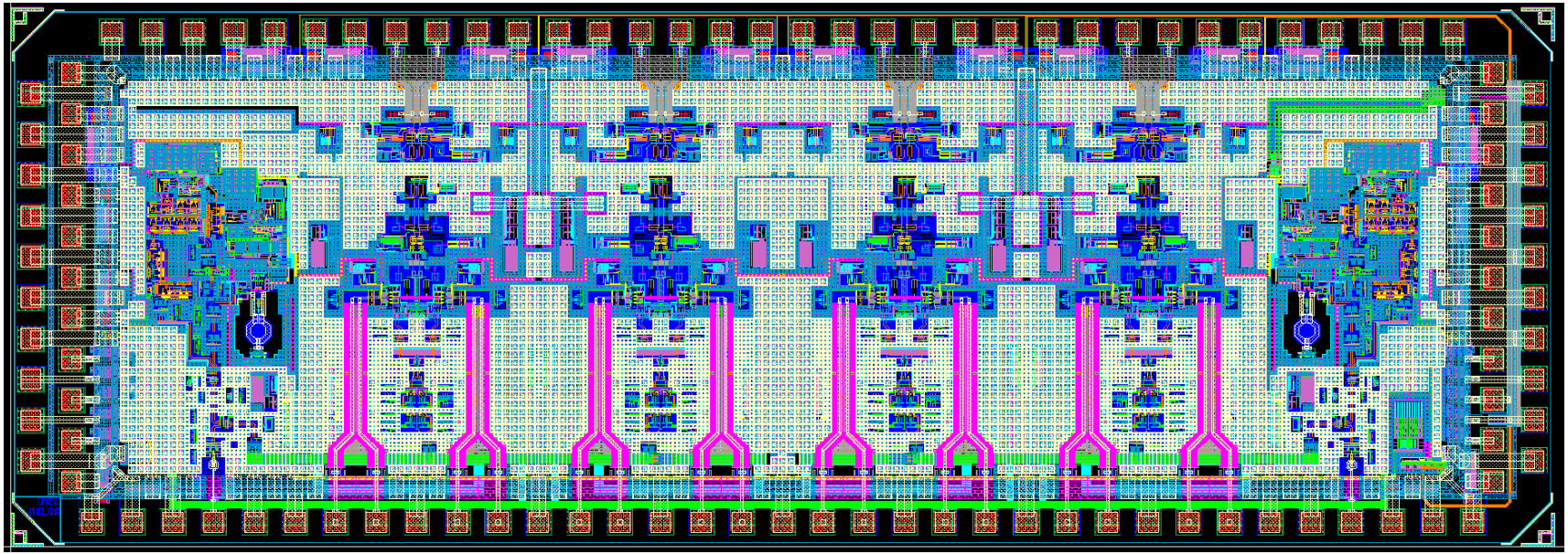
H2020 POETICS

- Quad 2:1 linear MUX with integrated EML driver and integrated PLL/VCO



120GBAUD SIGE BICMOS ONGOING DESIGNS

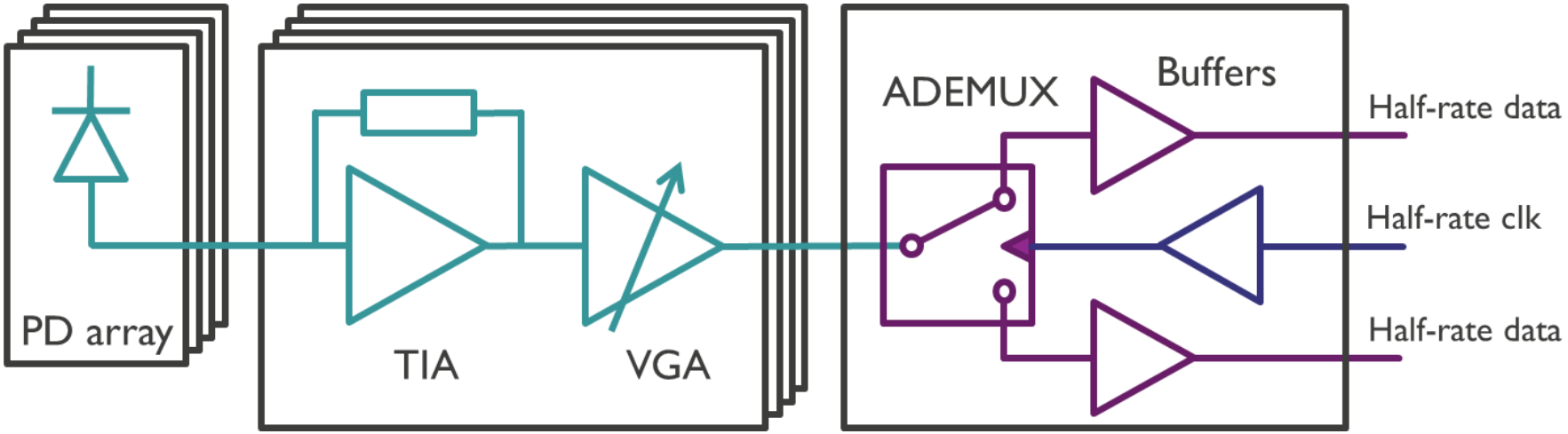
H2020 POETICS



120GBAUD SIGE BICMOS ONGOING DESIGNS

H2020 POETICS

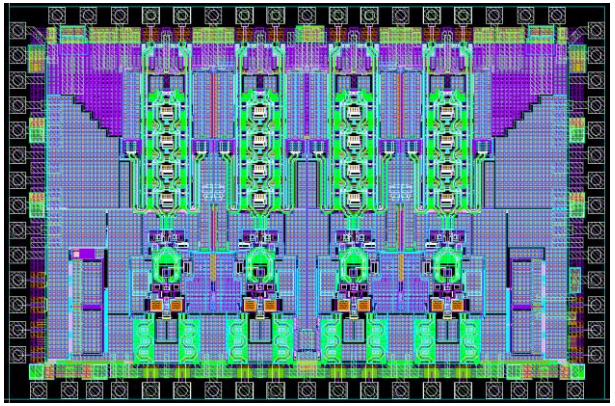
- Quad TIA and DEMUX

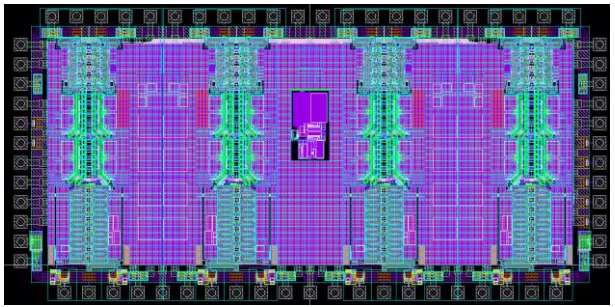


120GBAUD SIGE BICMOS ONGOING FABRICATION

H2020 PLASMONIAC AND H2020 NEBULA

- 4-channel linear Mach-Zehnder modulator driver array
  - 55nm SiGe BiCMOS
  - ~90GHz bandwidth, ~2.0…2.5Vpp differential swing
  - Status: just delivered, assembly ongoing
  - Co-designed with a Silicon Photonic DP-IQ modulator
- 4-channel linear transimpedance amplifier array
  - 55nm SiGe BiCMOS
  - ~50-60GHz bandwidth, low THD
  - OMA sensitivity ~ -6dBm
  - Status: just delivered, assembly ongoing
  - Suitable for single and balanced PDs

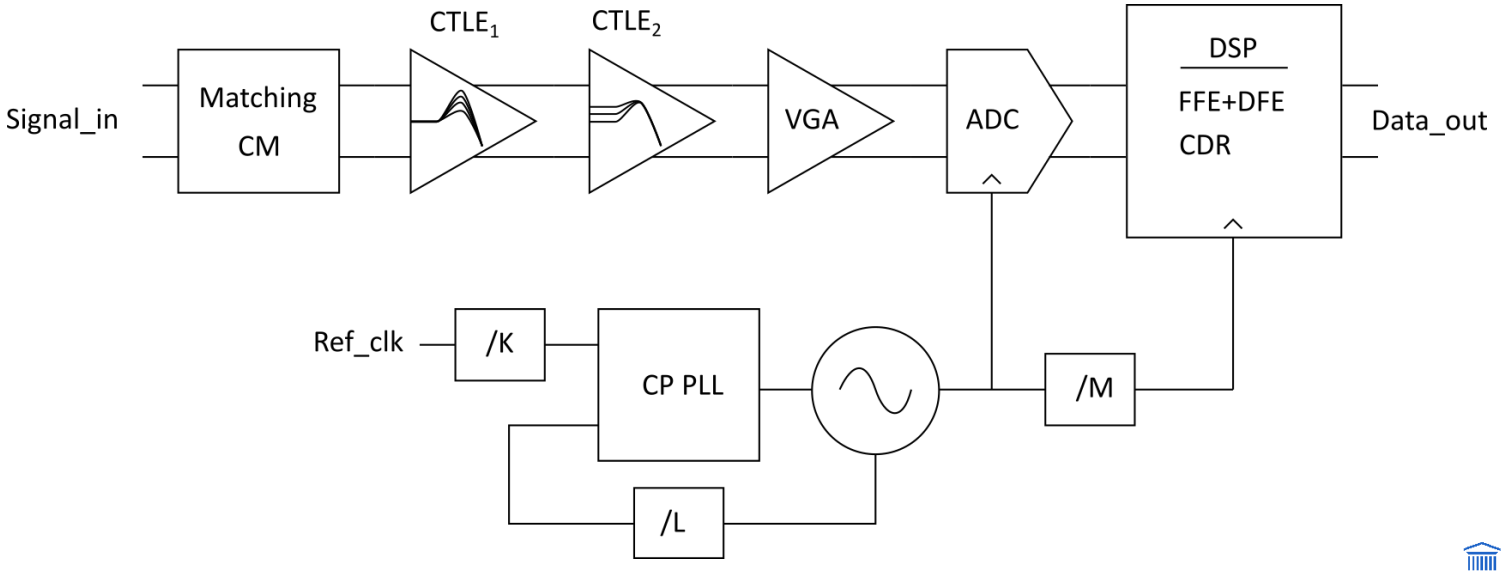




ONGOING WORK IN CMOS

112 GBAUD DSP-BASED CDR IN FINFET CMOS

- Low-phase noise clock generated by PLL
- FFE, DFE and CDR function in DSP
- ADC developed by imec Leuven



CLOSING REMARKS
AND ACKNOWLEDGEMENTS

WHAT COMES NEXT? WILL 200 GBAUD BE FEASIBLE?

VERY EXCITING DECADE AHEAD

- Technology, circuit design and co-integration will **progress** in the coming years
  - Several other applications push in same direction: 6G, radar, medical…
  - Novel transistor concepts, integration of high-mobility semiconductor materials
  - Hybrid integration through advanced packaging e.g. transfer printing (H2020 Caladan)
  - Evolution of circuit architecture and design tools
  - New TRx concepts combining electronic and photonic ICs: electro-optical DACs, optical equalization, optical time division multiplexing…
- However, the R&D is a **huge challenge**
  - An increasing list of issues/risks to be tackled
  - Power consumption is certainly a concern
  - Advanced technology access is restricted
  - IC design cost is really high

WHAT COMES NEXT? WILL 200 GBAUD BE FEASIBLE?

SOME PARTICULAR DESIGN ASPECTS FOR SIGNAL GENERATION

- Clock generation and distribution ~ 30-40 % of the power consumption
  - Lower jitter and phase noise required with increasing baud-rate / constellation e.g. < 100 fs rms
  - Jitter-Power trade-offs in PLLs
  - Multiple sub-rate clocks with precise phase relationship
  - Clock tree to provide high swing clocks wherever needed
- Noise coupling from DSP to VCO or sensitive Rx
- Bandwidth limitations
  - Sinusoidal clocks have limited rise/fall time
  - Loading on current summing nodes
  - ESD protection
  - Simulated waveforms need postprocessing e.g. TDECQ
  - …

B. Razavi, "Jitter-Power Trade-Offs in PLLs", IEEE TCAS-I, 2021

GRATEFUL ACKNOWLEDGEMENT

TO THE TEAMS AND FUNDING BEHIND THIS WORK

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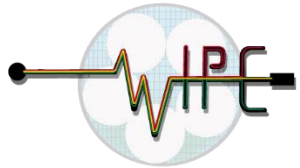
- Industrial and academic collaborators
- EU funding H2020 and ESA
- UGent IOF and BOF
- VLAIO – FWO
- Imec



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