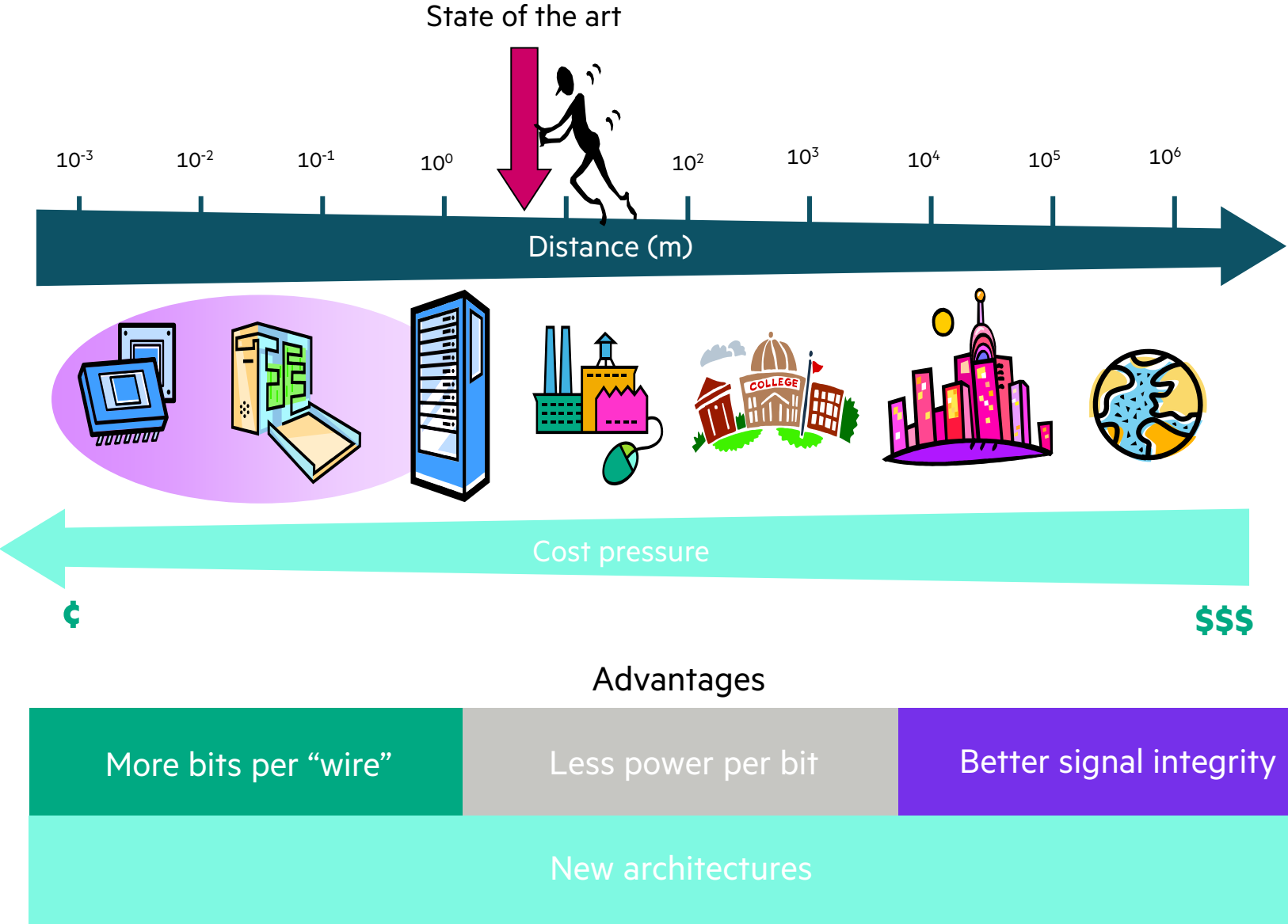# SILICON PHOTONICS FOR HPC: DEVICES AND TOOLS

Marco Fiorentino
Large Scale Integrated Photonics Lab, Hewlett Packard Enterprise

April 14th, 2022

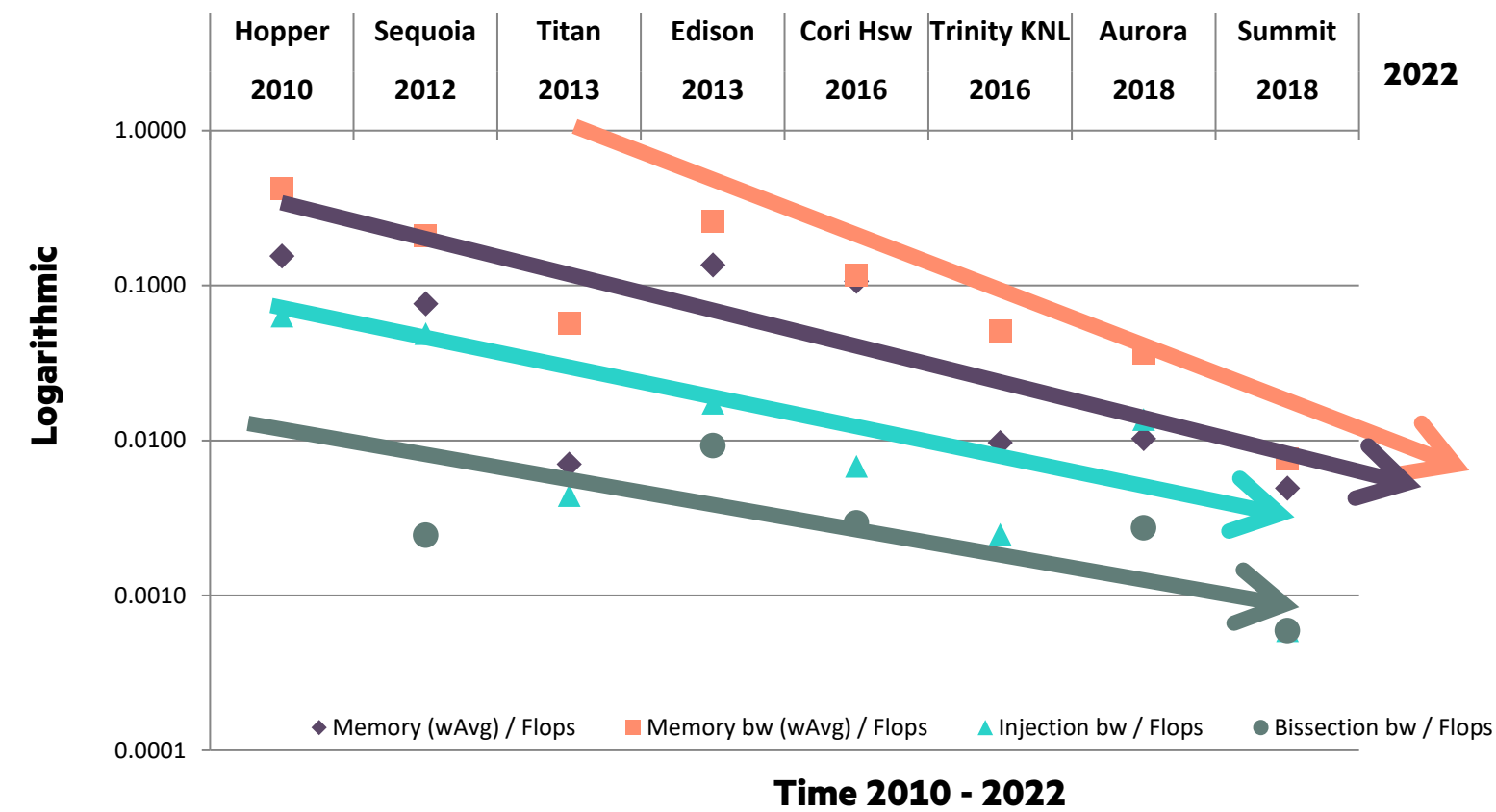# OPTICAL INTERCONNECTS

State of the art

10^{-3} 10^{-2} 10^{-1} 10^{0} 10^{2} 10^{3} 10^{4} 10^{5} 10^{6}

Distance (m)

Cost pressure

¢

$$$

Advantages

More bits per "wire"	Less power per bit	Better signal integrity

New architectures

SUPERCOMPUTER SYSTEMS TRENDS

Historical trends for key performance metrics

Hopper 2010	Sequoia 2012	Titan 2013	Edison 2013	Cori Hsw 2016	Trinity KNL 2016	Aurora 2018	Summit 2018	2022

Legend:
- ◆ Memory (wAvg) / Flops
- ■ Memory bw (wAvg) / Flops
- ▲ Injection bw / Flops
- ● Bissection bw / Flops

Y-axis: Logarithmic (1.0000, 0.1000, 0.0100, 0.0010, 0.0001)

X-axis: Time 2010 - 2022

Balanced system architecture

Memory-driven programming model

Energy efficiency from chip to cooling tower

Open architecture, open ecosystem

**..our ability to "service" the FLOPs is degrading**

ECOSYSTEM REQUIREMENTS

- Current SiPh players own all the IP
  - "Vertical" model
  - Inefficient
  - High entry barrier
- "Horizontal" model
  - Licensable IP, off-the-shelf parts
  - Comprehensive catalog of tools, parts, and services
  - Quick time to market
- Targeted for high-volume
  - CPU, GPU, switch manufacturers
 - System integrators
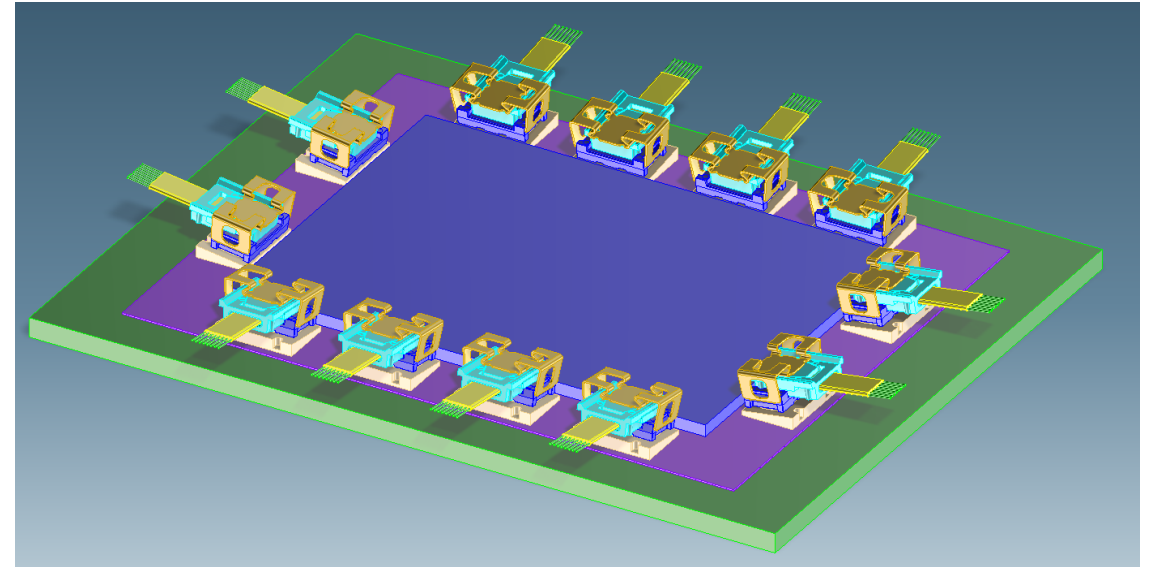
A SILICON PHOTONICS ECOSYSTEM

How do we increase market penetration of SiPh?
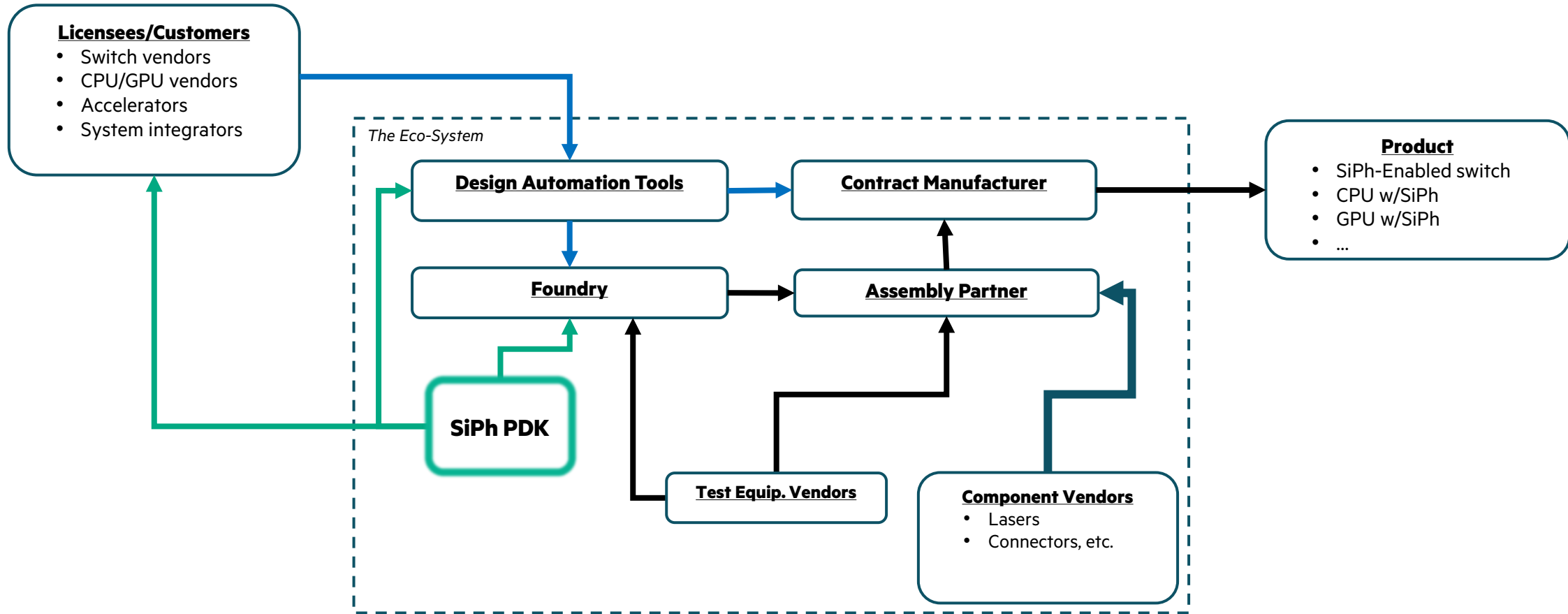
Fiorentino et al. "**An open Silicon Photonics ecosystem for computercom applications**" in Silicon Photonics IV, D. Lockwood and L. Pavesi eds.

DESIGN TOOLS

- Separate design cycles
- Device design tools
  - Required for photonics engineers
  - Python-based p-cells
  - Create symbols and models for system designers
- System design tools
  - Facilitate use for non-experts
  - Automated place and route
 - Integrated simulations
  - LVS
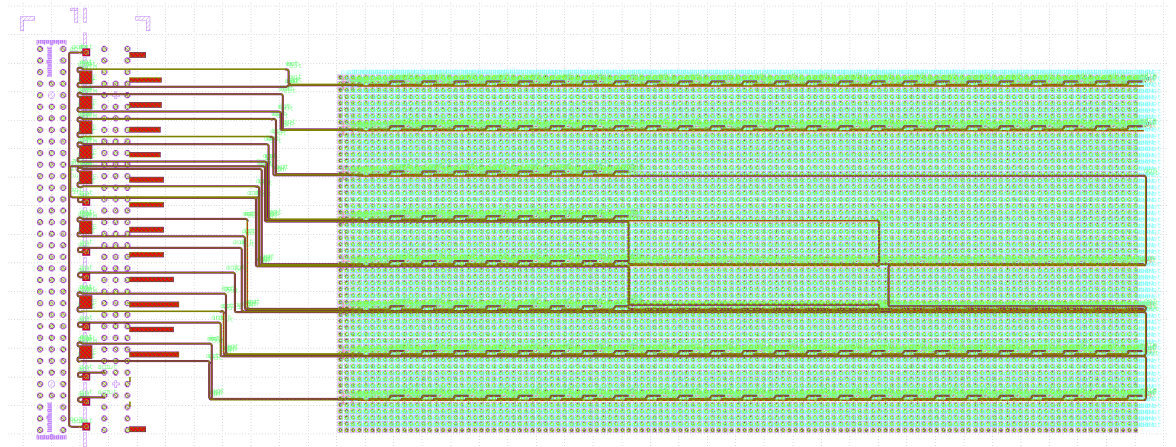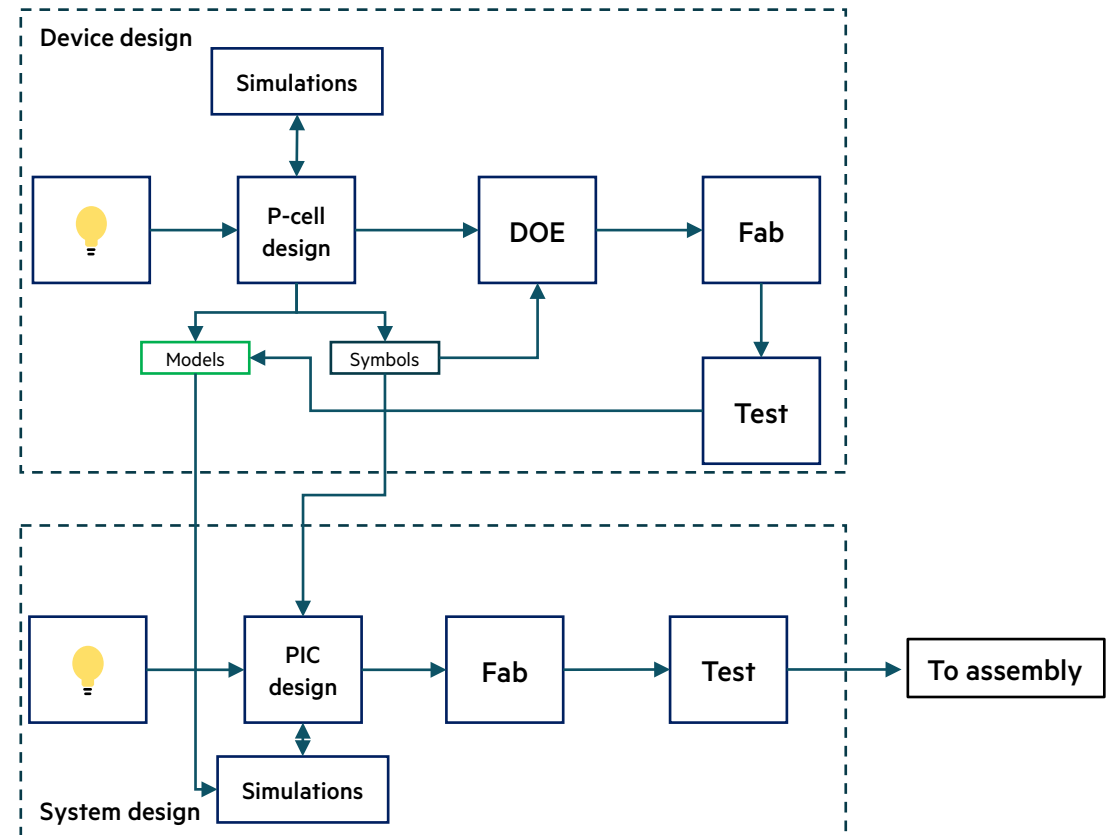
DEVICES

- Initial offering
  - Short- and long-reach WG
  - Transitions, splitters, and crossings
  - Gratings and edge couplers
  - AWG, interleaver and ring filter
  - Bias diode and heater
  - PIN and PN ring modulators
  - Ge PDs
  - TSV-ready
- Additions
  - Ge APDs
  - Integrated lasers
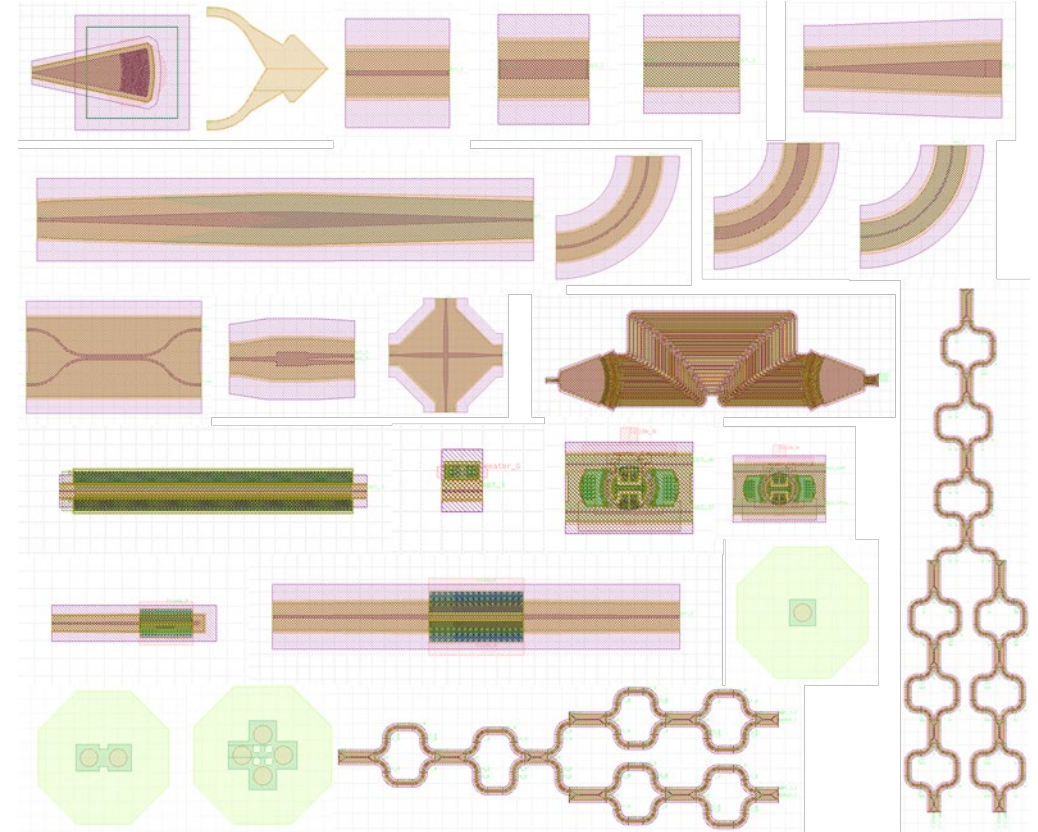
3D INTEGRATION CO-SIMULATION

- Co-Design Methodology for Silicon Photonics 3D IC
  - SI/PI using Ansys Electronics
  - also supports IR-Drop simulation
- Showed Thermal-Aware Photonic Circuit Simulation
  - Thermal Simulation using Ansys Icepak
  - Photonic Circuit Simulation using Ansys Lumerical INTERCONNECT
- Eliminate Design Issues in the Early Design Stages
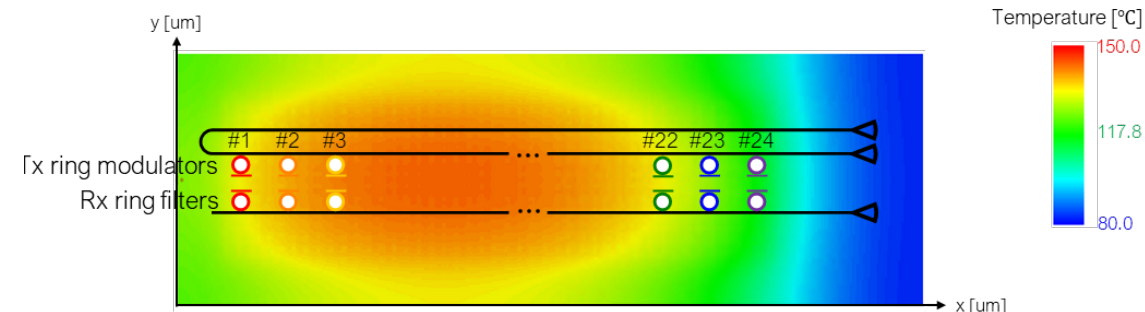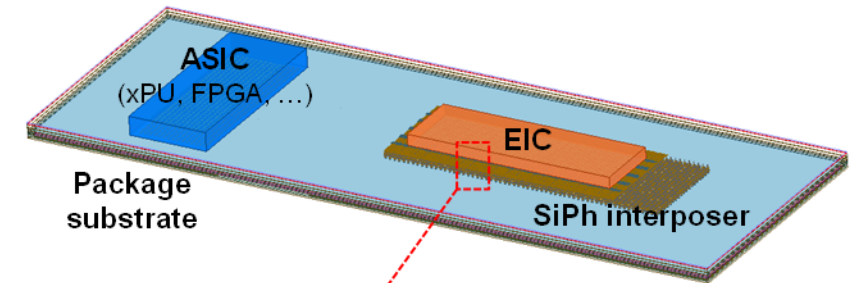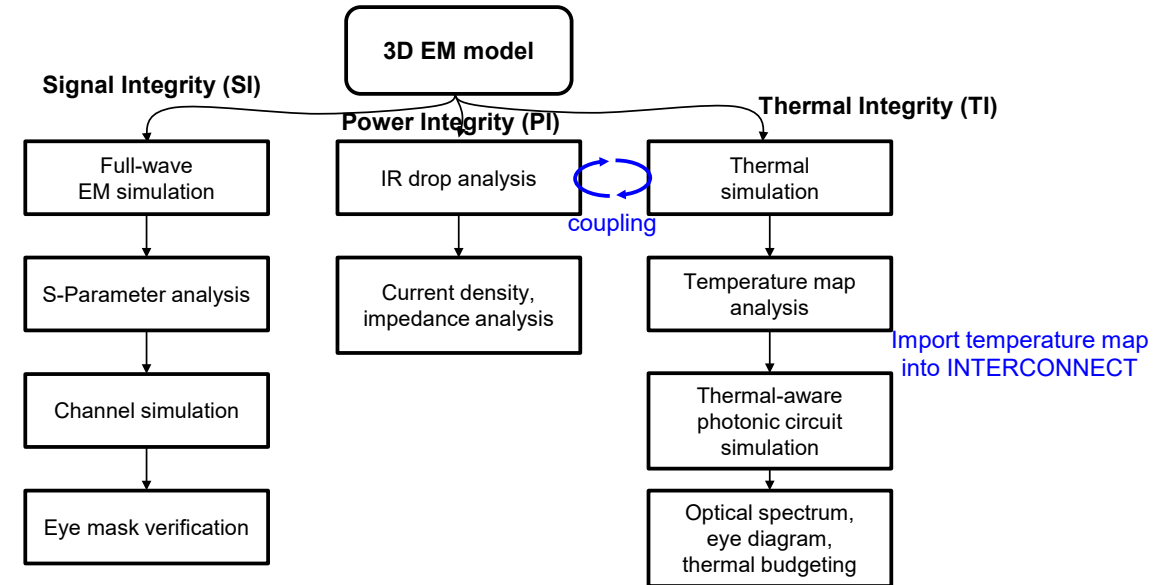
Jinsung Youn **"Electronic-Photonic IC Co-Design with Signal/Power Integrity and Thermal Simulation for Silicon Photonics 3D IC"** in DesignCon 2021.

FUTURE WORK

Still much work to do!

- Continued technology improvement
  - Demo of TSVs
  - Expand device portfolio with active components and APDs
  - Improve chip packaging
  - Develop high fiber count connectors
- Simplify supply chain
  - Consolidate suppliers
  - Simplify processes
- Continue recruiting partners/users
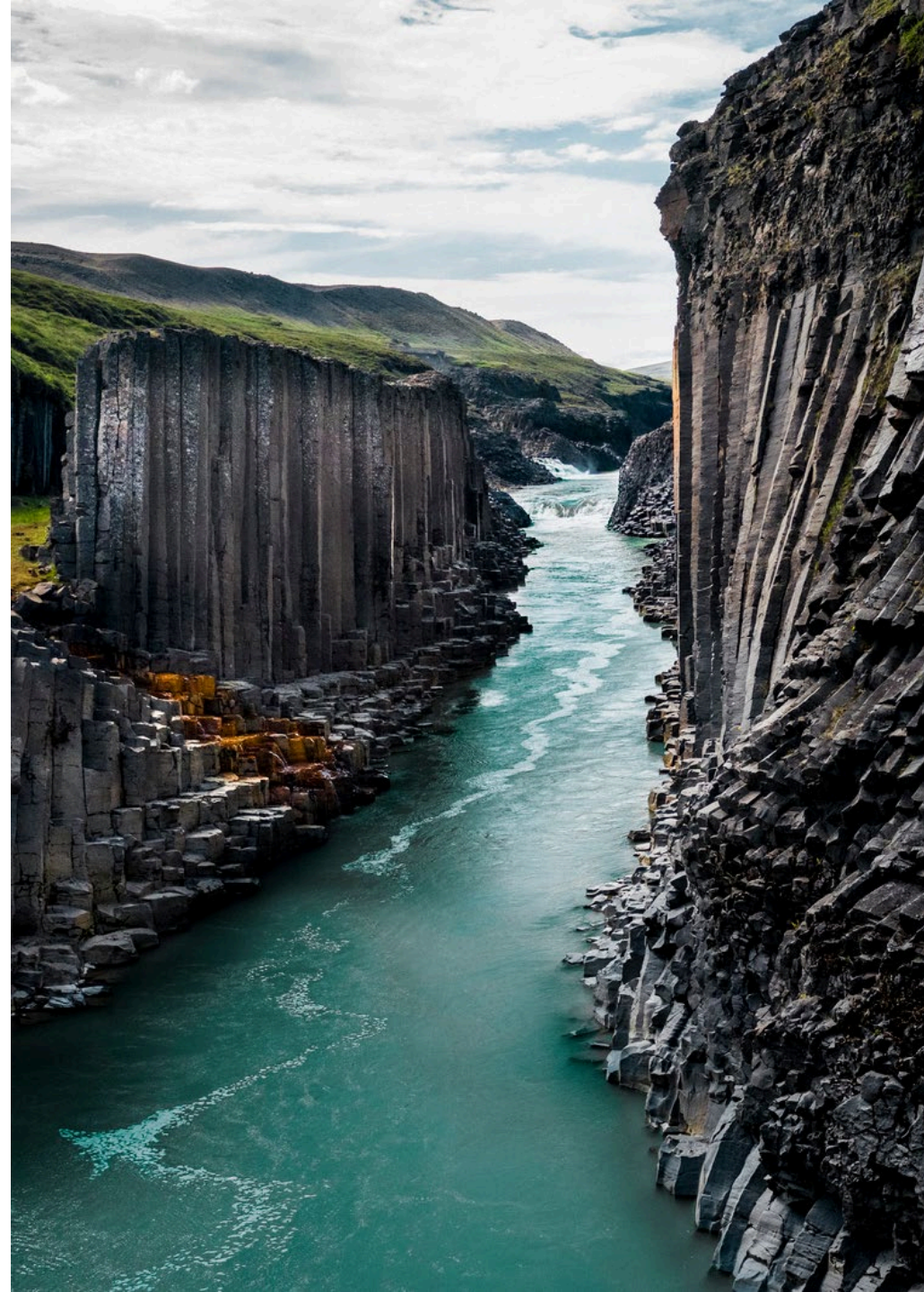
ACKNOWLEDGEMENTS

- Lab director: Ray Beausoleil
- SiPh ecosystem: Ashkan Seyedi (now at Nvidia)
- Process and verification: Peng Sun
- Design tools: Jared Hulme with Mentor Graphics and Lumerical
- 3D co-design: Jinsung Youn with Ansys/Lumerical
- PDK devices: Peter Rhim, Jinsung Youn, Jared Hulme
- Lasers: Di Liang and Geza Kurczveil with Innolume
- Packaging: Sagi Mathai with US Conec
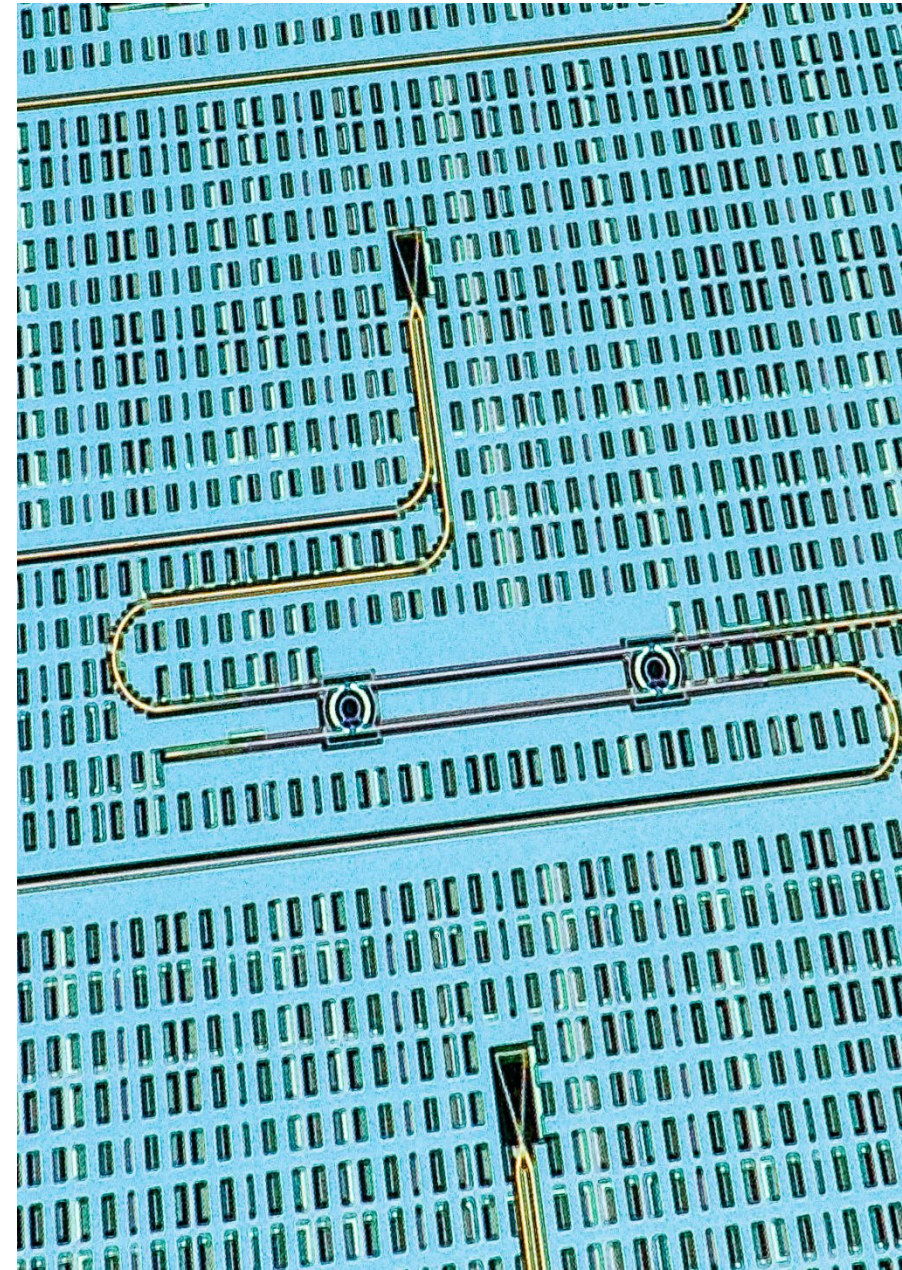
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