OPTICS

2023 Forum on Optical/Photonic Interconnects for Computing Systems

08-09 November, 2023

Starting at 5:00 PM Central European Time (CET): **08 Nov., 2023**
Starting at 1:00 PM Central European Time (CET): **09 Nov., 2023**

CEDA®
IEEE Council on Electronic Design Automation
Guangzhou Chapter

OPTICS 2023

Despite the slowdown of Moore's Law, applications from machine learning and edge computing to scientific computing and mobile computing continuously demand more performance under tighter cost, energy, and size constraints. Silicon-based photonic technologies advanced rapidly in the last two decades and have become promising solutions to complement electronic technologies. The OPTICS (optical/photonic interconnects for computing systems) workshop aims at discussing the latest advances in optics/photonics for computing systems, covering topics from fabrications, photonic devices, photonic circuits, architectures, system integrations, and design automation and optimization. The workshop targets researchers and engineers working on optics/photonics, electronics, architectures, systems, applications, and design automation.

Topics to be discussed include but are not limited to:

- PEDA (Photonic-Electronic Design Automation): layout, placement and routing, floorplan, crosstalk, thermal, process variation, etc.
- Photonic-electronic system integration and application: data center, HPC, automobile, aviation, etc.
- Photonics-based architecture: optical neural network, rack-scale optical network, inter/intra-chip optical network, optical switching, etc.
- Photonic/optic circuits: OE conversion, optical interconnect, optical computing circuit, etc.
- Photonic device and fabrication: laser, photodetector, modulator, switch, filter, etc

Organizing Committee

Dr. Minkyu Kim received the B.S. and Ph.D. degrees in Electrical and Electronics Engineering from Yonsei University, South Korea, in 2015 and 2021, respectively. His doctoral thesis concerned the monolithic silicon photonics transmitter with ring modulator and its temperature controller. From 2021, he joined IMEC as an R&D engineer where he is currently working on high-speed silicon photonics modulator design as well as I/O system design.

Dr. Luca Ramini received the M.S. degree in Electrical Engineering from the University of Ferrara in 2010 and the PhD from the same University in 2014. He has been technical leader of system-level cross-benchmarking efforts between optical interconnects and their electrical counterparts. Luca has been visiting researcher at Columbia University in 2011, Postdoc at the University of Ferrara and Contract Professor at the University of Verona from 2014 to 2016. From May 2016 to June 2019 he was senior silicon photonics designer at STMicroelectronics. Since July 2019 Luca joined the Large Scale Integrated Photonics Lab as a research scientist at Hewlett Packard Enterprise Labs. Luca's research interests include the design of silicon photonic circuits, network architectures, and systems. Luca is co-author of more than 35 scientific contributions including conference papers, journal papers, book chapters and US patent applications filed.

Dr. Yeyu Tong received the B.E. degree from the University of Electronic Science and Technology of China in 2016, and Ph.D. degree in Electronic Engineering from the Chinese University of Hong Kong supervised by Prof. Hon Ki Tsang in 2020. He was a visiting researcher at Prof. John Bowers' group at the University of California, Santa Barbara in 2019. He joined Interuniversity Microelectronics Center (IMEC) as an R&D Engineer from 2021 to 2022. Since 2022, Yeyu joined the Hong Kong University of Science and Technology (Guangzhou) as an assistant professor. His research interests include photonic integrated circuits, silicon photonics, optical interconnect, optical computing, passive and high-speed optoelectronic components. He has authored and co-authored more than 50 journal and conference publications. He also holds one US patent and publishes one book chapter.

Sessions Chairs (Day 1)

Ahsan Alam is a Lead R&D Engineer at Ansys. His areas of expertise include simulation and modeling of solid state electronic and photonic devices and circuits. As the lead for developing Ansys's photonic design solutions, he collaborates with key customers and foundry partners to establish a comprehensive electronic-photonic design automation (EPDA) ecosystem. He is also involved in the development of Ansys Lumerical's system suite and plays the role of a product manager.

Mahdi Nikdast is an Associate Professor and an Endowed Rockwell-Anderson Professor in the Department of Electrical and Computer Engineering at Colorado State University (CSU), Fort Collins, where he is directing the Electronic-PhotoniC System Design (ECSyD) Laboratory. His research interests are at the intersection of integrated photonics, silicon photonics, and high-performance computing systems.

Sessions Chairs (Day 2)

Jiang Xu received his PhD from Princeton University and worked at Bell Labs, NEC Labs, and a startup company before joining the Hong Kong University of Science and Technology (HKUST). He is the Founding Head of Microelectronics Thrust at HKUST(GZ). Prof. Xu is the Hong Kong Chapter Chair of IEEE Council on EDA. He serves as the Associate Editor for IEEE TVLSI and on the steering committees, organizing committees, and technical program committees of many international conferences, including OFC, DAC, DATE, ICCAD, CASES, ICCD, CODES+ISSS, NOCS, HiPEAC, ASP-DAC, etc. Prof. Xu is awarded IEEE Computer Society Distinguished Contributor as the Charter Member in 2021. He was an IEEE Computer Society Distinguished Visitor and an ACM Distinguished Speaker. He authored and coauthored more than 150 book chapters and papers in peer-reviewed international journals and conferences. Prof. Xu and his students received Best Paper Award from the International Symposium on Memory Systems in 2023, IEEE Technical Committee on VLSI Best Paper Award of ISVLSI in 2018, Best Paper Award from IEEE Computer Society Annual Symposium on VLSI in 2009, and Best Poster Award from AMD Technical Forum and Exhibition in 2010. His research areas include machine learning system, photonic-electronic codesign, optical interconnection network, and hardware/software codesign.

Marco Fiorentino received the Ph.D. degree in physics from the University of Naples, Naples, Italy, in 2000. His doctoral work focused on quantum optics. He is currently a Research Scientist with Large Scale Integrated Photonics Lab, Hewlett Packard Enterprise Labs, Milpitas, CA, USA. Before working with the HP/HPE Labs, in 2005, he was with the Northwestern University, Evanston, IL, USA, University of Rome, Rome, Italy, and MIT. In the past, he has worked on optics, high-precision measurements, and optical communications. He has authored or coauthored more than 50 papers in peer-reviewed journals and given numerous contributed and invited talks to international conferences. He is a Senior Member of the Optical Society of America.

Workshop Overview

Time Zone: Central European Time (CET)

Day 1 Wednesday, November 8, 2023

05:00 PM **Workshop Opening**

05:10 PM **Session 1#**

Exploring Photonic Technologies/Circuits for High Performance Computing and AI applications I

05:10 PM ◦ **Marco Sampietro**: Integrated Electronics Tailored for Integrated Photonics

05:30 PM ◦ **Bassem Tossoun**: Energy-Efficient Integrated Photonics for Next-Generation Computing

05:50 PM ◦ **David Z. Pan**: Photonic AI via Cross-layer Circuit-Architecture-Algorithm Co-design

06:10 PM ◦ **Bhavin Shastri**: Neuromorphic Silicon Photonics and Applications from Classical to Quantum

06:30 PM **Break**

06:45 PM **Session 2#**

Future High-Capacity Optical Interconnects and Advanced Electronic-Photonic Co-Design

06:45 PM ◦ **Benjamin G. Lee**: Scaling Accelerated Computing with Photonics

07:05 PM ◦ **Duanni Huang**: Silicon photonic WDM transceiver with integrated lasers and SOA for optical I/O

07:25 PM ◦ **S. J. Ben Yoo**: 3D Electronic-Photonic integrated circuits for future high-performance AI application

07:45 PM ◦ **Zeqin Lu**: Modeling Electro-Optical Integrated Circuits using Verilog-A

08:05 PM **Day 1 Workshop Closing**

Day 2 Thursday, November 9, 2023

01:00 PM **Workshop Opening**

01:10 PM **Session 3#**

Advances in Photonic Design Automation and Co-packaged Optics Standards

01:10 PM ◦ **Woo-Young Choi**: Electronics-Friendly Si Ring Modulator Models

01:30 PM ◦ **Qinfen Hao**: The Technology Challenge in Practice around China CPO Standard

01:50 PM ◦ **Pieter Dumon**: Functional Verification of Advanced Photonic ICs

02:10 PM ◦ **Alexandre Truppel**: Accurate Infinite-Order Crosstalk Calculation for Optical Networks-on-Chip

02:30 PM **Break**

02:45 PM **Session 4#**

Exploring Photonic Technologies/Circuits for High Performance Computing and AI applications II

02:45 PM ◦ **Yoojin Ban**: Silicon Photonics Technologies for Next-Generation Computing

03:05 PM ◦ **Bin Shi**: Massive Parallelisms for WDM-based Photonic Integrated Convolutional Processor

03:25 PM ◦ **Andrea Melloni**: Self-adaptive Photonic Integrated Processors for Communication and Computing

03:45 PM **Day 2 Workshop Closing**

Integrated Electronics Tailored for Integrated Photonics

08:10 PST, 11:10 EST, 17:10 CET, 00:10 China

Marco Sampietro
Professor
Politecnico di Milano, Italy

Abstract

The integration of basic electronic building blocks, if not entire electronic circuits, into photonic chips are enabling real-time control of interpherometric meshes, thus defining their working points against thermal drifts or fabrication tolerances, opening the realm for stable and effective dynamic optical processing. The presentation focuses on the vision of Politecnico di Milano in integrating electronic functionalities into the best photonic platforms at zero-change in technology, to ensure optical excellence at zero-price. By exploiting a non-conventional structure of MOSFETs, results will be presented of an electronic controller co-designed into a programmable photonic circuit to enable time-multiplexed readout of integrated photodetectors and sequential activation of thermal phase shifters with on-chip electronic memory. The accuracy of the time-multiplexed control, achieved on a time scale of less than 10 ms, is demonstrated by penalty-free routing of 10 Gbit/s modulated signals.

Speaker Bio:

Marco Sampietro (Member IEEE), born in 1957, is full professor of Electronic Circuits and Devices at Politecnico of Milano, Italy. He is responsible for the activities in high-sensitivity instrumentation for the nanoscience, with a focus on the design of electronic circuits for monitoring, tracking and feedback controlling the working point of optical micro-integrated devices and he has coordinated the activity on the electronic system platform to exploit photonic probes on complex photonic architectures. He is co-author of more than 230 peer-reviewed international publications and holds 5 patents. He is the co-founder of POLIFAB, the micro and nano technology facility at Politecnico di Milano. He has been the coordinator of many national and international research projects and scientific partner in seven large-size European projects within the FP6, FP7 and HORIZON2020 (STREAMS, NEBULA). From 2012 to 2018, he has been the Dean of the Bachelor's and Master's Course Program in Electronics Engineering.

Energy-Efficient Integrated Photonics for Next-Generation Computing

08:30 PST, 11:30 EST, 17:30 CET, 00:30 China

Bassem Tossoun
Research Scientist
Hewlett Packard Labs, USA

Abstract

Integrated photonic computing promises revolutionary strides in processing power, energy efficiency, and speed, propelling us into an era of unprecedented computational capabilities. By harnessing the innate properties of light, such as high-speed propagation, inherent parallel processing capabilities, and the ability to carry vast amounts of information, photonic computing transcends the limitations of traditional electronic architectures. Furthermore, silicon photonic neural networks hold promise to transform artificial intelligence by enabling faster training and inference with significantly reduced power consumption. This potential leap in efficiency could revolutionize data centers, high performance computing, and edge computing, minimizing environmental impact while expanding the boundaries of computational possibilities. The latest research on our silicon photonic platform for next-generation optical computing accelerators will be presented and discussed.

Speaker Bio:

Bassem Tossoun received his PhD in Electrical Engineering at the University of Virginia in 2019 with his research interests including silicon photonics and the design, fabrication, and characterization of optoelectronic devices for data communications and information processing. Currently, he is a Research Scientist at Hewlett Packard Labs working on heterogeneously integrated III-V on silicon photonic devices and circuits for next-generation optical computing.

Photonic AI via Cross-layer Circuit-Architecture-Algorithm Co-design

08:50 PST, 11:50 EST, 17:50 CET, 00:50 China

David Z. Pan
Chair Professor,
University of Texas at Austin, USA

Abstract

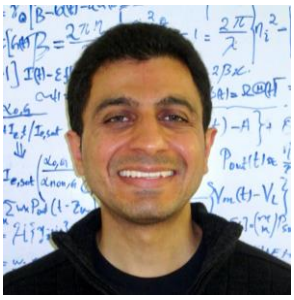
There has been increasing interests in developing photonic AI accelerators for the next generation datacenters, smart sensing, intelligent edge, and automotive computing. However, realizing its full potential requires overcoming significant design challenges through a cross-layer co-design approach, where devices, circuits, architectures, and algorithms are optimized together. In this talk, I will present some recent work with perspectives of our customized photonic device, circuit, architecture, and software co-design for efficient machine learning, including a butterfly-style optical subspace neural network architecture [ACS Photonics 2022], a compact-device based co-design framework SqueezeLight [TCAD'23], and a new photonic tensor core design for Transformer workloads [SNAP@MLSys'23].

Speaker Bio:

David Z. Pan is Silicon Laboratories Endowed Chair Professor at the Chandra Department of Electrical and Computer Engineering, The University of Texas at Austin. His research interests include electronic design automation, synergistic AI and IC co-optimizations, design for manufacturing, hardware security, and design/CAD for analog/mixed-signal and emerging technologies. He has published over 480 refereed journal/conference papers and 9 US patents. He has served in many editorial boards and conference committees, including various leadership roles such as DAC 2024 TPC Chair, ICCAD 2019 General Chair, and ISPD 2008 General Chair. He has received many awards, including 20 Best Paper Awards (from TCAD, DAC, ICCAD, DATE, ASP-DAC, ISPD, HOST, SRC, IBM, etc.), SRC Technical Excellence Award, DAC Top 10 Author Award in Fifth Decade, ASP-DAC Frequently Cited Author Award, NSF CAREER Award, IBM Faculty Award (4 times), and many international CAD contest awards. He has held various advisory, consulting, or visiting positions in academia and industry, including MIT and Google. He has graduated 52 PhD students and postdocs who have won many awards, including ACM Student Research Competition Grand Finals 1st Place twice and Outstanding PhD Dissertation Awards from ACM/SIGDA and EDAA 5 times. He is a Fellow of ACM, IEEE, and SPIE.

Neuromorphic Silicon Photonics and Applications from Classical to Quantum

09:10 PST, 12:10 EST, 18:10 CET, 01:10 China



Bhavin Shastri
Assistant Professor
Queen's University, Canada

Abstract

Artificial intelligence (AI) powered by neural networks has enabled applications in many fields (medicine, finance, autonomous vehicles). Digital implementations of neural networks are limited in speed and energy efficiency. Neuromorphic photonics aims to build processors that use light and photonic device physics to mimic neurons and synapses in the brain for distributed and parallel processing while offering sub-nanosecond latencies and extending the domain of AI and neuromorphic computing applications. We will discuss photonic neural networks enabled by CMOS-compatible silicon photonics. We will highlight applications that require low latency and high bandwidth, including wideband radio-frequency signal processing, fiber-optic communications, and nonlinear programming (solving optimization problems). We will briefly introduce a quantum photonic neural network that can learn to act as near-perfect components of quantum technologies and discuss the role of weak nonlinearities.

Speaker Bio:

Prof. Shastri is an Assistant Professor of Engineering Physics at Queen's University and a Faculty Affiliate at Vector Institute. He received a Ph.D. degree in electrical engineering from McGill University in 2012 and was a Banting Postdoctoral Fellow at Princeton University. Dr. Shastri is the recipient of the 2022 SPIE Early Career Achievement Award and the 2020 IUPAP Young Scientist Prize in Optics "for his pioneering contributions to neuromorphic photonics." He is a co-author of the book Neuromorphic Photonics, a term he coined with Prof. Prucnal. He is a Senior Member of Optica and IEEE.

Scaling Accelerated Computing with Photonics

09:45 PST, 12:45 EST, 18:45 CET, 01:45 China

Benjamin G. Lee
Senior Research Scientist
NVIDIA, USA

Abstract

GPU-based accelerated computing is at the center of the AI revolution. Today's GPU systems rely on clusters of high-performance processors and switching ASICs that scale out through a high-performance network fabric. Photonic transceivers have an opportunity to improve the thermal density and performance of future systems, if they can meet the stringent efficiency and cost targets. I will explore the drivers and requirements for using integrated optics in future AI systems.

Speaker Bio:

Benjamin G. Lee is a Senior Research Scientist in NVIDIA's Circuits Research Group where he explores photonic architectures for future accelerated computing systems. Before joining NVIDIA, he worked at IBM's T. J. Watson Research Center from 2009 to 2021. He received a Ph.D. from Columbia University in 2009 in electrical engineering. Dr. Lee has contributed to research in optical packaging, multimode and single-mode interconnects, photonic switch fabrics, and optical networks. He has published over 150 peer-reviewed journal and conference papers and holds 20 granted US patents.

Silicon Photonic WDM Transceiver with Integrated Lasers and SOA for Optical I/O

10:05 PST, 13:05 EST, 19:05 CET, 02:05 China

Duanni Huang,
Senior Research Scientist
Intel Labs, Santa Clara, USA

Abstract

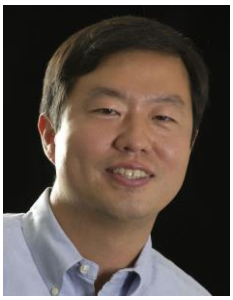
Optical I/O is a chip-to-chip interconnect application that requires very high optical bandwidth density, low energy consumption, and the ability to scale to high-volume production. To meet these challenging demands, tight integration is required between all the optical components as well as all the control and drive electronics. We demonstrate an 8λ×32Gbps/λ WDM transceiver with eight 200GHz-spaced wavelengths simultaneously modulated at 32Gbps and <1e-12 BER. The system includes a silicon photonic PIC with integrated lasers, microring modulators, SOAs, Ge photodetectors, and a co-designed CMOS EIC.

Speaker Bio:

Dr. Duanni Huang received his B.S. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2013, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Santa Barbara, Santa Barbara, CA, USA, in 2015 and 2019, respectively. He is currently a senior research scientist with Intel Labs in Santa Clara, working on silicon photonic integrated circuits with an emphasis on heterogeneous integration of III-V and other materials with silicon.

3D Electronic-Photonic Integrated Circuits for Future High-Performance AI Applications

10:25 PST, 13:25 EST, 19:25 CET, 02:25 China



S. J. Ben Yoo
Distinguished Professor
University of California, Davis, USA

Abstract

We will discuss Brain-Derived Neuromorphic Computing architectures exploiting attojoule spiking optoelectronic neurons and hierarchical Photonic-Electronic Synaptic Interconnection Networks with tensor-train decomposition. 3D Electronic-Photonic-Integrated-Circuit implementations with sparsity in temporal, spectral, and spatial domains expect to achieve brain-like scalability and energy-efficiency as well as self-learning capabilities.

Speaker Bio:

S. J. Ben Yoo is a Distinguished Professor at the University of California at Davis (UC Davis). His research at UC Davis includes 2D/3D photonic integration for future computing, cognitive networks, communication, imaging, and navigation systems, micro/nano systems integration, and the future Internet. Prior to joining UC Davis in 1999, he was a Senior Research Scientist at Bellcore, leading technical efforts in integrated photonics, optical networking, and systems integration. His research activities at Bellcore included the next-generation Internet, reconfigurable multiwavelength optical networks (MONET), wavelength interchanging cross connects, wavelength converters, vertical-cavity lasers, and high-speed modulators. He led the MONET testbed experimentation efforts, and participated in ATD/MONET systems integration and a number of standardization activities. Prior to joining Bellcore in 1991, he conducted research on nonlinear optical processes in quantum wells, a four-wave-mixing study of relaxation mechanisms in dye molecules, and ultrafast diffusion-driven photodetectors at Stanford University (BS'84, MS'86, PhD'91, Stanford University). Prof. Yoo is Fellow of IEEE, OSA, NIAC and a recipient of the DARPA Award for Sustained Excellence, the Bellcore CEO Award, the Mid-Career Research Faculty Award (UC Davis), the Senior Research Faculty Award (UC Davis), and numerous best paper awards from IEEE, ACM, and OSA (Optica) conferences.

Modeling Electro-Optical Integrated Circuits using Verilog-A

10:45 PST, 13:45 EST, 19:45 CET, 02:45 China

Zeqin Lu,
Lead R&D Engineer,
Ansys, Canada

Abstract

Photonic integrated circuits (PICs) are often controlled or driven by electronic integrated circuits (EICs). Ideally, EIC and PICs should be co-designed in a single schematic and be co-simulated to capture the tight interaction between the optical and electrical domains, such as photonic components' loading effects to the EICs and electrical feedback loops between the two domains. This allows designers to analyze and optimize the overall performance. Verilog-A models are analog behavioral models that can be solved by SPICE solvers and are commonly used for EIC designs. In this talk, we will present the use of standard Verilog-A language for modeling advanced photonic components in PIC analysis, where complex, bidirectional, multimodal, and multi wavelength optical signal are fully supported. As an example, we will demonstrate the co-design and co-simulation for a 4-channel, dense-wavelength division-multiplexing (DWDM) silicon photonic transceiver and its electrical drivers and receivers. Besides, we will showcase Ansys' automated tools and workflows that can generate photonic Verilog-A models for users' custom devices.

Speaker Bio:

Zeqin Lu is a Lead R&D engineer at Ansys. He joined Ansys in 2017 and has been leading the solution development for enabling electro-photonic integrated circuit designs, especially with focuses on design tools integration, advanced photonic compact models, and design automation workflows. Prior to Ansys, he received his PhD degree at the University of British Columbia, where he worked on silicon photonic component and circuit designs.

Electronics-Friendly Si Ring Modulator Model

04:10 PST, 07:10 EST, 13:10 CET, 20:10 China

Woo-Young Choi,
Professor,
Yonsei University, Korea

Abstract

The Si ring modulator, with its high-bandwidth modulation capability and small size, has become the key photonic component of optical interconnect solutions for high-performance electronics systems, where bandwidth density is the key performance metric. For these photonic I/O applications, the best system performance can be achieved through the co-optimization of electronics and photonics. To achieve this, there is a strong need to develop an accurate and easy-to-implement Si ring modulator model in the standard electronics design environment. Such a Si ring modulator model will be presented, and its application in designing a high-performance Si photonic transmitter containing Si ring modulator, driver electronics, and ring modulator temperature controller will be provided.

Speaker Bio:

Woo-Young Choi received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 1986, 1988, and 1994, respectively. His doctoral dissertation was on MBE-grown InGaAlAs laser diodes for fiber-optic applications. From 1994 to 1995, he was a Postdoctoral Research Fellow at NTT Opto-Electronics Laboratories, where he worked on femtosecond all-optical switching devices based on low-temperature grown InGaAlAs quantum wells. In 1995, he joined the Department of Electrical and Electronic Engineering, Yonsei University, Seoul, South Korea, where he is currently a full professor. His current research interests include high-speed circuits and systems that include high-speed interface circuits and silicon photonics.

The Technology Challenge in Practice Around China CPO Standard

04:30 PST, 07:30 EST, 13:30 CET, 20:30 China

Qinfen Hao,
Professor,
Chinese Academy of Sciences, China

Abstract

Thanks to the rise of new technologies represented by AI-generated content in recent years, the field of data center optical interconnection has received unprecedented investment. As optical interconnection bandwidth increases, conventional optical modules are bound to evolve towards co-packaged optics (CPO) due to the difficulty in maintaining the increasing demand for rate. The CPO switches and CPO transceivers, despite facing diverse technical challenges at present, have garnered significant attention due to their remarkable benefits in terms of power consumption, cost, and bandwidth density. Standardization is crucial for the ecological development of CPO and requires the collaborative efforts of multiple vendors within the ecosystem. However, formulating CPO standard requires solving many problems such as system architecture, connectors, external laser light sources, mechanical specifications, optical and electrical signal specifications, etc. In addition, the formulation of CPO standard also needs to consider the current technological status of China, thereby promoting the development of CPO in China.

Speaker Bio:

Qinfen Hao, received Ph.D degree in Computer Architecture from Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China, in 2001. After a long career in industry, he is now working in Institute of Computing Technology, CAS as a professor. He has participated in multiple national research projects and was awarded Chinese National award for science and technology progress twice and Beijing Science and Technology Award once. Based on these research project, he now published over 40 research papers and applied over 30 patents. His research interests now include Co-packaged Optics (CPO), Chip-let technology and novel computer architecture.

Functional Verification of Advanced Photonic ICs

04:50 PST, 07:50 EST, 13:50 CET, 20:50 China

Pieter Dumon
CTO,
Luceda Photonics, Belgium

Abstract

Photonic ICs are increasing in complexity with increasing integration level in data communication chips as well as novel applications such as industrial and medical sensing, LIDAR, quantum computing and communications. Pieter will present recent advances in verification of such ICs by means of netlist extraction, schematic design review and simulation.

Speaker Bio:

Pieter Dumon is CTO and co-founder of Luceda Photonics, where he is engaged in software development, PDK development, circuit and device modeling and professional services. Pieter obtained his EE master's degree from Ghent University in 2002 and a PhD in photonics in 2007. At the Photonics Reseearch Group and imec, he coordinated ePIXfab, the first small-volume prototyping service for silicon photonics from 2007 until 2014 and has been involved in semiconductor technology development and design.

Accurate Infinite-Order Crosstalk Calculation for Optical Networks-on-Chip

05:10 PST, 08:10 EST, 14:10 CET, 21:10 China

Alexandre Truppel,
PhD student,
Technical University of Munich, Germany

Abstract

Optical Networks-on-Chip (ONoCs) are becoming more and more appealing due to rising network requirements in integrated circuits. One important aspect in ONoC design is the amount of crosstalk generated by the network because crosstalk and Signal-to-Noise Ratio (SNR) are strong limiting factors to network scale and performance. Calculation of crosstalk is thus essential for effective ONoC design. Motivated by this fact, we developed a new general linear algebra based method to calculate the steady-state of any system obeying a simple set of rules. We prove that ONoCs follow these rules and show how this general method can be applied in the particular case of ONoCs to calculate accurate first-order and infinite-order crosstalk and SNR results for any ONoC network.

Speaker Bio:

Alexandre Truppel received the bachelor's and master's degrees in electrical and computer engineering from the University of Porto, Porto, Portugal, in 2016 and 2018, respectively. He is currently working toward the Ph.D. degree as a Doctoral Researcher at the Technical University of Munich, Munich, Germany. His research focuses on the development and use of optimization techniques in emerging technologies, such as optical networks-on-chip.

Silicon Photonics Technologies for Next-Generation Computing

05:45 PST, 08:45 EST,14:45 CET, 21:45 China

Yoojin Ban,
Program Manager,
IMEC, Belgium

Abstract

Silicon photonics has grown as a main driver for scaling intra-data-center communication infrastructure. Recently it has emerged as a possible solution for ultra short reach interconnects as needed for the most demanding compute applications such as machine learning now facing the limits of electrical I/O scaling in terms of bandwidth, energy efficiency. In this presentation, we will discuss how Si photonics enables next generation computing like extensive machine learning. Other emerging applications based on Si photonics like automotive lidar system or optical quantum computing will be shortly introduced.

Speaker Bio:

Yoojin Ban is program manager of the industry-affiliation R&D program on Optical I/O at IMEC since 2021 which targets the development of a scalable and industrially viable optical interconnect technology based on silicon photonics. Before that she spent 6 years as responsible for the Si Photonics device development and Si Photonics based optical transceiver demonstration at IMEC. She received M.E degree in electrical and electronics engineering from Yonsei University, South Korea, in 2015 for her works on Si photonics micro-ring modulator.

Massive Parallelisms for WDM-based Photonic Integrated Convolutional Processor

06:05 PST, 09:05 EST, 15:05 CET, 22:05 China

Bin Shi,
Postdoctoral Researcher,
Eindhoven University of Technology, Netherlands

Abstract

We exploit massive parallelisms from the nature of light to accelerate the convolutional processing for photonic convolutional neural networks. The proposed additional parallelism with combination of space and wavelength domains, provided by cyclic array waveguide grating, improves the computing speed of the WDM-based convolutional operation on chip by 10s times with respecting to the state-of-the-art photonic integrated convolutional processors, suggesting up to 40 Tera Operations/s for a chip with 64 weighting elements.

Speaker Bio:

Bin Shi received the B.S. degree in optical information science from the China University of Mining and Technology, Xuzhou, China, in 2014, and the M.S. degree in lasers and photonics from Ruhr University Bochum, Bochum, Germany, in 2017. He received the Ph.D. degree from the Eindhoven University of Technology, Eindhoven, The Netherlands, in 2022. He is currently a Postdoctoral Researcher with Eindhoven Hendrik Casimir Institute (formerly IPI), Eindhoven University of Technology, Eindhoven, the Netherlands. His research interests include photonic neural network, photonic integrated circuits, optical beamforming, and optical switching. He has authored and co-authored more than 30 peer-reviewed journal and international conference papers, including 4 invited journal papers. He is an active reviewer for journals including Journal of Selected Topics in Quantum Electronics, Journal of Lightwave Technology, and Nature Photonics, etc.

Self-adaptive Photonic Integrated Processors for Communication and Computing

06:25 PST, 09:25 EST, 15:25 CET, 22:25 China

Andrea Melloni,
Professor
Politecnico di Milano, Italy

Abstract

An integrated photonic processor consisting of a mesh of Mach-Zehnder Interferometers as photonic core and a co-integrated electronic control circuit is presented. The optical processor performs generation, manipulation, and shaping of the optical free space beams, and establishes orthogonal free-space channels through scattering media and perform matrix algebra mathematical computations. The self-adaptive control scheme stabilizes the working point of each photonic device and enables a fast and low power consumption automatic handling of the photonic programmable processor.

Speaker Bio:

Andrea Melloni, OSA Fellow, Full Professor at Politecnico di Milano-Italy with Chair in Electromagnetic Fields, leader of the Photonic Devices group, Director of Polifab, the facility for micro and nano technologies at Politecnico di Milano. His field of research is in integrated optical devices for optical communication, sensing and optical processing, now focusing on adaptive control, stabilization and testing of large photonic integrated circuits. He is author of more than 400 publications, 18 patents and 3 book chapters.