Model electro-optical integrated circuits using Verilog-A

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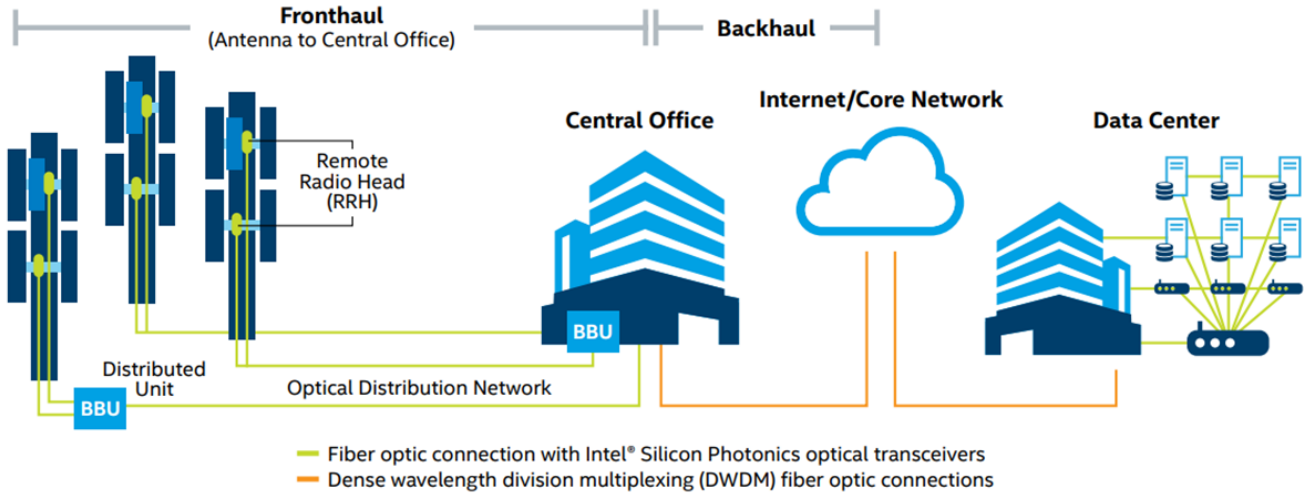
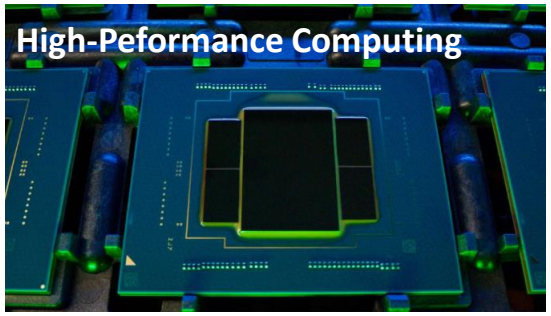
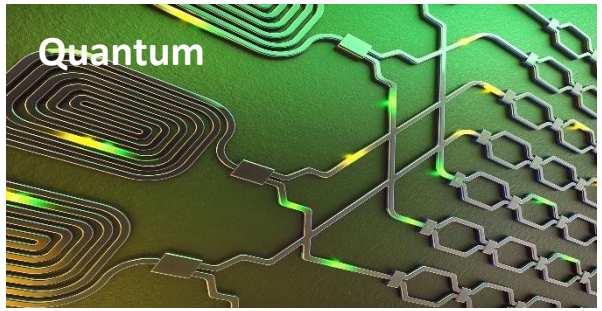
Photonics is a Key Enabler of 5G, Data Centers, AI and More



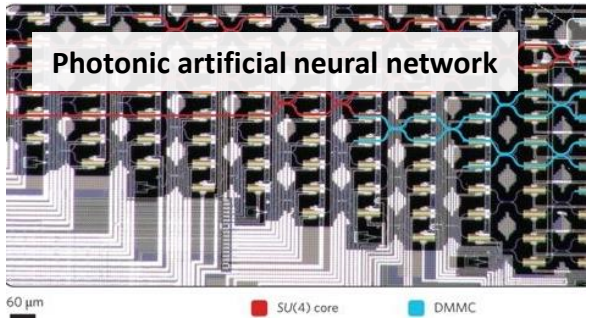
Source: "Exploring 5G Fronthaul Network Architecture Intelligence Splits & Connectivity" 5G Wireless Communications – Silicon Photonics, Intel



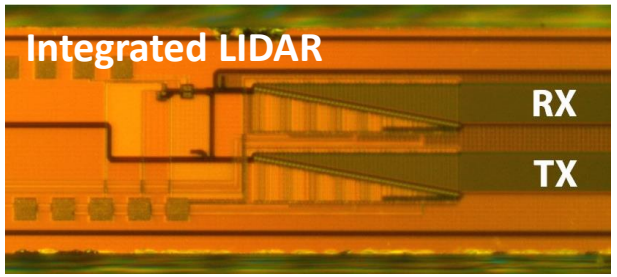
High Performance Computing | Ayar Labs In-Package Optical I/O
https://ayarlabs.com/high-performance-computing/



https://spectrum.ieee.org/tech-talk/computing/hardware/building-quantum-computers-with-photons
Image: Xiaogang Qiang/University of Bristol



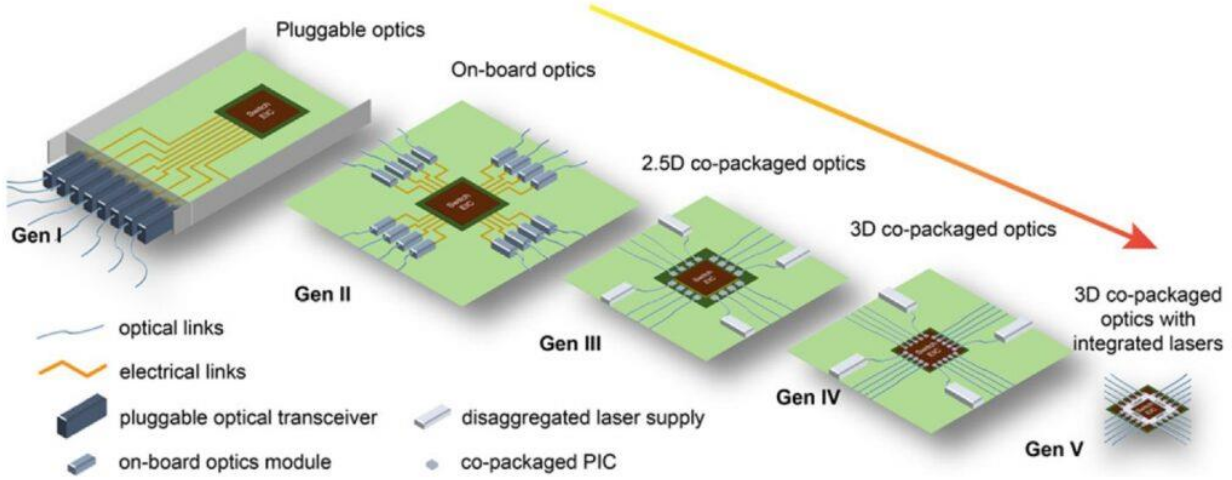
Y. Shen et al. Deep learning with coherent nanophotonic circuits,
Nature Photonics,
https://doi.org/10.1038/nphoton.2017.93



MIT and DARPA Pack Lidar Sensor Onto Single Chip
https://spectrum.ieee.org/tech-talk/semiconductors/optoelectronics/mit-lidar-on-a-chip
Image: Christopher V. Poulton

The trends…

- The rising demands for compute power;
- Optical interconnects will continue to replace copper to bring the power consumption down.
- Photonic packaging evolves quickly and moves towards 3DIC
- **Challenges:**
  - **Signal integrity: EIC & PIC should be co-designed to optimize their overall performance**
  - **Thermal integrity**
  - **Optical I/O**



Ref: "Perspective on the future of silicon photonics and electronics" N. Margalit, et.al., Appl. Phys. Lett. 118, 220501 (2021)

Agenda

- Basic: model optical signal using Verilog-A
- Advanced photonic Verilog-A models
- Create Verilog-A models through automation
- Example: 4-ch DWDM SiP transceiver design
- Key takeaway

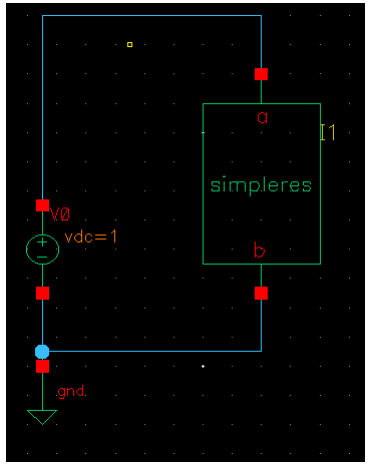
Basics of photonic Verilog-A

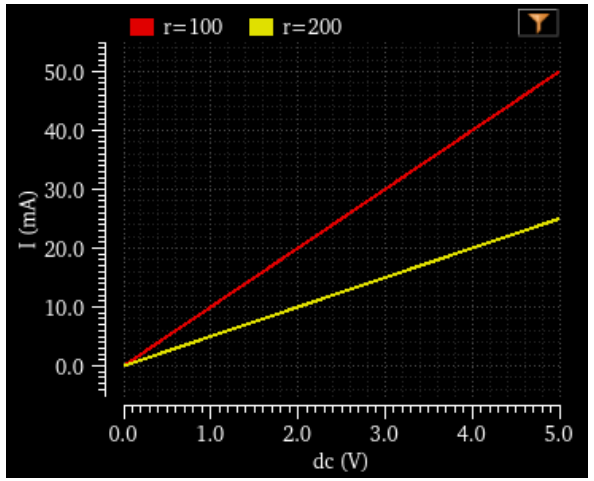
Ansys

What is Verilog-A model?

- Verilog-A models are analog behavior models that can be solved by SPICE circuit solvers.
- Verilog-A model behavior and ports can be customized by script.
- Compatible with various electrical analyses (dc, ac, tran)

```
module simpleres(a, b);
   inout a, b;
   electrical a, b;
   parameter real r = 1000 from (0:inf);

   analog begin
      I(a,b) <+ V(a,b) / r;
   end
endmodule
```





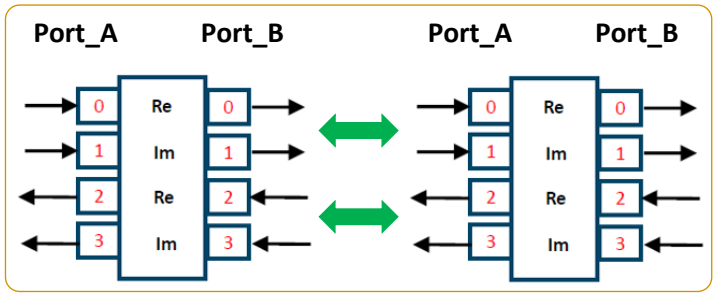
How to simulate optical signal using Verilog-A?

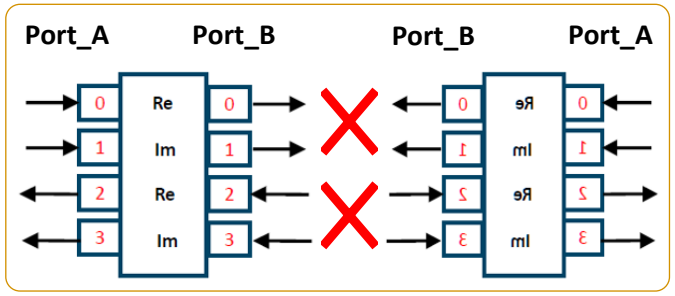
- Electrical signal includes potential and flow
- Optical signal is complex (Re & Im), frequency-dependent, mode-dependent, and bidirectional.
- Workaround:
  - Optical signal is represented by buses
  - Each port is a structured port
  - Analytically describe input-to-output signal transmission (single directional)

```
`include "../../../../cad/constants.vams"
`include "../../../../cad/disciplines.vams"

module Optical_Waveguide(inLight, outLight);
    inout   [0:3]   leftLight;  // [0:1] is left side input, [2:3] is left side output
    inout   [0:3]   rightLight; // [0:1] is right side output [2:3] is right side input.  optical
    [0:3]  rightLight, leftLight;

    // Physical Design Parameters, all units in SI
    parameter real L = 0.0005;          // length
    parameter real ng  = 4.1963;        // group index
    parameter real np = 2.1;            // refractive index
    parameter real alphaA = 287.6;      // loss
    parameter real G_freq = 1.93e14;    // reference frequency parameter passed in from
    top level simulation

    // initialize intermediate points
    optical [0:1] rightOutput;
    optical [0:1] leftOutput;
    optical [0:1] transfer; // for calculated phase-shift and amplitude change
    optical [0:1] transferCart; // for above in real and imaginary forms

    pol2cart convs1(transfer, transferCart); // convert waveguide effect to real and
    imaginary parts
    cartmul mulout1(transferCart, leftLight[0:1], rightOutput);   //Calc outputs
    cartmul mulout1B(transferCart, rightLight[2:3], leftOutput);

    analog begin
        //calculate phase-shift and amplitude change in polar coordinates
        E(transfer[0]) <+ (-L*np*2*`M_PI*G_freq/`P_C)%(2*`M_PI);
        E(transfer[1]) <+ exp(-alphaA*L);

        // Output delayed signals
        E(rightLight[0]) <+ absdelay(E(rightOutput[0]), L*ng/`P_C);
        E(rightLight[1]) <+ absdelay(E(rightOutput[1]), L*ng/`P_C);
        E(leftLight[2]) <+ absdelay(E(leftOutput[0]), L*ng/`P_C)
        E(leftLight[3]) <+ absdelay(E(leftOutput[1]), L*ng/`P_C);
    end
endmodule
```

C. Sorace-Agaskar, et. al.,, "Electro-optical co-simulation for integrated CMOS photonic circuits with VerilogA," Opt. Express 23, 27180-27203 (2015)

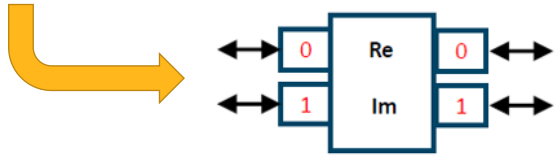
Photonic SPICE/Verilog-A challenges

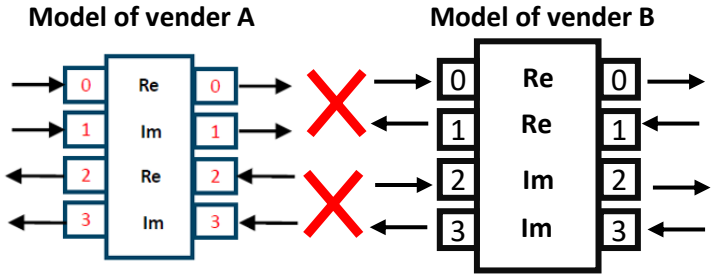




Challenge 1

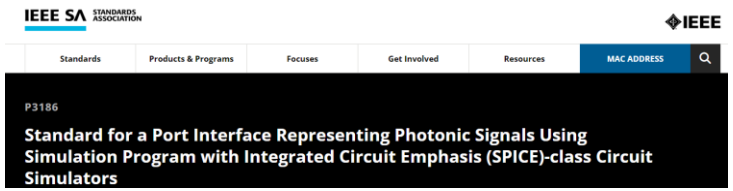
- Male/Female type unidirectional ports are widely used in photonic Verilog-A model, making schematic connection very restricted.
- **Ansys' Solution**: Bi-directional ports

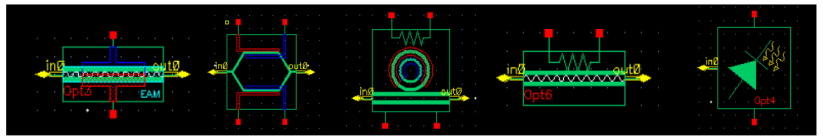




Challenge 2

- No industry standards for optical port interface!
- **Possible solution**: IEEE Working Group P3186





Challenge 3

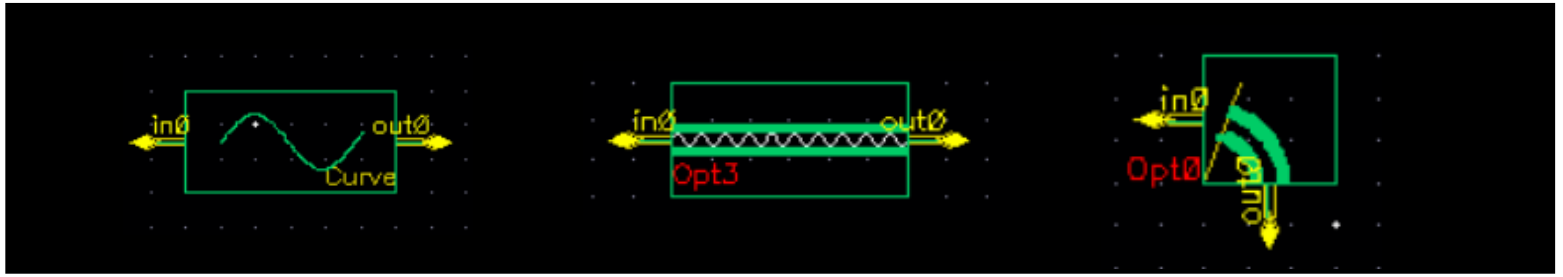
- Creating model requires a lot of model expertise
- Maintaining/updating complex models with hundreds/thousands lines of code is time-consuming.
- **Ansys' solution:** Automated model compiler!

Advanced photonic Verilog-A models

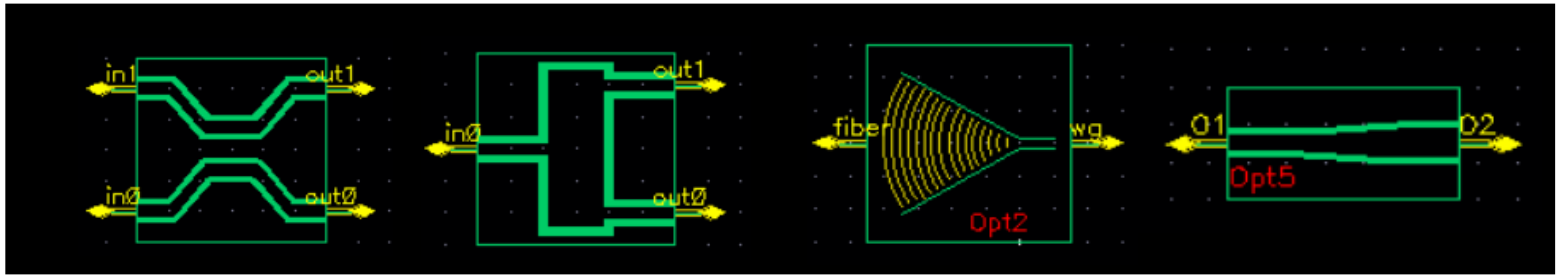
Ansys

Mode library overview

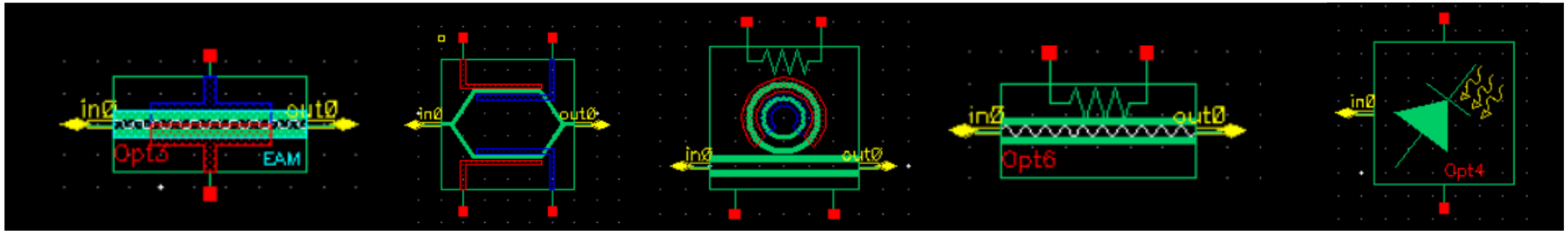
- **Waveguides:** Fixed and parameterized waveguides



- **Couplers:** Fixed and parameterized couplers based on S-parameters, grating and directional couplers



- **Actives:** Electrical/thermal phase shifters, ring modulators, Mach-Zehnder modulators, EAMs and photodetectors

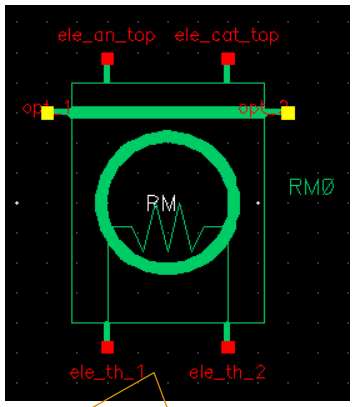


Ring modulator

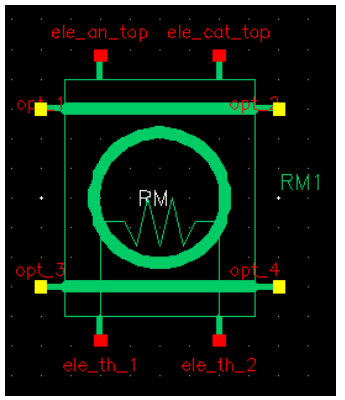
- Model source data:
  - Ring radius
  - Coupler data
  - Waveguide neff, ng, loss
  - Thermal tuner data
  - Carrier-depletion/injection tuner data
  - Electrical RC parameters
  - etc…

Compile

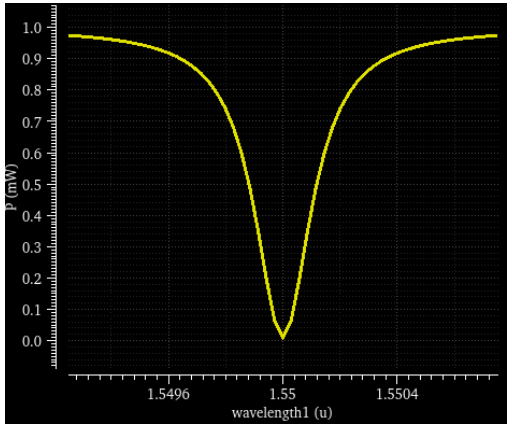
All-pass ring modulator



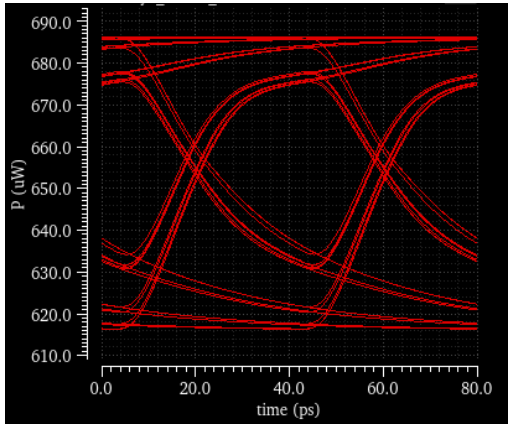
Add-drop ring modulator



Frequency sweep



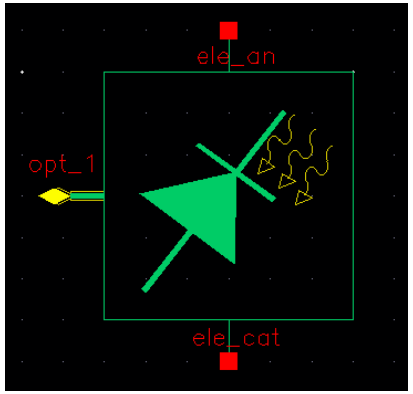
Time-domain modulation



Photodetector

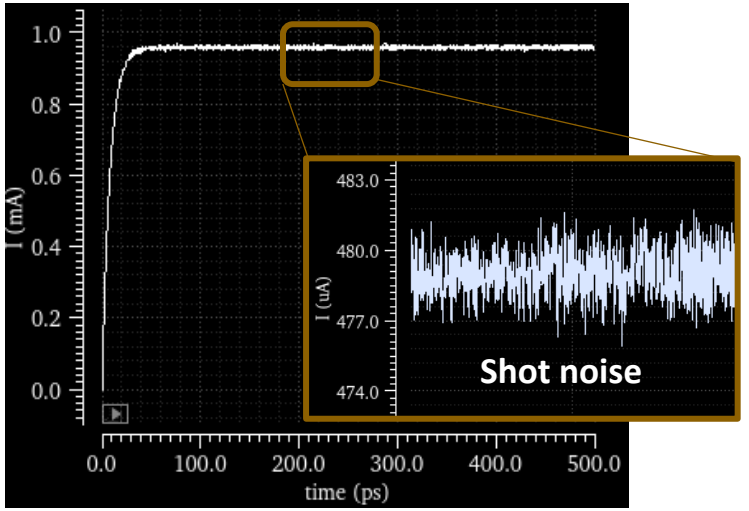
- Model source data:
  - Frequency-dependent responsivity
  - Voltage-dependent dark current
  - Voltage-dependent net bandwidth
  - Electrical RC parameters
  - Enable/disable shot noise
  - etc…

Compile



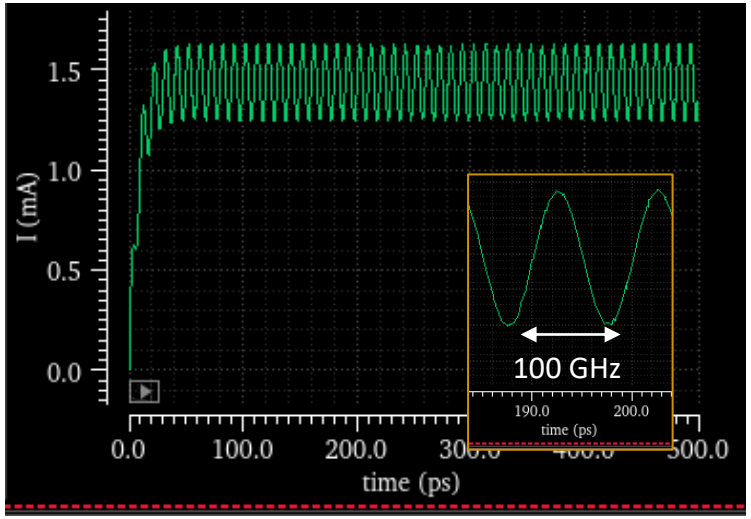
Transient response (1-ch input)

- @1550 nm, 1mW



Channel crosstalk

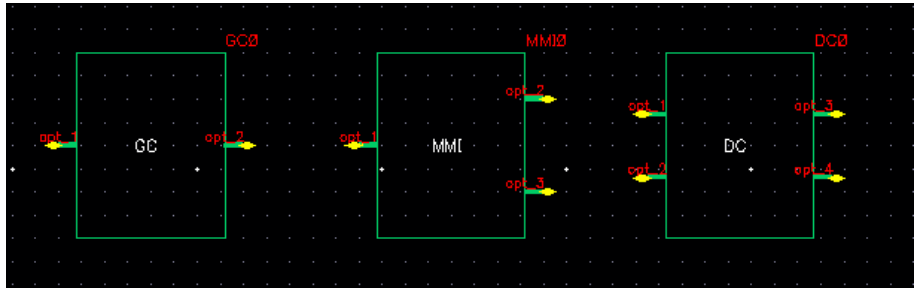
- @1550 nm, 1mW
- @1550.8 nm, 1mW



S-parameter elements

- Model source data:
  - Lumerical S-parameter data file
  - Touchstone S-parameter data file

Compile



.txt

gc_strip_te_c_S_params - Notepad

File Edit Format View Help

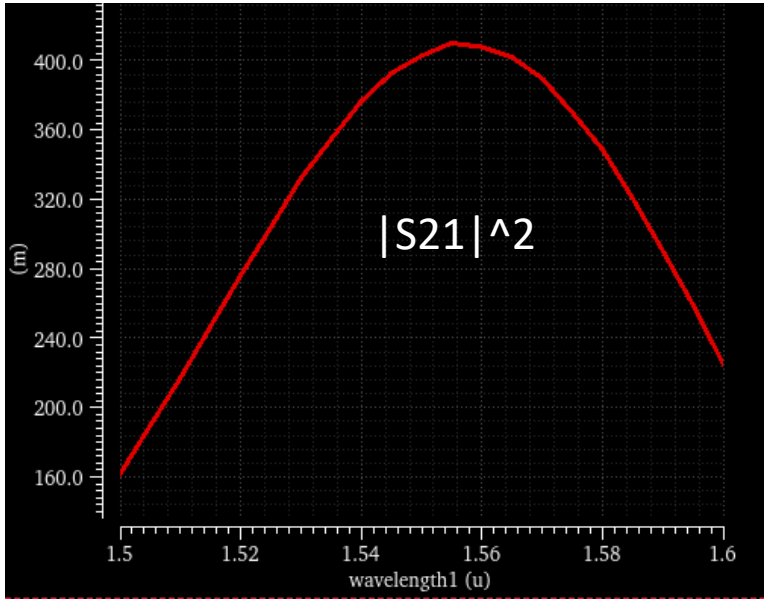
```
["port 1","LEFT"]
["port 2","RIGHT"]
("port 1","TE",1,"port 1",1,"transmission",0)
(50, 3)
1.873702862500000e+014 6.1510072296566035e-002 -2.4083991086875516e+000
1.8762521180952381e+014 6.5888041511021359e-002 -2.2061625103690039e+000
1.8788013736904762e+014 6.6778269975932697e-002 -2.0147206933514687e+000
1.8813506292857144e+014 6.5675594802082432e-002 -1.8756427170802863e+000
```

.snp

y_S_params - Notepad

File Edit Format View Help

```
! Ansys Lumerical
! Created Wed 12/09/2020 17:20:21.85
# HZ S MA R 50.00
! Ports: port 1, port 2, port 3
! Mode: label="TE"; ID=1

1.91428e+14     0.0322185       78.687  0.706023        -36.405 0.69198 -36.4156        0.706023        -36.405
   0.0472402    -5.57883        0.0243284       123.913 0.69198 -36.4156        0.0243284       123.913
   0.0473715    -5.72998

1.91518e+14     0.0308474       84.0228 0.705845        -29.6452        0.692091        -29.6558        0.705845
-29.6452
   0.0464452    1.97367 0.0240062       135.289 0.692091        -29.6558        0.0240062       135.289
   0.0465754    1.81826

1.91607e+14     0.0294763       89.3587 0.705671        -22.8854        0.692194        -22.8961        0.705671
-22.8854
   0.0456502    9.52618 0.023684        146.664 0.692194        -22.8961        0.023684        146.664
   0.0457792    9.36651
```



How to create models through automation?

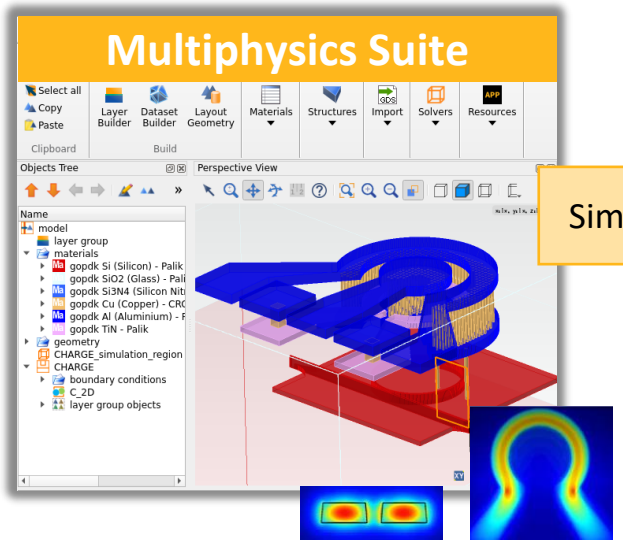
Ansys

Compact model library (CML) compiler

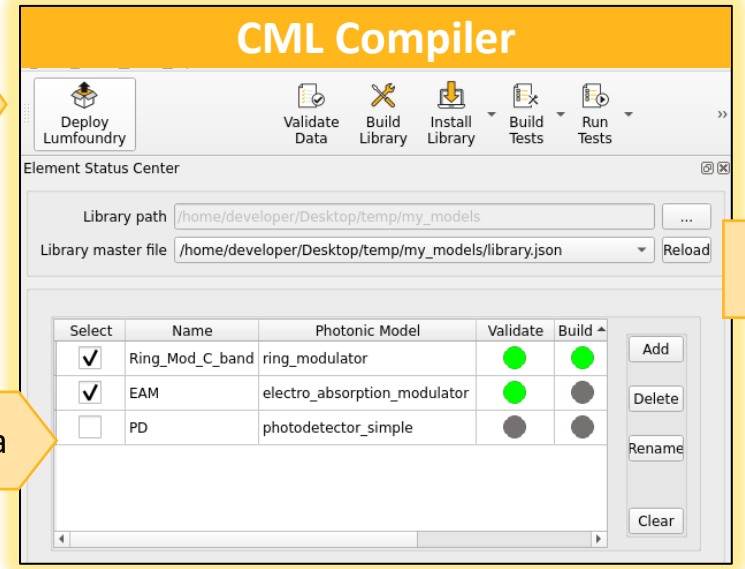
- Automates generation of photonic compact model libraries (CMLs)

Component data collection → **Compact Model Generation** → **Circuit/System Design**

Measurement data

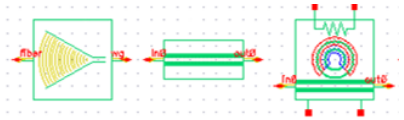


Simulation data



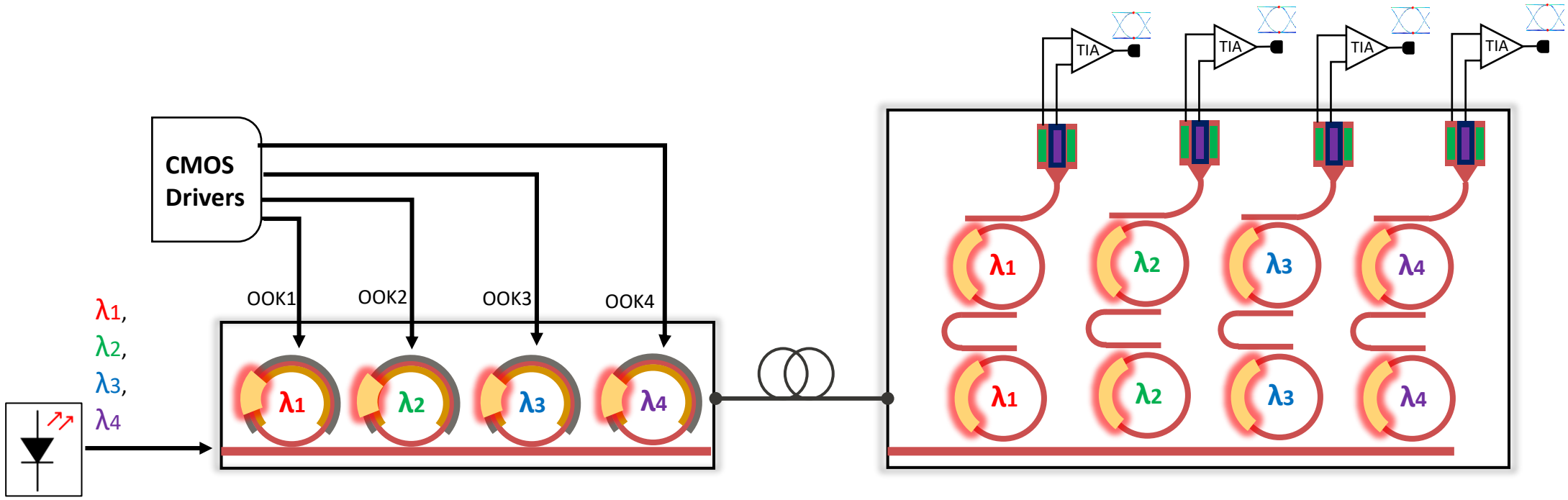
Compact models

Photonic Verilog-A models + Schematic symbols



Let’s see an example

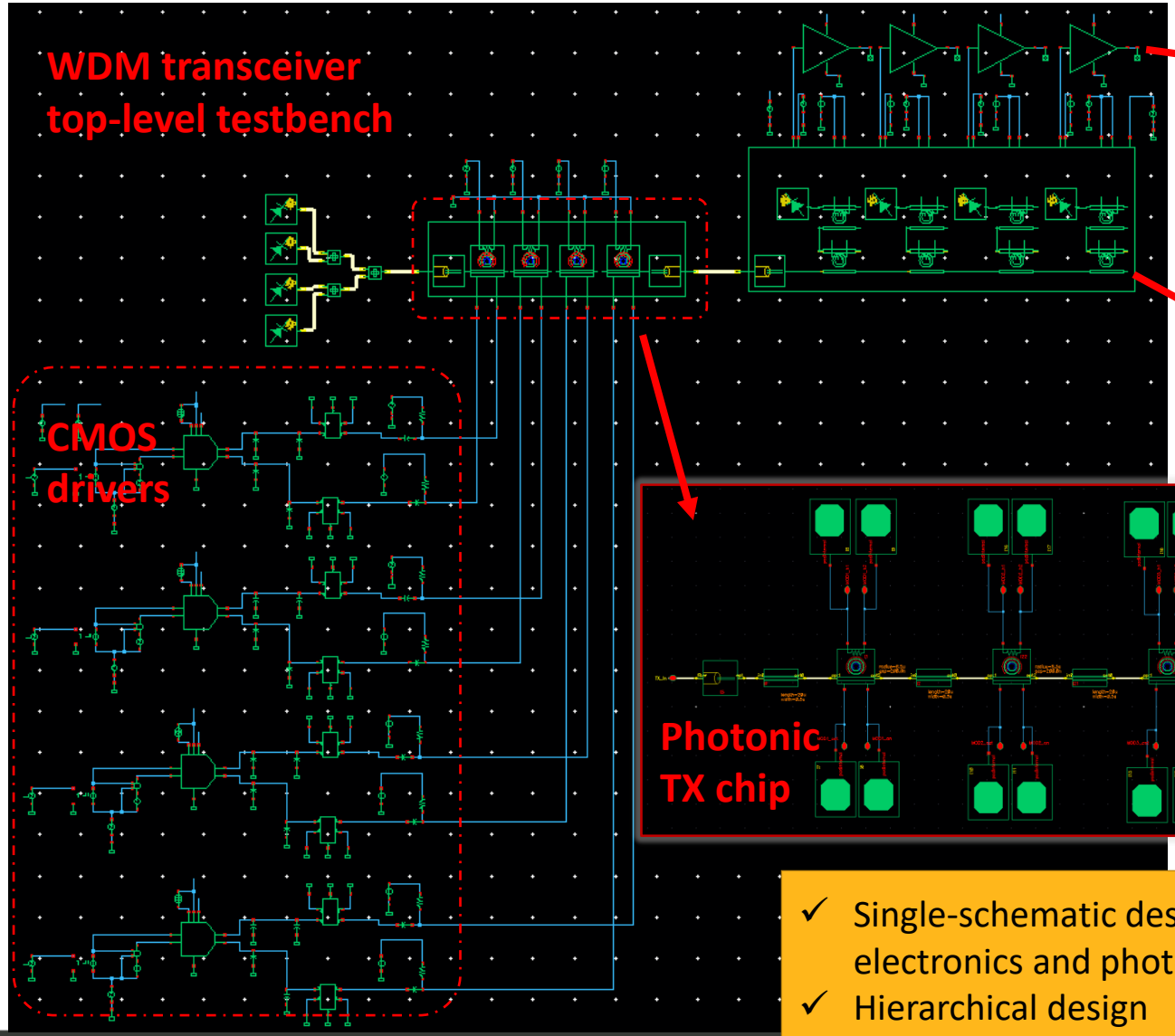
Example – 4-channel DWDM Transceiver Design



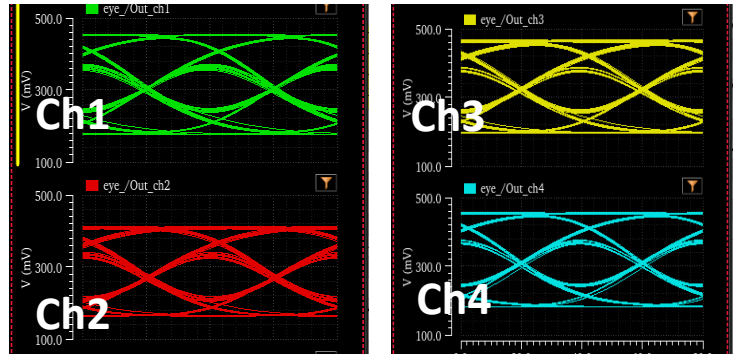
Silicon photonic (SiP), ring-based, 4-channel DWDM transceiver design

- **Channels**: 1551.72nm, 1552.52nm, 1553.33nm, 1554.13nm
- **Data rate**: 25Gbps x 4 = 100 Gbps

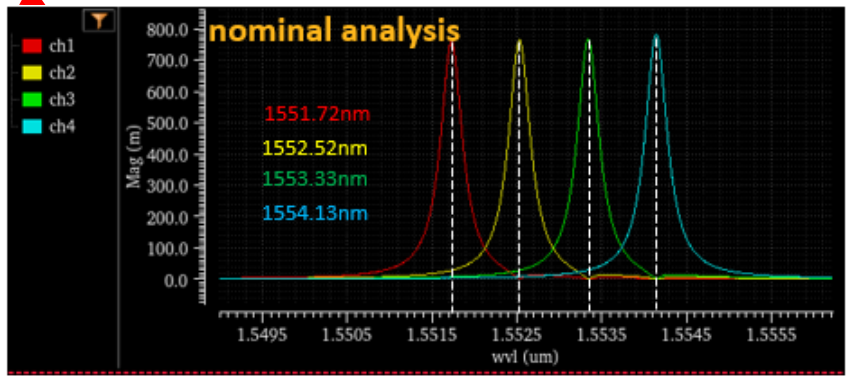
Schematic design & simulation



Transient eyes at TIAs



Frequency response of RX chip



- ✓ Single-schematic design for electronics and photonics
- ✓ Hierarchical design

Conclusion

- We presented the use of standard Verilog-A language for modeling advanced photonic components in PIC analysis, where complex, bidirectional, multimodal, and multi-wavelength optical signal are fully supported.
- Photonic Verilog-A models are compatible with commercial SPICE solvers, making them ideal for EIC and PIC co-design and co-optimization.
- Ansys' CML Compiler can help creating Photonic Verilog-A models in automated approach.
- Model vendors and EDA vendors need to work together to create IEEE standards for optical port interface!


Ansys